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Implementation and Analysis of 32-Bit TCAM (Ternary Content Addressable Memory) using FPGA

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Abstract:

Content addressable memories are implemented in FPGAs for the applications in the 5G networks to improve their performance. CAM's are searching devices which can search the input according to their address locations in one clock cycle. TCAM are implemented in the routing table in the networks to transmit the data in packets where don't care bits are chosen for the multiple address locations. In this paper FPGA based TCAMare implemented along with the use of other peripherals which are already available in the FPGAs. Compared with the previous TCAM architectures the proposed reconfigurable TCAM achieves better results in terms of power conserving. Hence the proposed TCAM's is implemented in FPGA's to improve the performance.

Keywords: 5G Networks, Field-programmable gate arrays (FPGAs), FPGA-deployed TCAM, power conserving, Routing Table.

I. INTRODUCTION

Field-programmable gate arrays are developed into system on-chip where processor cores that compete withapplication-specific integrated circuits (ASICs) in terms of performance [1], [2]. With tens of lakhs of reconfigurable digital signal processing slices and selective to design on SOC, they provide an incredibly flexible development platform. They can satisfy the requirements of commercial applications, constructing tile-communication systems, Voice over Internet Protocol, machine learning, and finance transaction systems, thanks to their wide range of buffersused to select input and output interfaces, due to high-speed connectivity and storage interferes are distributed well.

ASIC-based CAMs are more expensive, difficult to integrate, and less reconfigurable. However, they are having look up tables for their address locations to reach their destination with the use of matching ports to increase the throughput in network routers. The globe is evolving toward software defined networking, whose implementation calls for adaptable, reconfigurable, and high-performance hardware. When a software-defined CAM is required rather then a strong-wired CAM, FPGAs are the most appropriate platforms to build SDNs. These features are making FPGA- of the entire system is compared with the input searching with the address location based on the memory locations stored designs, which can provide good suppliers waste lot of power.

II.RELATED WORK

The majority of Content Addressable Memories (CAMs) and Ternary CAMs (TCAMs) are utilized in networking devices. CAMs offer read and write functionalitysimilar to a standard memory, but they also support search, which will locate the index of any matching data throughout the memory. Particularly in TCAMs, wildcard bits that match one and zero can be used. These wildcards canbe used for both memory access operations (signaling that some search bits are "don't cares") and for storing the data itself (Indicating some bits of the data should not be used for Determining a match). Many complex actions, such looking up a routing table, are made easier to accomplish because to TCAM's completely parallel search. The ordering of the pieces in the TCAM is less crucial because the TCAM searches every location in memory at once, and huge indexing structures are frequently completely avoided. This parallel search can be used as the foundation for more complicated searching schemes [6] and directly implements the requirements of specific applications, like IP-lookup [9], [11], [6], and [12]. TCAM is also utilised in various high- speed networking applications, including pattern matchingfor intrusion detection [10], access list control, packet classification [4], [6], and [9].

The three designs are built on RAM blocks, LUTs, and registers. Despite the fact that CAM implementations differ from Ternary CAM implementations, [7] offers some guidance for assessing CAM implementations in FPGA, which might serve as a foundation for evaluating our TCAM implementation on FPGA. Since TCAMs consume a lot of electricity, muchTCAM research focuses on ways to make them use lesspower. The motivation behind RP-TCAM [1] comes from the fact that TCAMs' high dynamic power consumption is brought on by the regular charging and discharging of their highly capacitive match lines. In [1], a selective pre-charge strategy is suggested. With this, a match line is only charged if the first four bits of the TCAM word match exactly. Achieving a search time of 1.86ns, RP-TCAM consumes80% lesser power.

Despite the fact that TCAMs are extremely helpful in high-speed applications, many system designers are concerned by their power consumption. Several methods have been put out to lower TCAM power usage by searching only portion of the TCAM [9], [11], [12]. It is possible to speed up a variety of program profiling applications and techniques [8] and data flow tracking mechanisms [1], [9] by using TCAMs for quick lookups with all feasible power- saving mechanisms. The authors of Cool CAM [9] make the assumption that the power usage is inversely correlated with the number of rows. They offer a collection of sophisticated algorithms and a two-level TCAM design, which need searching fewer rows and hence use less power overall. Although their presumptions are a good approximation for relative estimations, it would be preferable to have an absolute quantitative figure for power savings in terms of Joules or Watts. The power usage is decreased in Ease CAM[11] using a page-based system, and the authors base their energy savings on the use of CAM in Cacti (which is different than a TCAM). There are more works that offer to minimize the number of bits in contrast to these row trimming strategies [5].

We intend to look into the possibility of enhancing the most recent TCAM implementation such that it offers power performance that is comparable to Bloom filter without sacrificing latency advantages. Networks that make use of software-based controllers and Application programmable interfaces (API) that are used to configure the networks dynamically and supports underlying network hardware infrastructure using clous services and to direct network traffic are the succeeding networks that empowers thedesign to be more adaptable and programmable using a centralized controller. Field-Programmable Gate Arrays provides flawless hardware to render these versatile networks. Ternary Content-Addressable Memory (TCAM) is a crucial hardware module of network devices to carry out packet classification and forwarding, but these were lacking in present day FPGAs. Explorers and FPGA retailers have put forward countable blueprints to contend TCAM by making use of accessible memories on FPGA, in spite of that they are energy incompetent because of, turning on full IC (Integrated Circuit) in a single search operation.

III.PROPOSED ARCHITECTURE

The memory storage in the TCAM is done with thedivision of banks which shrinks the memory they cause the bank overflow. The input data in the TCAM will store in any pattern based on the address locations, if the selector bits are chosen same in the memory allocated data. For example, the TCAM is split into 4 equal banks and each one having the selector bits according to their memory size. Based on the selector bits appropriate bank will select and banks are mapped with the address locations where the data is going to store in the particular bank.

If all the memory locations are completely filled and thenew data is ready to store the data when already the memory is full. This condition is called the bank overflow which causes the loss of data. Hence a new rule is implemented to reduce the overflow of TCAM architecture. In practical applications, the data is stored in random locations andthe chances of selecting the same bank is very less. Hencethe overflow data is almost reduced and the propagation of data is stored in the different banks.

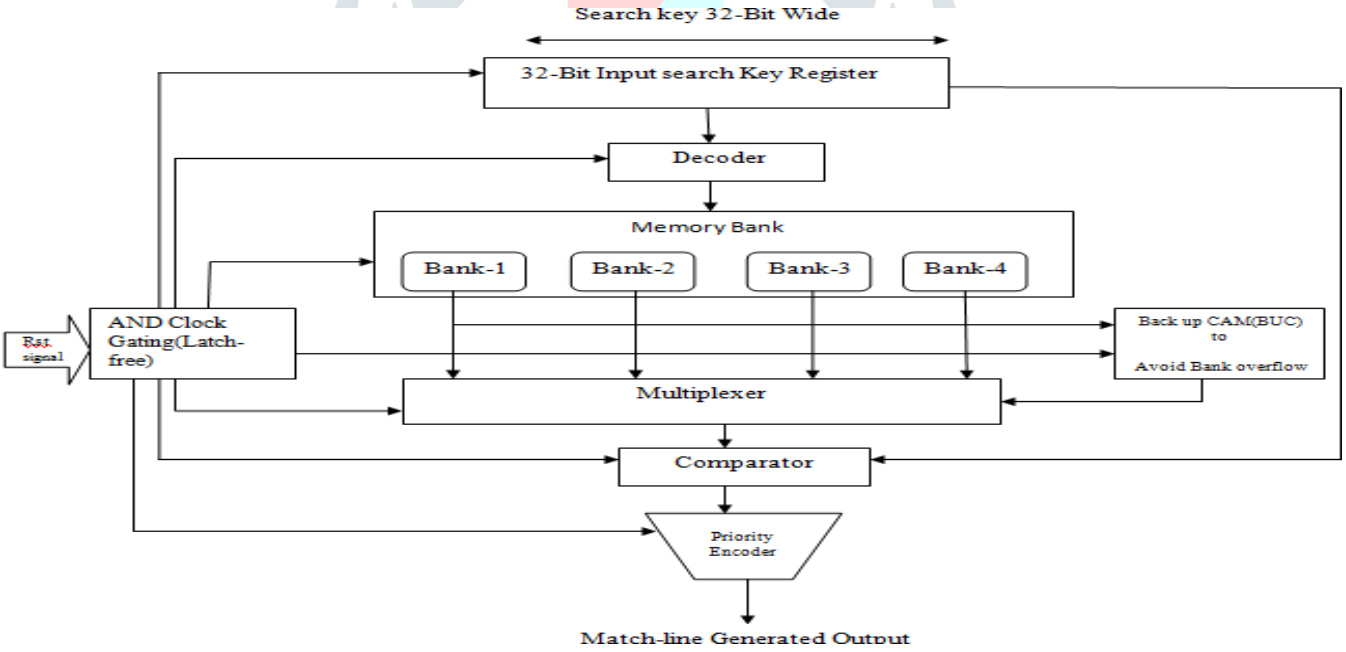

Fig. 1. TCAM System Proposed Architecture.

The overflowed data is stored in the extra memory called as the backup CAM. The proposed 32-bit TCAM design is shown in the Fig.1.The width of the backup memory is same as the TCAM width, and bank storage is reduced to half of the banks of TCAM. The overflowed data and the input data are put down in particular location hinge on the match lines. When the selection bits are same and greater than the deepness of the individual banks the data put down in the backup memory is put down in the banks of the TCAM. Hence the overflowed is stored in the TCAM without any loss of data and selector bits. Hence the proposed RPE TCAM achieves better performance compared with the previous TCAM architectures.

The proposed TCAM achieves low power due to its modified design. Here the TCAM investigates the whole memory locations in single clock cycle which reduces the delay time. The TCAM memory investigates all the possible bit variations including don't care conditions and high impedances also which had a higher searching address locations based on the matching lines. The read and write

cycle of the memory depends on enable conditions of both the matching lines.

The power consumption in the TCAM is more for searching algorithm which can be finished in one clock cycle. The TCAM memory is operated based on the rising edge of the clock and enable conditions of write and read signals. The power dissipation in the TCAM is bring down by using various low power consumption techniques. In this paper bit wise logical elements in the searching algorithm which improves the power efficiency for enormous data. Hence the proposed TCAM architecture achieves low power and high speed when collated with previous TCAM designs.

The Proposed 32-bit TCAM architecture has the following blocks. Which Supports the Processing of 32-Bit input data to the output as shown in the above Fig.1. TCAM System Proposed model. This System has the following blocks called building blocks such as logic Selector, Decoder Encoder, Priority Encoder, Comparator and BUC (Back up CAM), AND Clock Gating Circuitry along witha Memory Bank Which is Shrink to form a 4-Divisible Banks. The above Block diagram is the Architectural overview and implementation of 32-bit TCAM (Ternary Content- Addressable Memory). With the help of this Design implementation of 32-bit TCAM is possible with low lower dissipation. Total power consumed by the circuit is reduced by using Clock gating and Line Encoding techniques. BUC are utilized to minimize Data Redundancy problems.

This BUC plays crucial part of the design and eliminates unwanted data propagation, in case of uneven functioning of the combinational circuits like Logic selector, Priority Encoder, Decoder and Comparator used in architecture. Cache Memory is used in the circuit for efficient utilization of the main Memory Bank and quicker data processing. The input search key of 32-bit is given to the 32-bit register and it is passed through the stages of Data filtering and decoder, which is used to convert the input binary stream and converts into digital signals and passed through the clock gating circuitry, memory and MUX and through thepriority Encoder and produces the output.

The 32-Bit TCAM that allows selected part of the hardware to pull off the search query in single clock cycle and bring off an large scale-design space exploration to perceive the effective numeral of banks on Xilinx FPGAs, which results in utmost power conserving, a path break which terminates the memory shrinking using Backup CAM (BUC) is implemented as part of the hardware to precise the overflowed CAM entries and Bus Invert Encoding technique is implemented by using of Encoder and Decoder in the architecture for reducing the power consumed by Bus lines and also employing of this BUC acts as data filters for fault tolerance.

The proposed 32-Bit TCAM is having a 32-Bit search register which is used to store the search key on temporary basis and acts as a Cache memory, which was used in Architecture for fast processing speeds of input Query,resulting in faster search of inputs thus by increasing processing speeds. To conserve the power, Clock gating technique is implemented and to restrict the usage of power by hardware when not in use and supplies power to the hardware in operation and usage Power Conserved, speed together beside single-clock cycle update latency along-side no concession on the efficiency and scalability of the design when collated with other cutting-edge FPGA-rested TCAM designs with Reconfigurable CLB's.

The evolution of TCAM Architectures has changed the way of, the accessing speeds of IP look up tables and theirfast processing of data at very higher speeds and consuming low power by occupying the lesser area on the chip due to advancements made in IC manufacturing technologies. From input to output data operational speeds, it conserves a greater amount of power. The revolutionary speeds of TCAM from past to present has developed to a greater extent.

The Table 1 shows the different TCAM designs along with their design parameters i.e size,power, speed and time. All of among shown below the 32-bit low power TCAM architecture has done a best job in providing good results in all design parameters.

TABLE I: ANALOGY WITH OTHER CUTTING-EDGE TCAM; POWER:DYNAMIC POWER IN milli Watt, Analyzed by Xilinx XPOWER ANALYZER.

Design	size	Power in (mW)	Speed in (MHz)	Time period in (ns)
HP-TCAM	512x36	190	118	4.2
UE-TCAM	512x36	80	202	2.5
DURE	512x36	50	335	1.49
G-AETCAM	512x36	119	358	1.4
REP-TCAM	512x36	71	319	1.5
32-Bit TCAM	512x36	17	319	1.5

Table 1. Design metrics of Different TCAM Architectures

IV.PERFORMANCE ANALYSIS

Fig. 2. RTL Schematic Output of 32 Bit TCAM

The above Fig. 2 shows the Register Transfer level schematic output of 32-bit TCAM design. The RTL level states that data processing from register to register in design architecture using various combinational and sequential logics using combinational delays from input to output of the design. The above fig shows the entire hardware implementation in register level and also it shows the stream of digital signals between the hardware registers. This RTL is the combination of various combinational and sequential circuits.

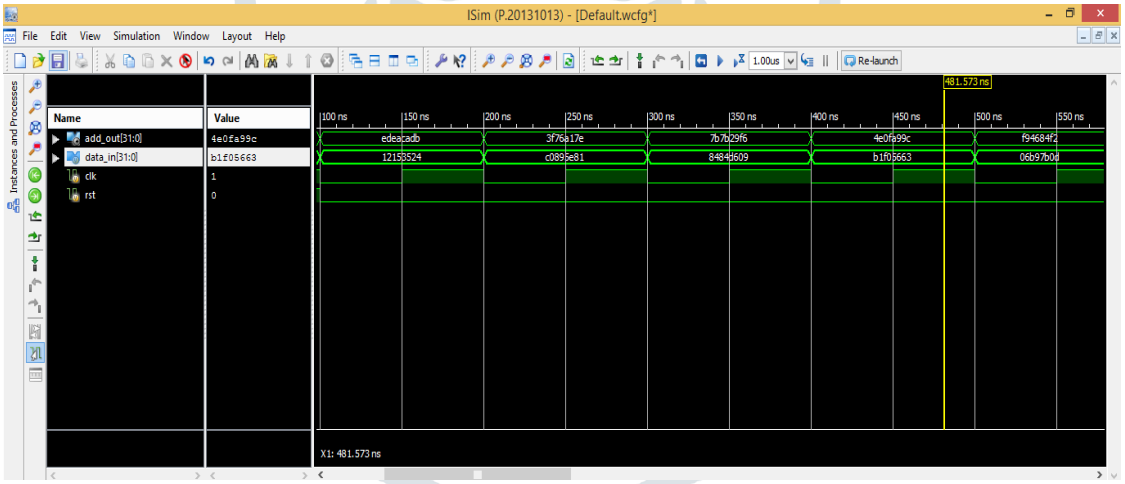

Fig.3.Simulation Result of a 32-Bit TCAM

The above Fig.3 shows the Simulation waveforms of 32-bit TCAM. This can help us realize the functioning of the circuit by giving input vectors also called as inputs to the design architecture. By giving clock vector to one i.e forcing clock to one the design is implemented and we can observe the functionality of the design we are giving clock constant because it is a synchronous circuit, these circuits are clock dependent and if reset is given as one it initializes the hardware.

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	5	---	---
Logic	0.000	87	46560	0
Signals	0.000	244	---	---
IOs	0.016	66	240	28
Leakage	1.293			
Total	1.310			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.621	0.001	0.619
Vccaux	2.500	0.045	0.000	0.045
Vcco25	2.500	0.007	0.006	0.001
MGTAVcc	1.000	0.303	0.000	0.303
MGTAVtt	1.200	0.213	0.000	0.213

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	2.7	81.4	53.6

Supply Power (W)	Total	Dynamic	Quiescent
	1.310	0.017	1.293

Fig.4.Power Analysis of 32-Bit TCAM

The Proposed TCAM Design has Incredible power drop of 76% of power conserved when accompanying with previous cutting-edge TCAM Designs. Compared to other TCAM designs this 32-Bit TCAM performs good in all design parameters, when compared to other TCAM designs

V.CONCLUSION

In the Existing System, the total on-chip power consumed was 71mw. In Proposed System Dynamic Power Consumed is 17Mw. which is 76% Percentage lesser then Existing System. TCAM's are implemented in FPGAs to improve data processing speeds. The proposed TCAM achieves better results in terms of power. With the configurability of the TCAM, the address searching and data has been transmitted at high-speed rate. The proposed architecture also achieves low power consumption, when collated with the previous designs.

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