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A Comparative Study on Different Type of Hybrid Full Adder Analysis

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Abstract : This study investigation various full adder such as xor xnor logic gate complementary metal oxide semiconductor (CMOS), complementary pass transistor logic (CPL) and transmission gate are full adder approches. The main objective find complete full adder that offer low power fast speed and good voltage swing is the primary goal xor and xnor is the less area. Most efficient Gluck and low power techniques is xor and xnor compared to traditional cmos technology. It require the fewest transistor. The main advantage of this electronic equipment is the reduction of the threshold voltage issues and the improvement of driving performance.

Index Terms - Reduced power, xor/xnor, CPL, TG

I. INTRODUCTION

The adder is a vital part of a CPU (central processing unit) an address generating unit (such as a catch or memory access unit), a floating-point unit, and an arithmetic's logic unit (ALU) [1]. It can be found in many VLSI system including micro processing and application-specific DSP architectures. It is a most valuable equipment as it contains several operations including subtraction multiplication division, address computing, and so forth. In the majority of these system, the adder is a part of the critique, which describes all effectiveness of the system. As a result a major objective is to improve the 1-bit adder cell's effectiveness [2].There are 2 types of static logic style: conventional logic and hybrid logic style. The single logic is utilized to instrument the entire FA representation in the standard way-dependent full adder. Pass-transistor logic that is complementary (CPL). Complementary pass-transistor logic style is an-other traditional method of implementing the FA architecture (CPL). To execute the FA design, CPL way approach uses double rail arrangement with transistors. Output node of this arrangement has a entire voltage oscillate, excessive speed, and good operative characteristics. Anyhow, because of enormous number of internal nodes in the cell, the circuit's fundamental flaw is significant power dissipation. Another issue with FA design is with layout, which is complicated due to the irregular transistor assembly. Pass transistor logic (PTL) is another traditional method for realizing the FA design. If logic "1" and "0" pass-by NMOS and PMOS transistors, correspondingly, the threshold loss problem emerges. As a result, the latest logic style and (TG) logic style, is employed to overcome the issue of threshold problem. Transmission gates are the most extensively utilized approach for dealing with the voltage-drop problem. It is based upon NMOS and PMOS transistors' complimentary properties: NMOS transistors transmit a powerful 0 but a fragile 1, conversely PMOS transistors transmit a strong 1 but a weak 0 Pass transistor logic (PTL) is a term used in electronics to represent numerous logic operations used in the construction of ICs. By deleting unnecessary transistor, it reduces the quantity of transistor needed to build different types of logic gates. We divide this whole paper into four different section (i) contain in basic introduction of the paper in which we include in flow of whole article. Section (ii) contain in five different topology. Section (iii) result and analysis is done on the basic of previously define architecture .The graph is various graphical representation is done on the basic of comparative table. Section (iv) contain the conclusion of different topology. On the basic of that we find out which circuit is best in the discussed configuration.

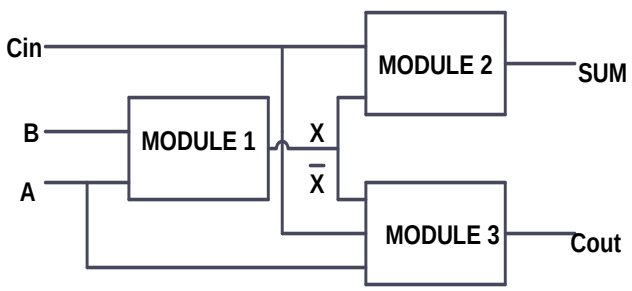

Fig.1 Three main logic structure of full adder cell in literature.

$$SUM = X\,Cin \oplus X\,Cin \quad (1)$$

$$Cout = XCin + \overline{X}Cin \quad (2)$$

In a full adder structure hybrid design concept and in the hybrid complete adder logic structure, three separates modules be utilized now given two input signal (A&B) in the first module and that the transfer complete oscillation signal (XOR-XNOR) at the output. The XOR-XNOR functions are generated by the first module in this architecture, and the resulting signals have strong driving capability and supply the whole output swing simultaneously.[4-5]. The TG and MUX are utilized to implement the SUM and CARRY operations in second and third modules, respectively. These hybrid logic architectures key advantage is that each module may be fixed separately.

II. Design Approach of the Different Type of Hybrid Full Adder.

1.1 Conventional 18T static CMOS circuit.

The static CMOS structure is used to construct the CMOS full adder [13] 9 PMOS and 9 NMOS transistor make up the design of hybrid full adder. This designs primary benefit is its capacity to generate full swing voltage. Due to the fact that the circuit of sum realizes on the carry out signal its cause's undesirable delays. Its uses more energy There are many transistors its make up more space [7] .Figure illustrate of CMOS full adder of structural layout.

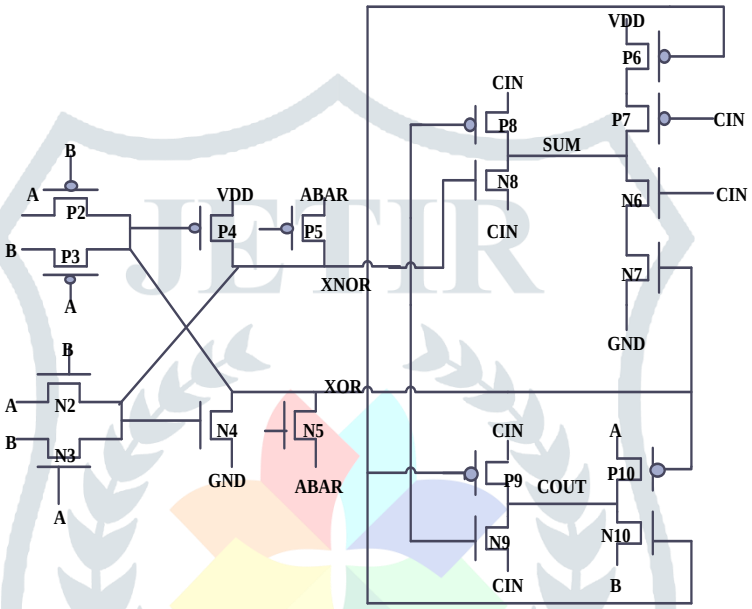

Fig.2 Conventional design of full adder.

1.2 Transmission gate based full adder.

In figure 3, transmission gate and transistor based inverter can be used to create a full adder. However a complementary CMOS find this to be irrational. Which effienctly design the controlled inverter utilizing a pair of transistor [9]. Since this full adder was designed using a total of 16T its power dissipation is higher but still less than of a 18T typical CMOS full adder design. The TG full adder is a transmission gate logic devices**.**

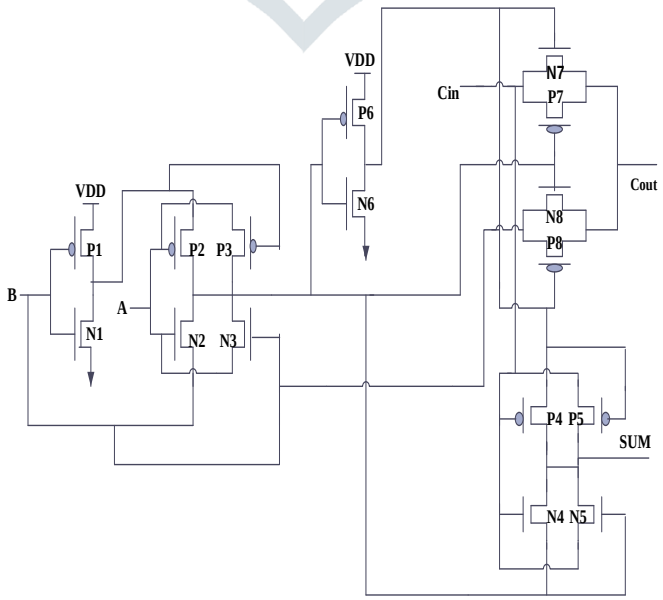

Fig.3 Transmission gate based 16T full adder.

1.3 CPL based full adder.

In figure 4 full adder circuit based on complementary pass transistors (CPL) includes of complementary put-in or put-out. NMOS pass transistor circuit is joined with CMOS inverter .Additional PMOS keeper in the circuit is utilities to less static power consumption and voltage swing restoration [7]. This system consist of a pass transis-tor network with two stage. The network is designed in two stage the first stage uses true input to drive pass transistor logic and the second stage uses complementary input to drive pass transistor logic [3] . Full adder circuit using CPL have the major issue of requiring degradation restoration in the NMOS network swing.

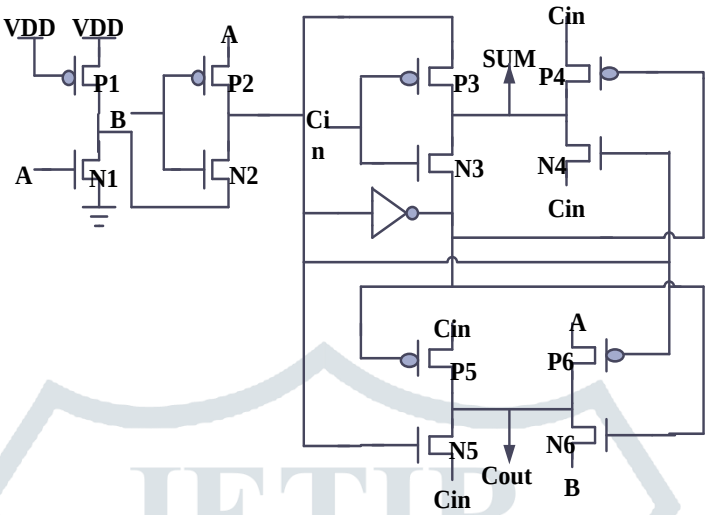

Fig.4 Full adder using CPL.

1.4 LPHS- Full adder.

In figure 5, it is suggested that a short power huge speed full adder, also known as an LPHS-FA, be used as an stylish method to simplify circuit electronic equipment and boost production. In contrast, a multiplier is utilized in implementing sum module, as shown in fig. Ci and Co are the input signals used in the multiplexer to carry out the logic operation, while H and H' are imputed to the multiplexer as control signals [8]. This electronic equipment has less power dissipation due to its less transistor count and all complete swing nodes structure without the threshold loss issue.

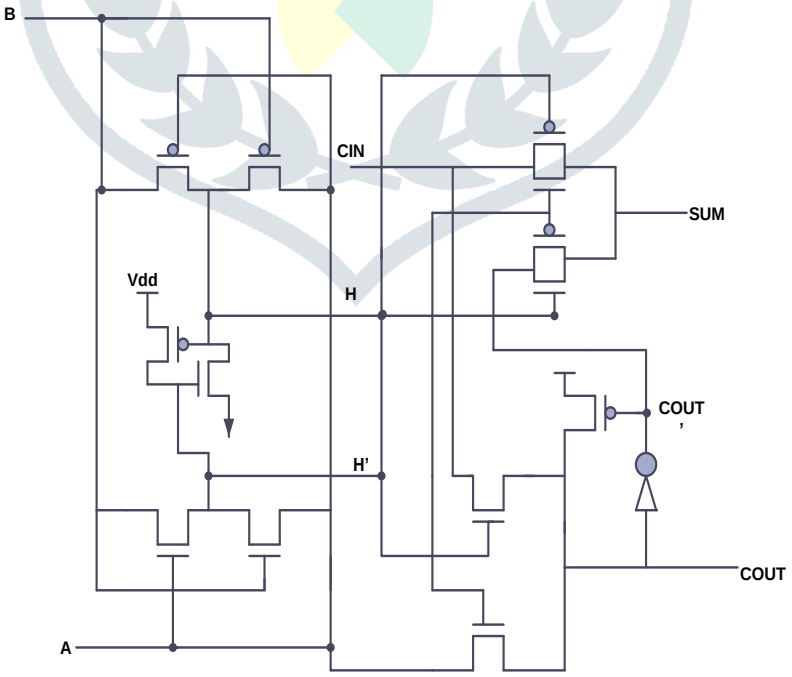

Fig.5 Full adder based LPHS

1.5 1-bit full adder using 20-T.

In figure 6, the hybrid CMOS full adder includes of 20 ICs and is built in the XOR-XNOR complete swing logic generation and transmission gate, pass transistor logic. The design includes ten PMOS pull-up and ten nicull-down transistors. The main advantage of this design in this circuit is that the higher delay in their design was resolved by using the CPL and

restored electronic equipment as presented in this hybrid full adder circuit [10]. The advantage of this circuit is that it solves the threshold voltage issue and improves driving capability.

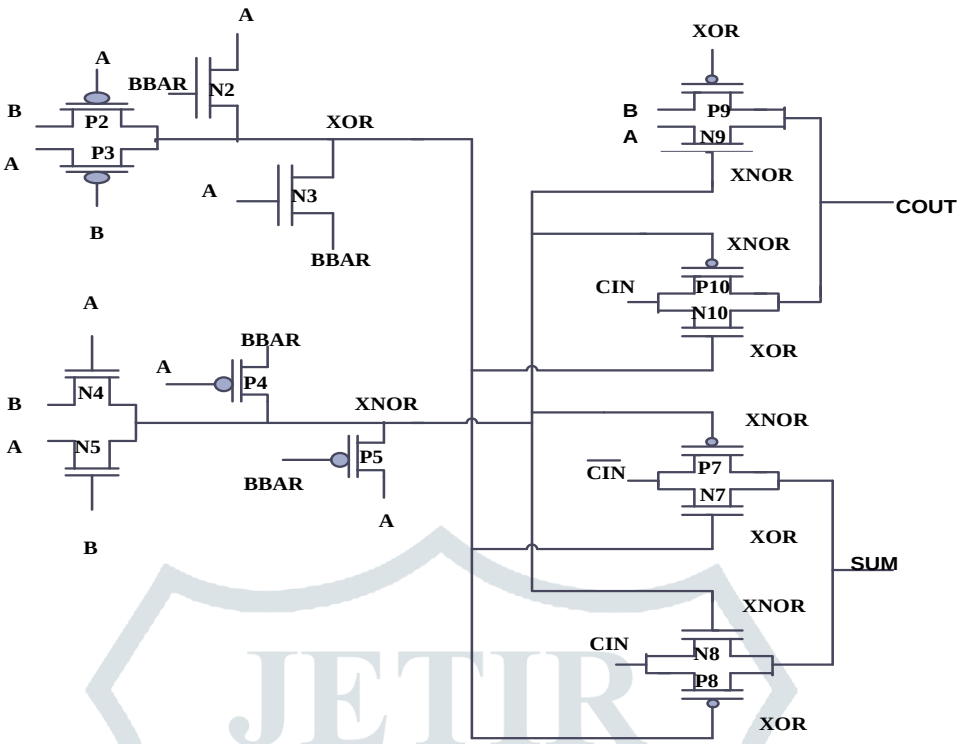

Fig.6 1- bit full adder.

1-BIT FULL ADDER SCHEMATIC DIAGRAM IN 90M USING CADENCE

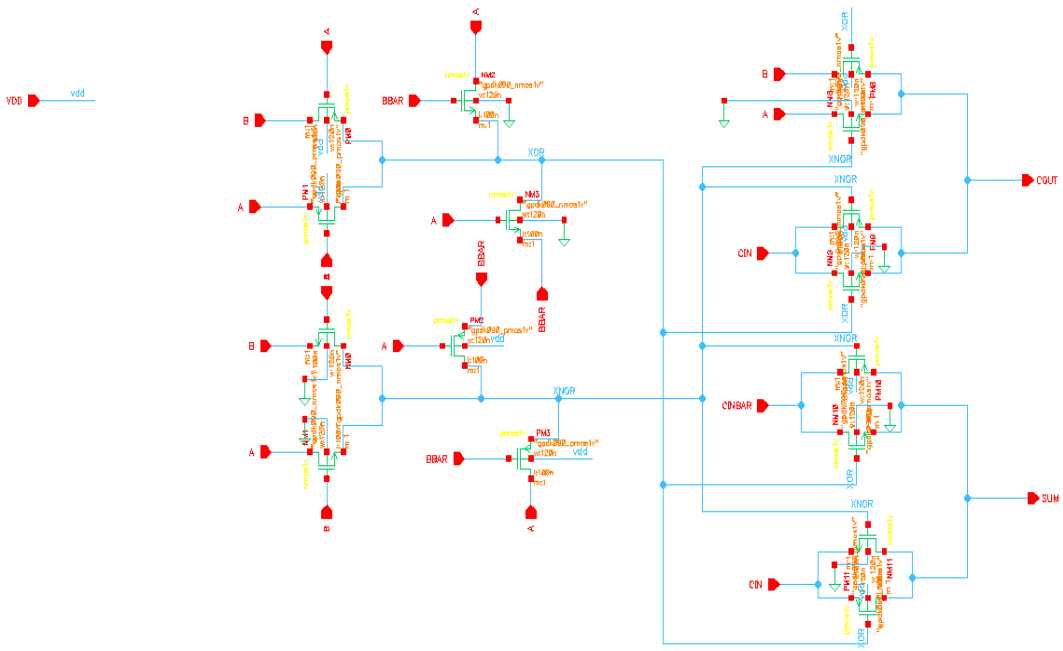

Fig.7 Schematic diagram of 1- bit full adder

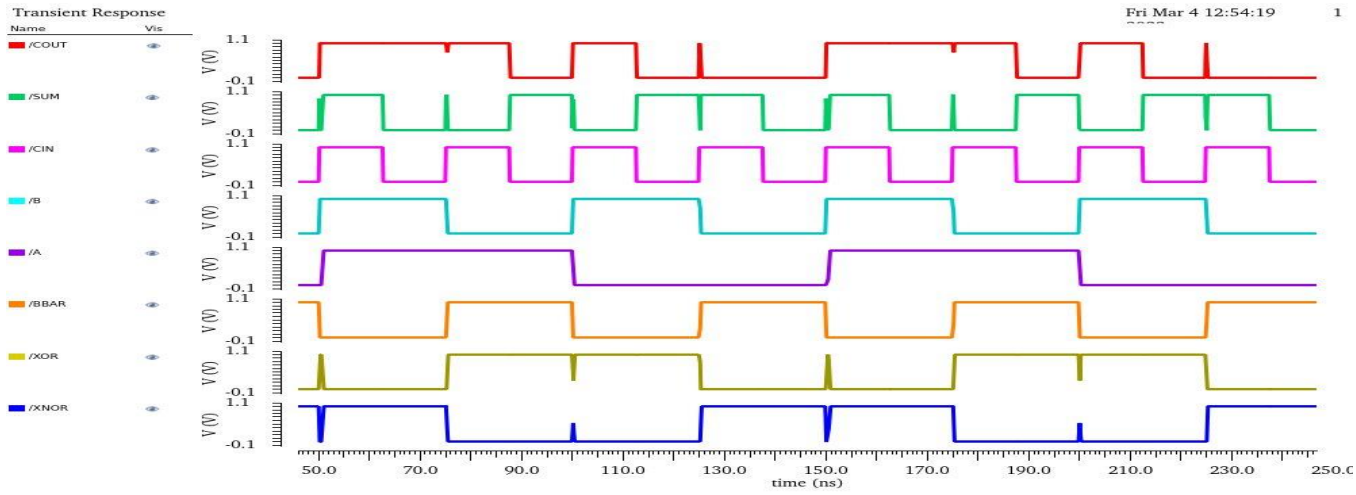

Fig.8 transient waveform of 1-bit full adder.

III. RESULTS AND DISCUSSION

Table.1 Show the comparison of various complete adder functionality in 90nm technology comparatively to other method of full adder and modified of xor xnor techniques then comparison of less than other transistor count, delay,pdp,power.

Table.1 COMPARISON TABLE

Full Adder	Delay(ps)	Power(µw)	PDP(fj)
XOR/XNOR BASED FA	38.1	3.586	820.44
TGFA	214.65	4.266	915.25
CPL	179.12	5.736	1026.75
LPHS-FA	224	4.15	936.52
20-T FA	36.1	2.53	931.38

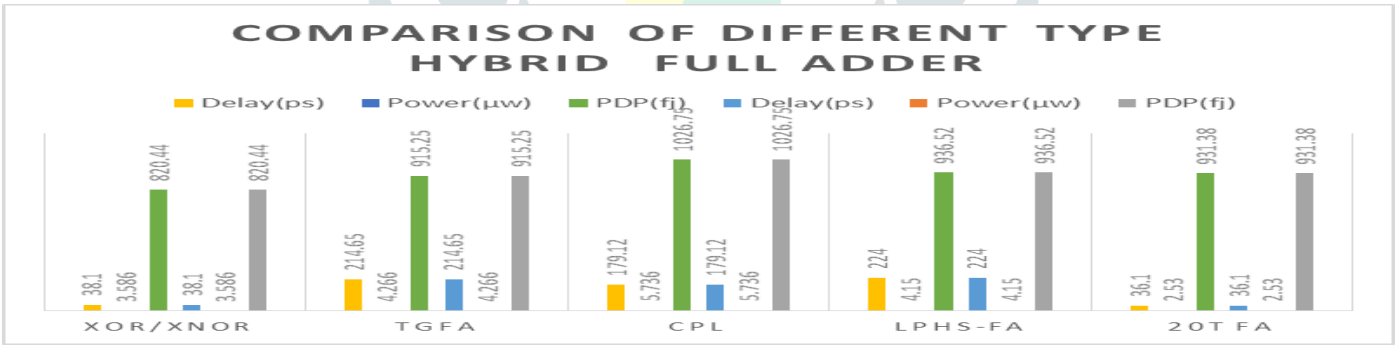

Fig.9 comparison of different topologies of full adder.

IV. CONCLUSION.

This article compares various full adder compositions. These complete adders were compared for efficiency utilizing 90nm technology in terms of delay, transistor count, and power consumption. Pass-transistor logic circuits dissipate less energy and take up less space, making them ideal for creating entire adder cells. A hybrid design provides VLSI designers the freedom to choose alternative modules to implement the circuit in accordance with their needs. The hybrid design technique using 20 transistors and a novel 1-bit FA design are provided in the current study. The suggested approach resolves the threshold voltage issue and improves driving performance. Additionally, the effectiveness is examined at various power supply and process corner terms. The results show that the suggested architecture is extremely strong in all states. Therefore, high-performance VLSI applications are appropriate for the suggested technique.

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