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Reversible Logic Gates and its Performances

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Abstract— **Heat is an important issue in VLSI circuits. But the reversible logic gives zero amount of heat dissipation. So, it's have a important role in nanotechnology, less energy complementary metal oxide semiconductor [CMOS] designs etc. It has been realized that quantum computing is one of the latest technologies using reversible logic gates. It is contemplating that accumulation extension of transistor density, energy desolation will command their limits in ordinary technologies. In ordinary area or range during the logic influence bits of orientation is erased resulting gratification of power in powerful amount. In the terms of reversible logic results are not lost.[1] This minimize the delays but at the amount of little hardware. So we can use reversible logic technology for decreasing the energy dispersion, heatwave dissipation, increasing rapidness etc. So it is used to maximize the speed and reducing energy consumption. In this, we can describe following reversible logic gates like fredkin, peres, Feynmen and toffoli gate etc.**

Keywords— Breakdown CMOS design, Reversible logic, Low energy VLSI, less energy CMOS design, nano scale technology, Adder, Subtractor, Mentor graphics tools.

I. INTRODUCTION

Power throw away is the dominant problem in the present day technology. Heat radiation due to illumination deficiency in high electronics component range and the combination fabricate using irreversible hardware was demonstrated. So, the damage of one bit of instruction lost, and will deplete KT*ln[2] joules of energy where, K is the Boltzmann's constant and K=1.38*10 -23 J/K, T is the absolute temperature in Kelvin. If instruction once lost it cannot be regained by any arrangement.[2] So according to this the fundamental connectional logic circuits release heatwave efficiency for every bit of instruction i.e reversible during the effect.

According to the Moore's law the number of transistors wills double every 18 months. Thus the power controlled appliances are the demand of the today's life. In this the output of the power radiation in a logical process deliver a blunt communication to the numeral of bits abolish during estimating. In this the better extended function of reversible connection lies in quantum computers[3].It has functions in different research operations such as quantum computing, nano technology, low power CMOS design, DNA computing.

II. BASICS TERMS USED

A. Reversible logic gate:

It is not apart advice us to dispose the results against the inputs but also advise us to incompatibly balance the inputs from the results.

B. Garbage output:

It is also associate to the representation of results which are not used in the synthesis of provided activity. In assertive covring these incline compulsory to accomplish reversibility [4].

Constant input value}+ Input value = Garbage value + Output value

C. Quantum cost:

The quantum cost of the design is less figure of 2*2 integrated gates to exhibit the design observance the results constant.[5]It is accredit to the cost of the design in the details of the part of a primary gate.

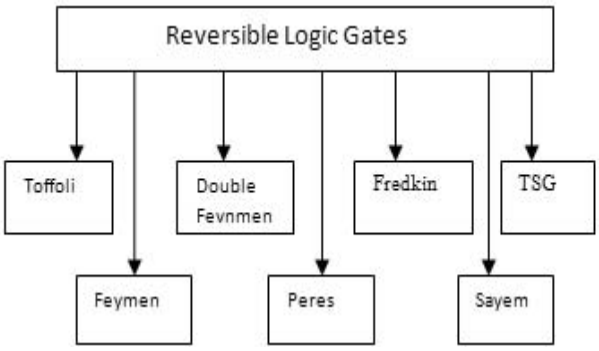
D. Flexibility:

Its indicate the collectivity of a reversible logic gates which accomplishing many activities.

E. Gate Level:

This associate the fraction of objectives in the design which is useful to conceive the provided connection[6].

III. TYPES OF LOGIC GATES



A. FEYNMEN REVERSIBLE LOGIC GATE

In this gate input and output is given by input [P, Q] and output [L,M]. So where the output is provided as L=P and M=P⊕Q.

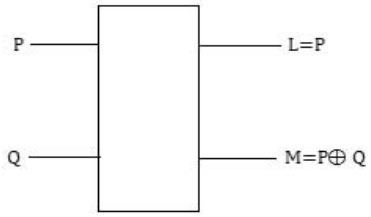


Fig1: Feynman Gate

Table 1: Truth Table

P	Q	L	M
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

B. DOUBLE FEYNMEN REVERSIBLE LOGIC GATE

In this gate input and the output is given by input [P, Q, and R] and output [L, M, N]. Where the output is provided as L=P, M=P⊕Q and N=P⊕R.

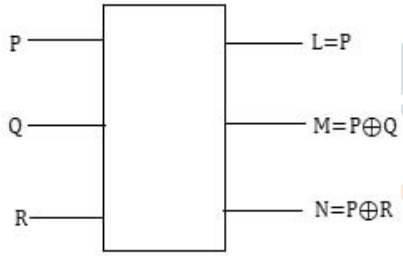


Fig2: Double Feynman Gate

Table2: Truth Table

P	Q	R	L	M	N
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

C. TOFFOLI REVERSIBLE LOGIC GATE

In this gate, input and output is given by input [P, Q and R] and output [L,M,N]. Where the Output is provided as L=P, M=Q and N=PQ⊕R. Its quantum cost is 5[7].

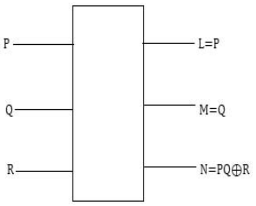


Fig3: Toffoli Gate

Table3: Truth Table

P	Q	R	L	M	N
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	0

D. FREDKIN REVERSIBLE LOGIC GATE

In this gate input and output is given by input [P,Q and R] and output [L,M,N]. Where the output response is L=P, M=PQ⊕PR, N=P'R⊕PQ.**[8]**

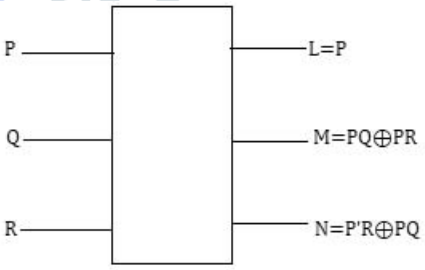


Fig4: Fredkin Gate

Table4: Truth Table

P	Q	R	L	M	N
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

E. PERES REVERSIBLE LOGIC GATE

In this gate input and output is given by input[P,Q,R] and output[L,M,N] and its result is L=P, M=P⊕Q, N=PQ⊕R. Its quantum cost is 4.

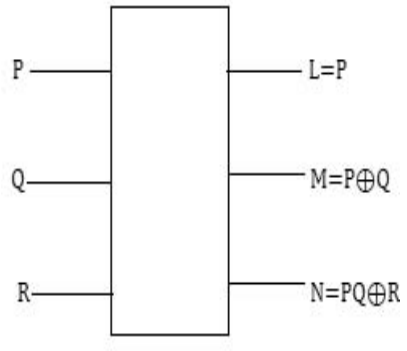


Fig5: Peres Gate

Table5: Truth Table

P	Q	R	L	M	N
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

F. TSG REVERSIBLE LOGIC GATE

In this gate input and output is given by input[P,Q,R,S] and output[L,M,N,O]. This is performing is function single reversible full adder and operate by the Boolean function. So its provided output is L=P, M=P'Q⊕PR, N= P'Q⊕PR⊕S and O=PQ⊕P'R⊕S.**[9]**

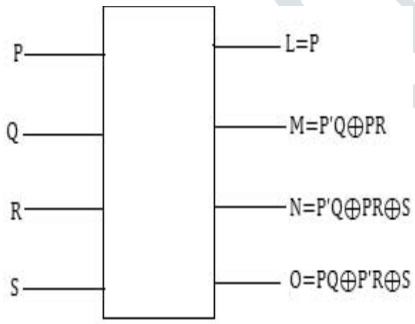


Fig6: TSG Gate

Table6: Truth Table

P	Q	R	S	L	M	N	O
0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	1	1	1
0	1	1	0	0	0	1	1
0	1	1	1	0	0	0	1
1	0	0	0	1	1	0	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	1
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	0
1	1	1	1	1	0	0	0

G. SAYEM REVERSIBLE LOGIC GATE

In this input is [P,Q,R,S] and outputs [L,M,N,O]. So the outcome is L=P,M=P'R'⊕Q',N=[P'R'⊕Q] ⊕S' and O=[P'R'⊕Q']S⊕[PQ⊕R].[10]

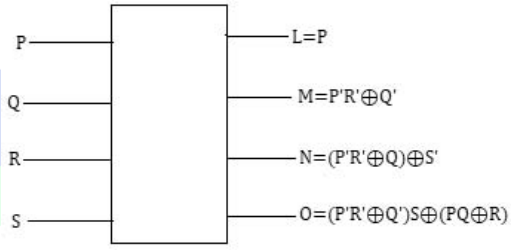


Fig7: Sayem Gate

Table7: Truth Table

P	Q	R	S	L	M	N	O
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	0	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	1

1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	0
1	1	1	1	1	1	0	1

IV. DIFFERENCE IN THE FORM OF ENERGY CONSUMPTION AND DELAYS BY USING LOGICAL GATES:

Name Of Gate	Input Given	Output Response	Energy Consumption[mw]	Delay [ns]
Feymen Gate	3	3	18	7.465
Fredkin Gate	3	3	18	7.824
Sayem Gate	4	4	18	7.824
Toffoli Gate	3	3	24	7.465
Peres Gate	3	3	24	7.824
TSG Gate	4	4	24	7.850

Fig8:Differential reversible logic gates [11]

V. DESIGN OF ADDER AND SUBTRACTOR BY USING REVERSIBLE LOGIC GATES:

Reversible circuits are designed by using the reversible logic gates only. There are many circuits of 1-bit full adder and subtractor design [12]. Here two circuits are design of full addrr and subtractor

Using 4 and 8 reversible logic gates and in this we can desing our circuit in the terms of reversible logic gates but using pass transistor and CMOS .

A. 1-bit fulladder and subtractor:

In fig.9, 1-bit reversible full-adder and subtractor[13] using the 3 Feynman gates, 2 TR gates, 1 Fredkin gate and 2 Peres gates to design the circuit. And the control input is given to the switch in between adder and subtractor. If provided control input is 1 then addition is achieve and if that is 0 then subtraction is achieve.[14]

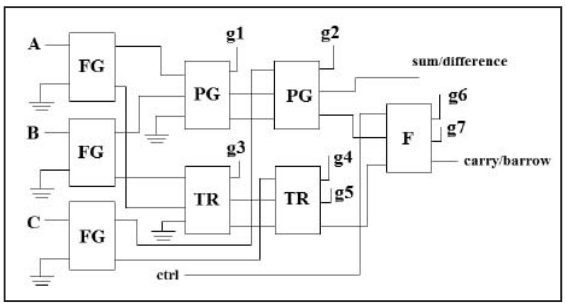


Fig 9: Design 1of one bit full adder/subtractor

Now, fig 10, in this we can use 2 Peres gates and 2 Feynman gates[14] and provide the control input to the switch between full adder and subtractor, so then, now if the control is 0 then adder is created or if i.e 1 then the subtractor is created.

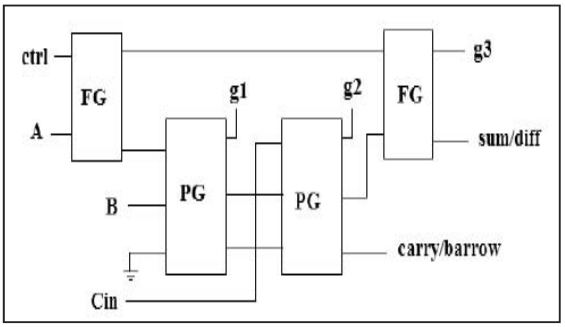
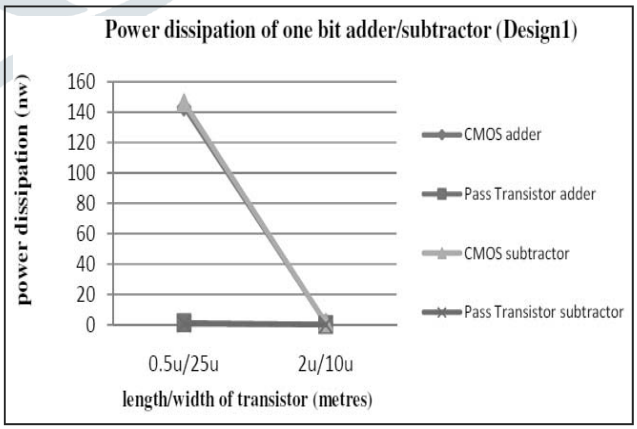


Fig10: Design 2 of one bit full adder/subtractor

VI. SYNTHESIZTION PERFORMANCE OF 1-BIT FULL ADDER/SUBTRACTOR DESIGN USING SUPPLY VOLTAGE 5V[15]

Reversible circuit	Logic family	No of transistors required	Length/width of transistor	Power dissipation (watts) adder	Power dissipation (watts) Subtractor
adder/subtractor design 1	CMOS	194	0.5u/25u	143.1620 n	146.258 n
			2u/10u	1.367 n	1.3680 n
	Pass transistor	72	0.5u/25u	1.4283 n	613.7312 p
			2u/10u	185.6219 p	184.3425 p
adder/subtractor design 2	CMOS	88	0.5u/25u	68.144 n	82.680 n
			2u/10u	696.199 p	656.185 p
	Pass transistor	36	0.5u/25u	276.6720 p	9.9716 n
			2u/10u	90.5589 p	86.8545 p



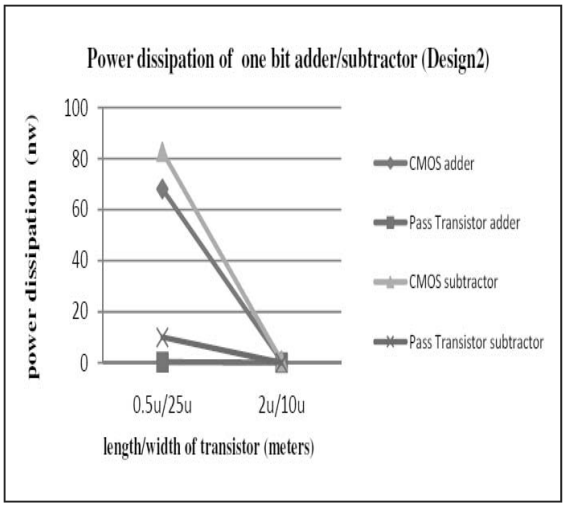


Fig11.Graphical representation of 1 bit adder/subtractor of design 1 anddesign 2[15]

VII. APPLICATION AREAS

Reversible logic gates are used in the security system, increasing excessive power productivity, rate and effecting, less energy wastage etc. [16] It includes some of the areas like design of low power digital circuit, field programmable gate arrays in CMOS, low power circuit designs, nano technology and the optical computing etc.

VIII. CONCLUSION

Use of the reversible logic gates are increasing day by day but the scientists are still continue with their work on this to further more decreasing environmental decay growth . So mostly we can use this for the power consumption. In this paper we just explained the types of the logic gates and its uses and how we can implement on these logic gates. In this Paper we can show the BCD adder circuit and after use of reversible logic gates definitely its energy consumption and delays are less than its actual circuit design. In this we can use the reference [17] in which we compare all types of the logical gate and we get our result of energy consumption and delays, in this Fredkin gate, Feynman gate, Sayem gate has low power consumption and Feynman gate and toffoli gate has less amount of delays**.**

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