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Analysis and Implementation of MAC Using Karatsuba Multiplier for DSP

[1]V.Tejaswi, [2]Smt.P.Puspalatha

[1]M.Tech Student,[2]Assistant Professor of ECE
[1]Department of Electronics and Communication,
[1]University College of Engineering JNTUK, Kakinada, Andhra Pradesh
[2]University College of Engineering, JNTUK, Kakinada, Andhra Pradesh

Abstract : MAC unit is mostly used in Digital Signal Processing Applications. It performs the application of both addition and multiplication operation. In this project, the main aim is to Implementation of MAC unit using the parallel prefix adder like Brent Kung adder and Karatsuba multiplier and Parallel-in, Parallel-out Shift Register. This adder is the high speed adder to improve the speed of MAC unit and multiplication purpose. This adder is implemented to Karatsuba multiplier and to design the MAC unit. The performance and analysis of MAC unit is done by verilog code and the MAC unit is simulated and synthesized in Vivado HLS 2019.1 software. Here, by using optimized MAC using Karatsuba multiplier the power and delay is reduced when compared with optimized MAC using Wallace tree multiplier. The simulation results shows power, high speed and low area consumption MAC unit.

IndexTerms - **MAC unit, Karatsuba Multiplier, Brent Kung adder, Parallel-in, Parallel-out Shift Register.**

I. INTRODUCTION

Digital Signal Processing contains multiplication and accumulation operations as a major part and MAC units plays a major role in implementing that operation in those DSPs applications. Actually, Previous successive products are added and stored in a register. By using Karatsuba multiplier the MAC application is used. Here, Karatsuba algorithm is one of the fastest way to multiply long numbers**.** Using Divide and Conquer, The inputs of MAC unit are given first to the register location and then given to the multiplier. These method consist of combination of advanced adders and multipliers. Efficient adders include Brent Kung adder and Advanced multipliers of Karatsuba Multiplier. MAC unit operates in two stages. Initially, the multiplier produces some number and then the result is forwarded to the second stage. In next stage, accumulation operation occurred. Multiplier takes two 8-bit numbers as inputs.MAC unit proposed supports one 16-bit MAC operation or addition of two 8-bit multiplications plus a 16-bit sum.

II. LITERATURE REVIEW

A.Mounika et.al [1] proposed that Hybrid Multiplier - based Optimized MAC Unit that, together with an effective hybrid adder network, targets the decrease in computational complexity in multiplication as a unique optimized MAC unit with runtime adjustable multiplier. The multiplier is built with reprogrammable controller logic blocks that guarantee optimal resource usage, lower power consumption, and suitability for applications in portable devices. It uses a FIR filter applications can be added to this improved MAC unit implementation. The Urdhva Triyagbhyam sutra and the Karatsuba algorithm are combined to create the integrated multiplier.

S. Rajapriya et.al [2] proposed that A Novel Architecture for Multiplier and Accumulator unit by using Parallel Prefix Adders that their used 64-bit carry save adder and it is taking maximum area on the chip, but its combinational logic delay is less when comparison to carry look ahead adder circuit. Hence, these adders are combined with array multiplier for implementing a MAC unit. As a result, the carry saving adder used to create the MAC unit is beneficial for low power applications but not for those where area on chip is a critical limitation.

Mehdi Modarressi et.al [3] proposed that Low-power Arithmetic Unit for DSP Applications using an application-specific result-cache that aims to reduce power consumption and some fixed point and floating-point arithmetic operations and trigonometric functions that have lengthy latencies and high power consumption.

III. Existing Work

In previous, there used approximate hybrid Wallace tree multiplier and Karatsuba multiplier. There both are compared based upon area, power and delay. There used approximate arithmetic operation to reduce power consumption and delay time. And there used 8 bit multipliers. And then, those multiplier is used in Image Processing Application and found that those multiplier gives similar results as their gives. Those are implemented using verilog language using vivado software.

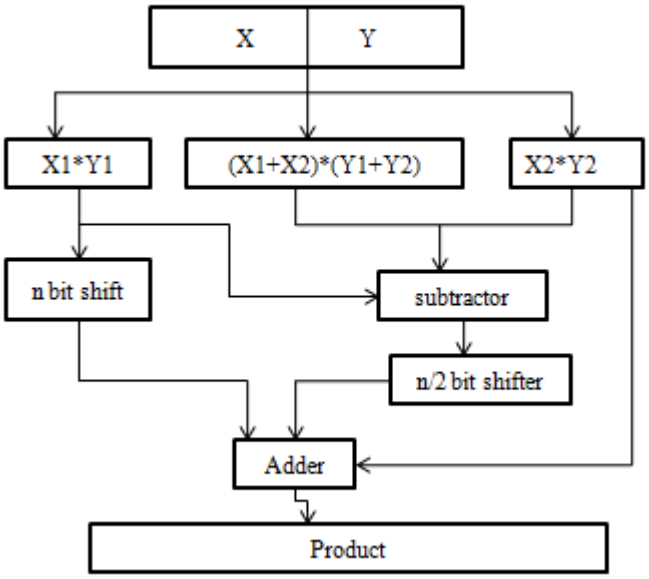

Figure 3.0 Block Diagram of Karatsuba Multiplier

3.1 Equations

We can multiply two numbers with less temporal complexity by using Divide and Conquer. We split the numbers into two equal halves.
Let X and Y be the supplied numbers.
Where X1 = 56, X2 = 78, Y1 = 12 and Y2 = 34, we have X = 5678 and Y = 1234.

Step1: X1*Y1 = 56*12 = 672 ……. eq (1)

Step2: X2*Y2 = 78*34 = 2652 ……. eq (2)

Step3: (X1+X2)(Y1+Y2) = (56+78)(12+34) = 6164 ……. eq(3)

Step4: eq (3-2-1) = 6164-2652-672 = 2840 ……. eq (4)

Step5: S1*X2^n+s4*(X2^n/2)+s2 = 7006652 ……. eq (5)

The complexity of multiplication is reduced from O (n^2) of traditional grade school multiplication to O (n^1.6) of faster multiplication using Karatsuba method. This result in reduced computation time to achieve large n digit by n digit multiplication. Recursive Algorithm is an algorithm or method that means it repeats itself.
In Karatsuba multiplication, you can multiply the numbers 17 times faster than normal traditional multiplication.
Thus, in existing method there have produced more power consumption and area utilization is also high.

3.2 Simulation Results for Existing Work

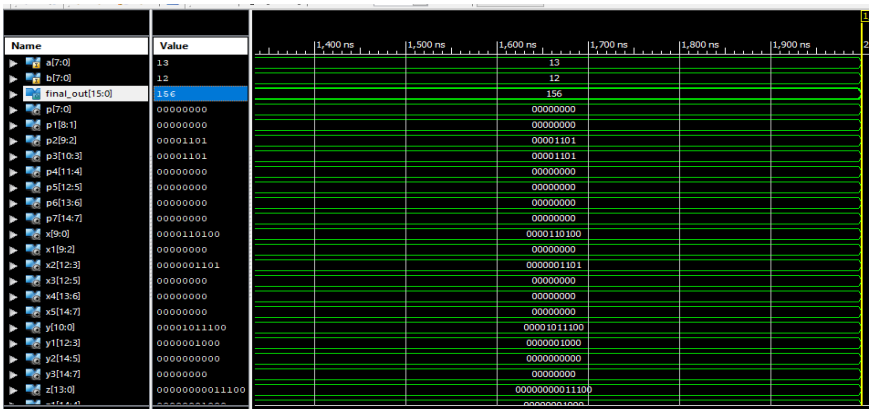

Figure 3.2.1 Output Waveform of Wallace Tree Multiplier

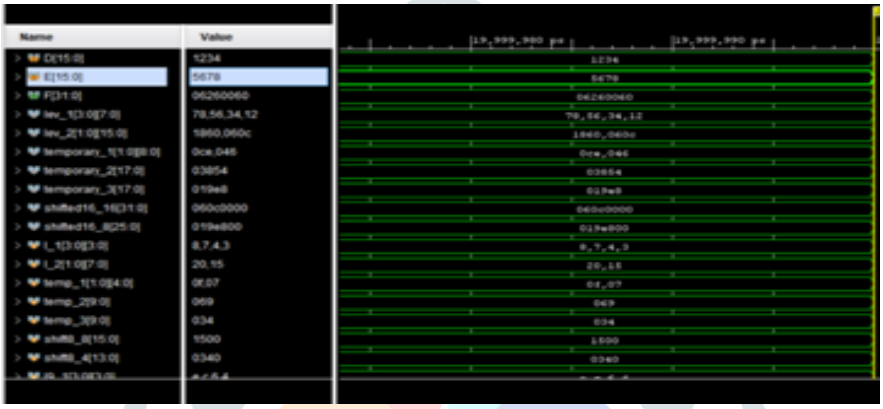

Figure 3.2.2 Output Waveform of Karatsuba Multiplier

. IV. Proposed Work

MAC unit performs multiplication and accumulation process. Multiplier, Adder, and Accumulator make up the fundamental MAC unit. Multiplier and adder blocks are used to implement MAC units in a feedback manner.. The multiply-accumulate unit calculates the product of two numbers multiplied together and adds it to an accumulator. The MAC unit is made up of a multiplier, adder, and accumulator register that stores the outcome when it is clocked. By using Karatsuba Multiplier and Brent Kung adder and Parallel In Parallel Out shift register the MAC operation is occurred.

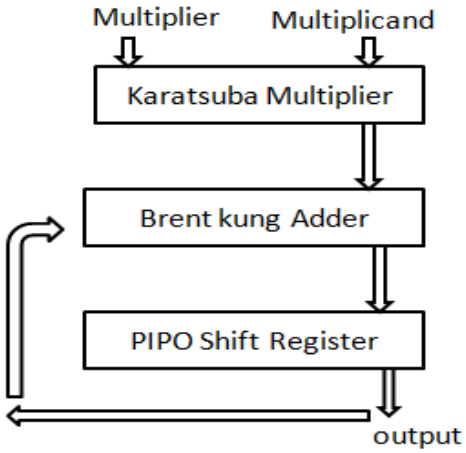

Figure 4.0 Block Diagram of MAC

The output of the multiplier is added to the register every clock by feeding it back into Brent Kung adder's inputs.

4.1 Introduction of Software

Here, I used Xilinx Vivado 2019.1 Version software. It is used to design, synthesize, simulate, test and verify digital circuit design.
The following are selected options for designing and analysis of our results.

- Product category: all
- Family: Artix-7
- Part: xc7a200tffg1156
- Target language: Verilog.

By using this tool I analyzed various parameters like device utilization, power report and delay report for various multipliers.

V. Simulation Results

5.1 Schematic Diagram

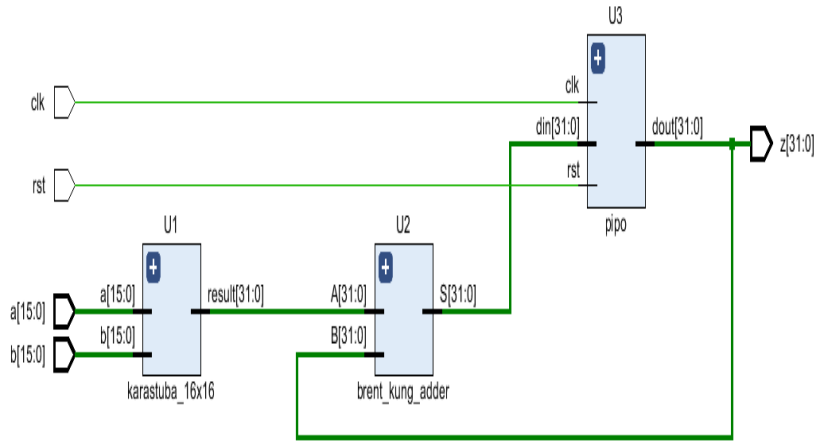

Figure 5.1.1 Schematic diagram

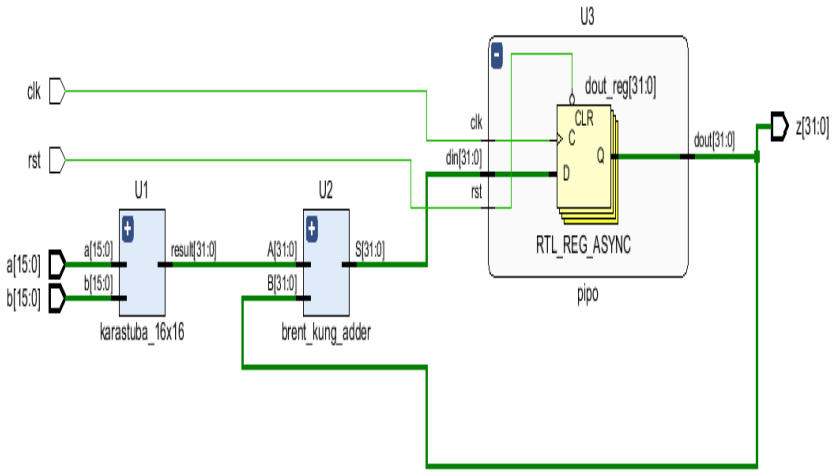

Figure 5.1.2 RTL Schematic diagram

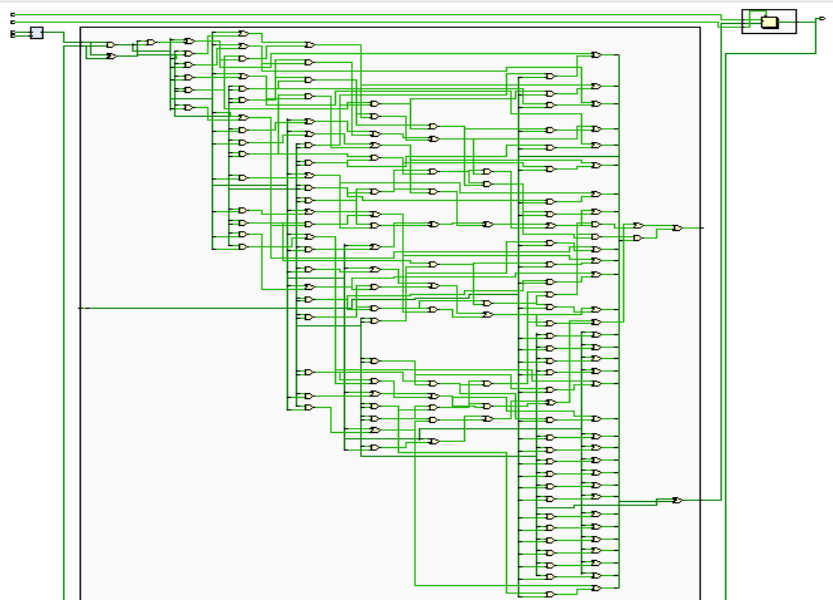

Figure 5.1.3 Technology Schematic diagram Extraction

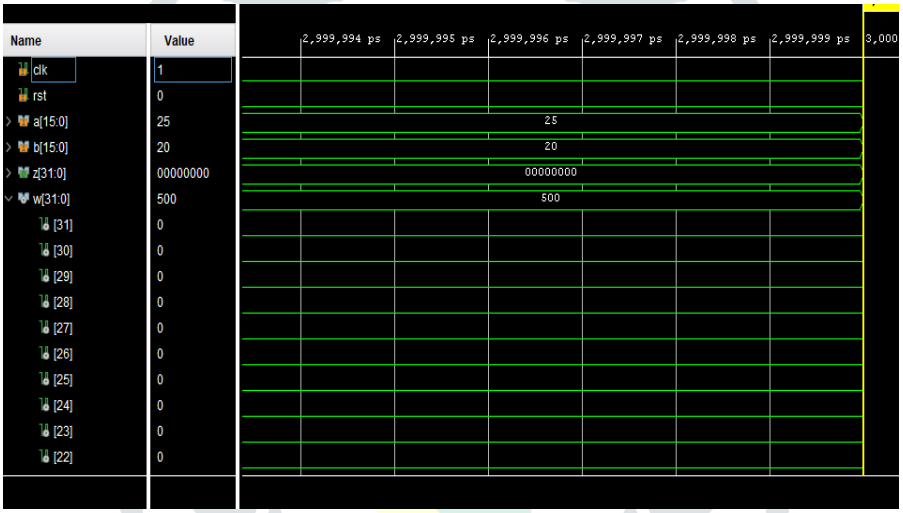

Figure 5.1.4 Output waveform of MAC

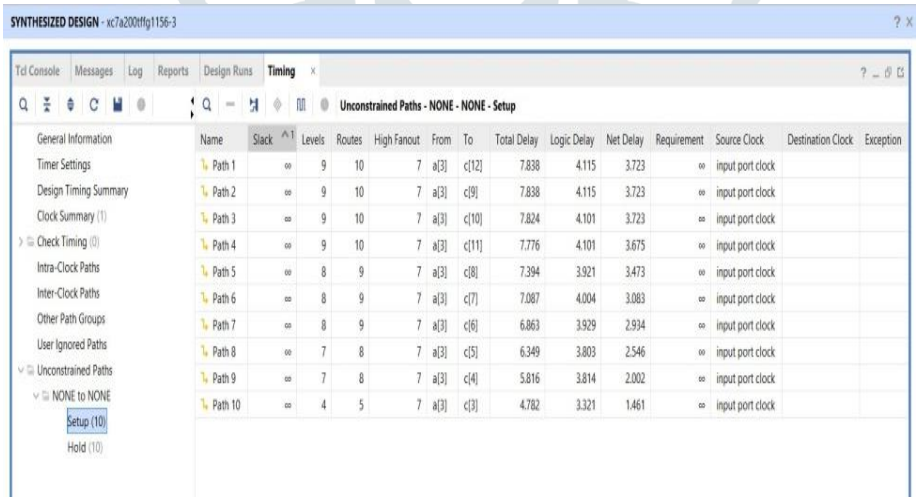

Figure 5.1.5 Delay Report

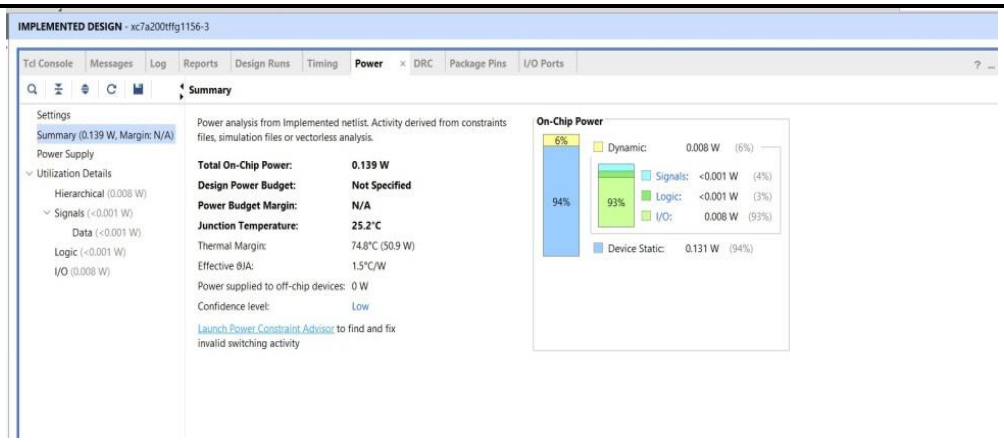

Figure 5.1.6 Power Report

5.2 Comparison Result

Results Summary of Optimized Mac Unit

Optimized MAC unit	Delay Total delay(ns)	Area(LUT's)	Power(mw)
16 bit Wallace Tree Multiplier	3.059	6133	2.43
16 bit Karatsuba Multiplier	1.887	6356	0.167

Table 5.2 Comparison table for different optimized MAC unit

VI. CONCLUSION

In this work a deep analysis has been performed on different types of multipliers like Karatsuba multiplier and Wallace tree Multiplier with Brent Kung adder and Parallel-in, Parallel-out Shift Register. It Says that Karatsuba multiplier is a fast multiplication Algorithm that gives better outcomes in comparison to Wallace Tree multipliers. So we have used this multiplier and designed 16-Bit multiplier using Karatsuba multiplication approach and placed it in the 32-bit Brent Kung Adder. After this we have synthesized and simulated this MAC unit to get reliability on our designed module. By seeing the comparison table, we can conclude that optimized MAC unit using 16 bit Karatsuba multiplier has low power consumption and less delay and area utilization is also less. Thus, by using Karatsuba algorithm it works on fast for large numbers.

VII. Future Studies

In Further, these multipliers are implemented with 32 bits and also used an application of image processing.

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