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HIGH SPEED VLSI ARCHITECTURE OF MAC VEDIC MULTIPLIER USING REVERSIBLE LOGIC

Subtitle: FPGA IMPLEMENTATION OF MULTIPLIER ACCUMULATOR UNIT USING VEDIC MULTIPLIER AND REVERSIBLE GATES

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ABSTRACT

The Multiplier-Accumulator (MAC) module may be built with the help of the Vedic multiplier and reversible logic gates. Specifically, the Vedic multiplier is constructed with the help of the recently discovered sutra Urdhava Triyagbhayam. How well a MAC works depends on the multiplier and adder units. An efficient multiplier and adder may be built with the use of reversible gates. Improved performance, smaller size, and fewer partial products can all be achieved by employing a Vedic multiplier. Due to its faster operation and reduced energy use, reversible computing is now trending up in the computer world. With an RCA-based DKG adder and a CSLA-based DKG adder, we showed off an 8, 16, 32, and 64-bit Vedic multiplier. Included in this group is the recently suggested DKG gate adder. CSLA claims that its operation is lightning quick. Carry select adder (CSA) vs. ripple carry adder (RCA) (CSA). Finally, the speed of operation of the proposed CSLA-based DKG gate with a Vedic multiplier-fast adder has been shown. The FPGA vertex7 board receives the results of the simulation and synthesis managed by Xilinx ISE14.7.

Key words : MAC unit ,vedic Urdhava Triyagbhayam algorithm,DKG reversible gate and CSLA structure.

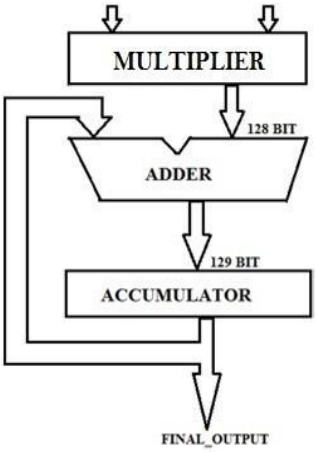
1.INTRODUCTION

MAC units are anticipated to be used in many applications in digital signal processing (DSP) that need multiplications and accumulations. It is also used in ultra-fast digital signal processing systems. Convolution, filtering, and the production of inner products are only some of the many uses for digital signal processing. Nonlinear functions are frequently used in DSP methods, such as the discrete cosine transform (DCT) and the discrete wavelet transform (DWT). Due to the fact that most arithmetic computations consist of cyclic addition and multiplication, their total speed is determined by the speed of execution and the overall performance of the calculation.

Multiplication and accumulation are two of the special features of digital filters. The MAC component then processes each data item separately from the CPU to relieve strain on the latter. High-speed filtering and additional processing power for DSP applications are also made possible by this essential MAC unit function. The optical communication system is one of the most impressive uses of the DSP because of the massive amounts of digital data it must analyse swiftly. Moreover, the Fast Fourier Transform requires the use of addition and multiplication (FFT). Since the 64-bit MAC unit is capable of processing a great number of bits, it necessitates more memory. It's made up of a multiplier and an accumulator that adds up all the product phrases that have come before. The inputs for the MAC unit come from the multiplier block's associated memory location.

2.LITERATURE VIEW

Implementation of a Modified High-Speed Vedic Multiplier, by Vijay Kumar Reddy The modified binary vedic multiplier utilised in the research project is described utilising vedic sutras from conventional vedic mathematics. It adjusts the initially-created Vedic multiplier. The updated binary vedic multiplier is proposed due to its decreased device use and delay time. The suggested method was conceived and implemented using Verilog HDL, with the Modelsim tool used for HDL simulation and Xilinx for circuit synthesis. Simulating the multiplication process using four bits, eight bits, and sixteen bits. The only simulation results displayed are those for the 16-bit binary vedic multiplier approach. This modified multiplication strategy is scaled up for greater dimensions. The results of this method of multiplication are compared to those of other ancient Vedic multipliers. Fast Speculative Multipliers from a Carry-Save Tree, by A. Cilardo et al. Approximation computing is a technique for increasing the efficiency of digital circuitry by forgoing precision while doing computations. The MAC (multiply and accumulate) unit estimate is provided in this research. The MAC partial product terms are compressed using basic OR gates as approximation counters, and some of the columns of the partial product terms are deleted to further preserve energy. To reduce the approximation error as a whole, the proposed MAC incorporates a compensation interval. More than 60% power reductions are achieved while maintaining acceptable picture quality by conceptualising and implementing a MAC unit specifically tailored to execute 2D convolution in TSMC 40nm technology in four distinct configurations.



3.IMPLEMENTATION OF A MAC BY64 X 64 VEDIC MULTIPLIER USING DKG ADDERS

MAC OPERATION

In addition to its importance in digital signal processing and multimedia information processing, the MAC function also has a wide variety of other practical uses. The MAC [12] consists of a multiplier, an adder, and a register/accumulator, as was previously stated. In this case, the Vedic multiplier was used. The input source for the MAC is the address in memory that maps to the multiplier block. This helps 64-bit DSP systems. It is possible to link the 64-bit memory address's input. After processing a 64-bit input, the multiplier returns 128-bit data. The output of any adder can be this 128-bit information. We use the Carry Save Adder, the Kogge Stone Adder, and the New DKG Gate in this case. The superiority of the DKG adder has been shown.

Specifically, the following equation describes the MAC unit function:

$$F = \sum P_i Q_i$$

The output of the adder unit is 129 bits since the carry is an extra bit. The appropriate output information is linked to the accumulator register. Parallel in parallel out (PIPO) register technique is used by the accumulator register. Because of the large size of the bits, PIPO is so named because both the input and output bits are generated in parallel. It also generates the output values for the adder at the same time. Any of the inputs can send the accumulator register's output to the matching adder. An elementary block diagram of the MAC subsystem is shown in Figure 1.

Fig. 1. MAC – Basic building block diagram

DKG gate

The DKG adder is designed exclusively with backwards-compatibility in mind. The inputs and outputs from two of the four possible sources are ignored. A total of four inputs and four outputs may be found. For a complete adder and subtractor, choose the DKG gate with the "A" input. The circuit operates as a reversible Full adder when A=0 and as a reversible Full subtracter when A=1. The reversible DKG gate's logic circuit is shown in Figure 5.

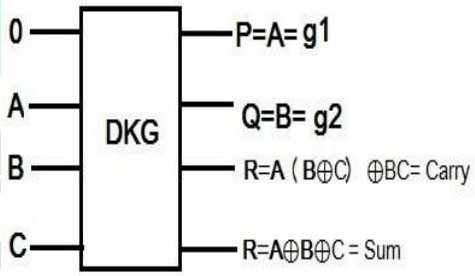


Fig. 2. DKG logic Gate

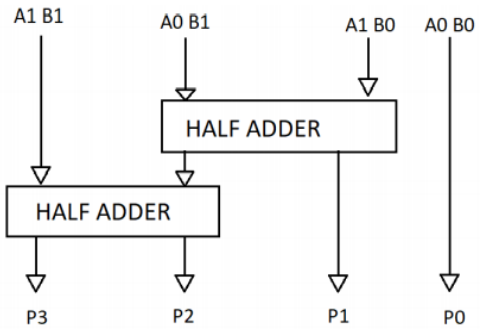


Fig3: 2x2Vedic multiplier

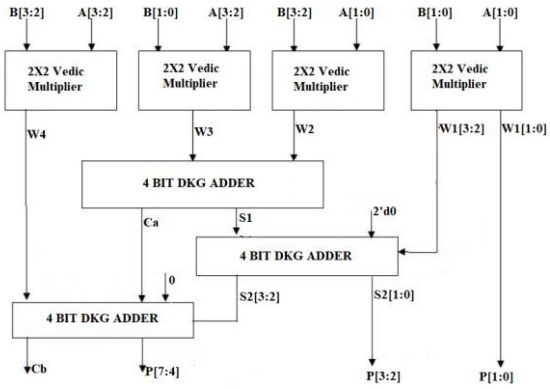


Fig4 : 4 Bit vedic multiplier

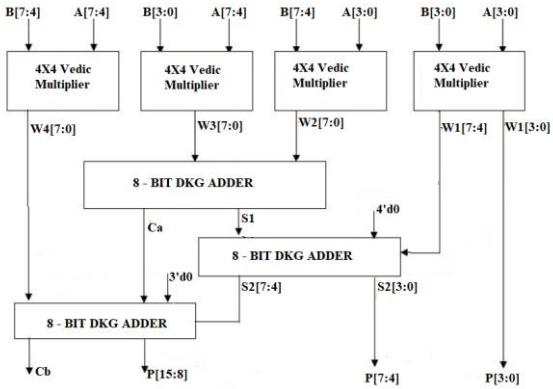


Fig 5: 8 Bit vedic multiplier

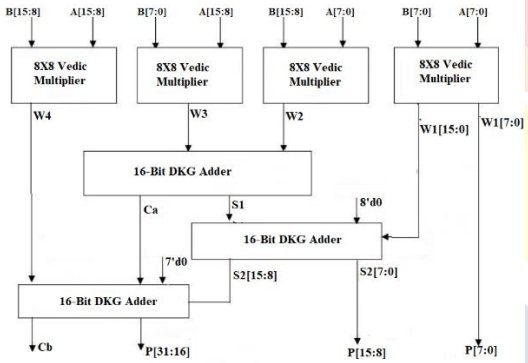


Fig 6: 16 Bit vedic multiplier

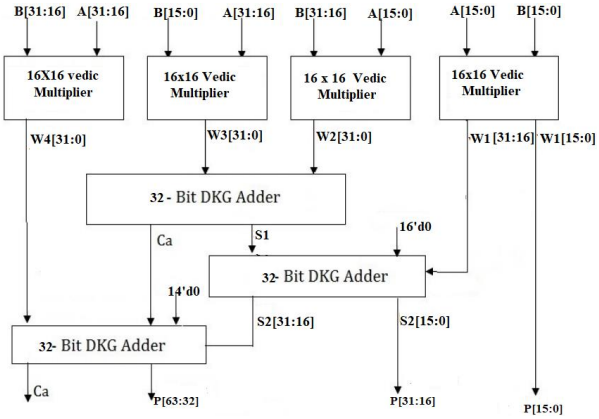


Fig 7: 32 Bit vedic multiplier

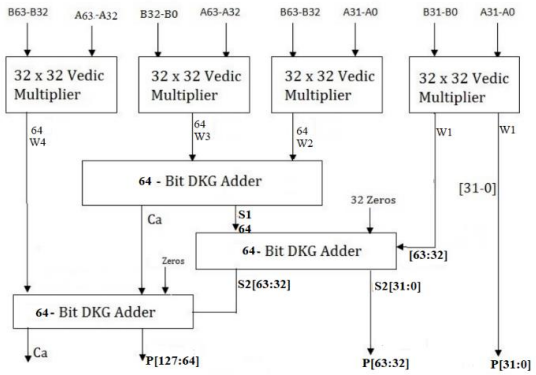


Fig. 8. 64-bit Vedic multiplier using DKG adder

In Figure 8, we see a DKG gate used in a 64-bit Vedic multiplier. If you're looking to put into practise the Vedic multiplier, the hierarchical approach is much easier to work with than the previously discussed architecture. In order to construct a 64-bit Vedic multiplier [8], a lower-level 32-bit multiplier is required. Multipliers of 16, 8, 4, and 2 bits are used in this scheme as well. As a result, preserving the adaptability of the multiplicative Design while greatly increasing it is a breeze. The suggested 64-bit operation's essential logic is easily split in two 32-bit pieces. Second-stage data is used as input for the first stage, and third-stage data is used as input for the last step, with the two halves of the data being swapped between the two processes. The intermediate adder stage is also required for this architecture. The adder stage is built from the ground up using the one-of-a-kind reversible DKG logic gate. In transverse mode, there are two inputs designated as A and B, with a 64-bit input and a 128-bit maximum output. Registers are used to store the 64-bit sum of the inputs. If the next phase includes carry, it is OK. The overall number of bits used in the addition process can be balanced by utilising zeros as one of the adder stage's inputs. That's the only way to guarantee the accuracy of these sums. We

need to fix three DKG stages before we can look at the 64-bit multiplier's design. The output total is received at the end of the adder, and the carry is formed during the last step. From the first stage of the multiplier, the LSB sum bits may be recovered. A 32-bit multiplier and a 64-bit multiplier are functionally and structurally equivalent, with the only difference being the number of input bits required.

Invention of the 4-bit DKG adder can be credited to Carry Select Adder. Two ripple carry adders, a multiplexer, and other parts make up the carry-select adder. When using a carry-select adder, the addition of two n-bit values is performed twice: once assuming the carry-in is zero, and once if it is one (and hence two ripple carry adders). The multiplexer is then used to select the correct carry-in, sum, and carry-out values once the two calculations have been made.

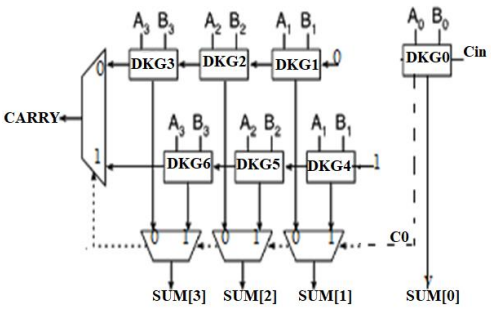


Fig9 : 4BIT DKG ADDER

4.RESULTS

RTL SCHEMATIC:- The register transfer level, abbreviated RTL, is the architecture's blueprint. It is used to contrast the proposed structure with the yet-to-be-developed ideal architecture. Using the coding language known as verilog or vhdl, the hdl language is used to transform an architecture's description or summary into a functional summary. Internal connection blocks are also described in the RTL schematic for convenience of understanding. The following graphic depicts the RTL schematic diagram for the proposed design.

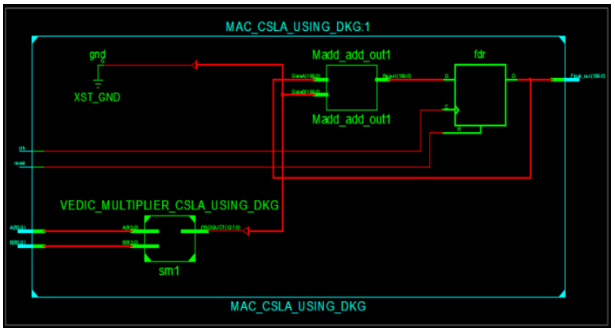


Fig10: RTL Schematic of MAC

TECHNOLOGY SCHEMATIC: - The technology schematic creates an image of the architecture in LUT format, which is utilised as an area parameter in VLSI to estimate the architecture's design. In the FPGA's LUTs, the memory allocation of the code is represented as a square unit.

Fig 11:View Technology Schematic of MAC

SIMULATION:-

The simulation is the process, while the schematic evaluates the linkages and building components. When the tool transitions from implantation to simulation, the simulation window opens on the home screen. The simulation window displays the outcomes as wave formations. In this instance, it is adaptable enough to handle many radix number systems.

Fig 12:Simulated Waveforms of MAC

PARAMETERS:-

VLSI takes into account three factors: area, latency, and power; using these variables, it is possible to compare one design to another. Here, geographical and latency considerations are taken

into account. The parameter is retrieved using XILINX 14.7, and verilog is the HDL language.

Parameter	MAC using RCA based DKG Adder	MAC using CSLA based DKG Adder
No of LUTs	11507	10830
Delay (ns)	56.232	37.814

Table1 :parameter comparison table

GRAPH:-

The graph provides a visual representation of the data that enables estimation comparisons. This graph compares the area and latency of two designs.

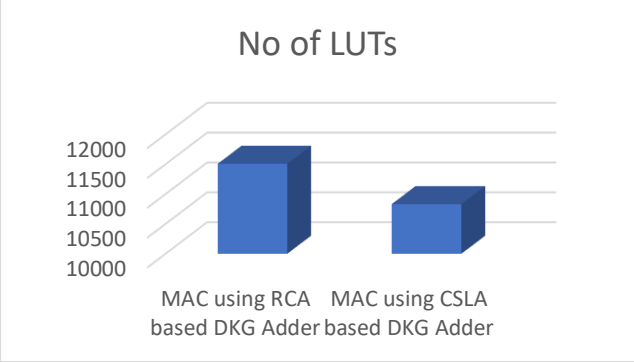


Fig 13:No of LUTs comparison Bargraph

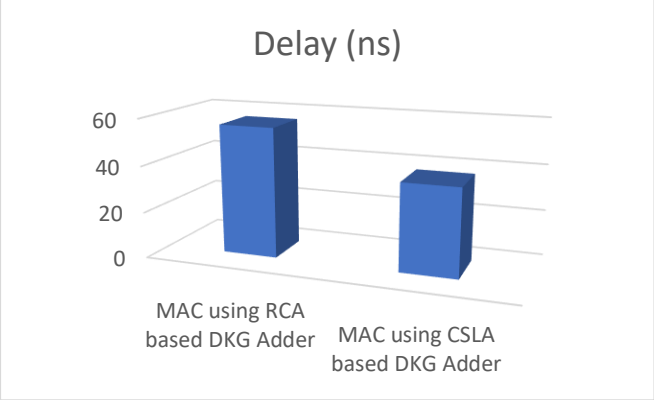


Fig14 :Delay comparison Bargraph

CONCLUSIONS

The proposed DKG adder gate design achieves respectable performance with the use of a Vedic multiplier and reversible computing. The proposed 64-bit MAC unit uses DKG reversible circuitry to implement a Vedic multiplier with RCA and CSLA. The design has been proven to be fully delay-optimized. We built and thoroughly tested the whole 64-bit MAC architecture for all currently-used building pieces. Based on the results of Table 1, we can infer that the Urdhava Triyagbhayam sutra has the quickest latency times thanks to its use of a 64-bit MAC Unit and a reversible logic method. The simulation and synthesis workflow is optimised with Xilinx ISE 14.7. The cornerstones of any building's design are where the focus should be. The core components of the MAC design we propose are a multiplier and an adder. Our proposed design for these structural elements is likely to be replaced in the future by one that is far more efficient. It drastically lessens MAC's latency overall.

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