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Review of CMOS Reversible Gates Logic for Low Power and Delay FPGA Application

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Abstract : Reversible logic computation is one of the most essential promising technologies in designing low-power digital circuits, optical information processing, quantum dot cellular automata, fault tolerant system and nanotechnology. In fact, the conventional digital circuits dissipate a significant amount of energy because several bits of information are deleted during the treatments. In reversible computation, the information bits are not lost. This paper presents the study of reversible realization of adder-subtractor circuit.

IndexTerms – Digital, Reversible, Realization, Adder, Subtractor.

I. Introduction

Reversible computation is a heavily investigated emerging technology due to its promising characteristics in low-power design, its application in quantum computations, and several further application areas. The currently established functional synthesis flow for reversible circuits is composed of two distinct steps. First, an embedding process is conducted which makes nonunique output patterns distinguishable by adding further variables. Then, this function is passed to a synthesis method which eventually yields a reversible circuit. However, the separate consideration of the embedding and synthesis tasks leads to significant drawbacks. In fact, embedding is not necessarily conducted in a fashion which is suited for the following synthesis process. In addition, embedding adds further variables to the function to be synthesized which exponentially increases its corresponding representation in the worst case.

An important component of quantum processing is reversibility, since advancement of a quantum framework is portrayed by a unitary operator and thus it is reversible. Quantum cost is another important factor of any reversible circuit. The most minimal quantum cost demonstrates the least cost of reversible circuit. By most reduced quantum cost can make a quantum PC. In this paper we tell the best way to locate the most minimal quantum cost and demonstrate a progressed Toffoli Gate that contains least quantum cost Quantum cost, the cost of a circuit, alludes to the general costs, relating to the utilization of Reversible Logic Gates for incorporating a given logical capacity, brought about in structuring of the circuit regarding the cost of the crude Reversible Logic Gates utilized. The quantum cost of the circuit is controlled by computing the definitely realized cost of the crude gates required for understanding the Number juggling and Logic circuit units. Some work presents 3*3 reversible gate to be specific Progressed Toffoli gate, that is, it has 3-input lines and 3-output lines. The fundamental alluring component of this gate is quantum cost. It has a 3 quantum cost which is less than 5 quantum cost. It works under certain conditions and application might be same as customary traditional Toffoli gate.

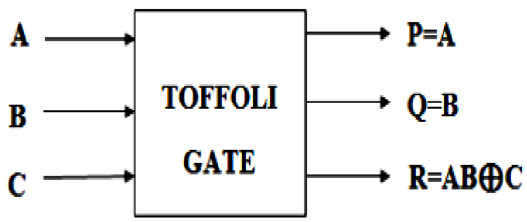

Figure 1: Toffoli Gate

Low power proficient digital gadgets are focus of specialists as of late. This point pulled in scientists to concentrate on the reversible digital circuit configuration approach. In perfect circumstances reversible circuits create zero power misfortune with improved performance. Reversible circuit configuration approach is progressively connected in the territory of DNA registering, low power CMOS plan, nanotechnology, quantum figuring and optical processing and so forth.

II. LITERATURE SURVEY

S. Majumder et al., [1] present, circuits with low power and less computation time are in high demand in VLSI technology. In this context, the applications of reversible logic are far-reaching. In this paper, the detailed evaluation of certain reversible gates, namely, Feynman gate, Peres Gate, Modified Fredkin Gate, Modified Toffoli Gate, and TS Gate is set forth. Evaluation comprises of transistor implementation, simulation results and average power and delay measurement. The utilization of TSG to form a completely reversible full adder has also been evaluated in details. The implementations are completely reversible in nature and finds their applications in circuits with low power and high speed which are suitable to implement in silicon.

M. Awais, et al., [2] Reversible logic is an emerging digital design paradigm which promises low energy dissipation; thanks to its information-lossless nature. True potential of this exciting concept can only be assessed by facing the design of practical complexity applications. Low density parity check (LDPC) decoding is one such application from forward error correction domain. The core of LDPC decoding is the check node (CN) processor, which executes the decoding algorithm and constitutes a major portion of decoder's overall power consumption. This work proposes a low-power LDPC CN architecture using reversible logic gates. Transistor level design and full custom layout of proposed architecture is carried out on UMC 90nm90nm complementary metal–oxide–semiconductor technology. All reversible blocks of proposed CN are optimised for quantum cost, garbage outputs and transistor count.

C. Bandyopadhyay et al., [3] reversible logic synthesis is one of the best suited ways which act as the intermediate step for synthesising Boolean functions on quantum technologies. For a given Boolean function, there are multiple possible intermediate representations (IRs), based on functional abstraction, e.g. truth table, decision diagrams or circuit abstraction, e.g. binary decision diagram (BDD), and-inverter graph (AIG) and majority inverter graph (MIG). These IRs play an important role in building circuits as the choice of an IR directly impacts on cost parameters of the design. In the authors' work, they are analysing the effects of different graph-based IRs (BDD, AIG and MIG) and their usability in making efficient circuit realisations. Although applications of BDDs as an IR to represent large functions has already been studied, here they are demonstrating a synthesis scheme by taking AIG and MIG as IRs and making a comprehensive comparative analysis over all these three graph-based IRs. In experimental evaluation, it is being observed that for small functions BDD gives more compact circuits than the other two IRs but when the input size increases, then MIG as IR makes substantial improvements in cost parameters as compared with BDD by reducing quantum cost by 39% on an average. Along with the experimental results, a detailed analysis over the different IRs is also included to find their easiness in designing circuits.

M. Soeken et al., [4] present a synthesis framework to map logic networks into quantum circuits for quantum computing. The synthesis framework is based on lookup-table (LUT) networks, which play a key role in conventional logic synthesis. Establishing a connection between LUTs in an LUT network and reversible single-target gates in a reversible network allows us to bridge conventional logic synthesis with logic synthesis for quantum computing, despite several fundamental differences. it is call our synthesis framework LUT-based hierarchical reversible logic synthesis (LHRS). Input to LHRS is a classical logic network representing an arbitrary Boolean combinational operation; output is a quantum network (realized in terms of Clifford+T gates).

V. Shukla et. al., [5] work presents two structure approaches for reversible acknowledgment of 8-bit adder-subtractor circuit with enhanced quantum cost. These plans are contrasted and existing structures on some selected performance parameters, for example, all out number of reversible gates, garbage outputs and quantum cost. The proposed plan for 8-bit adder-subtractor circuit utilizing reversible methodology reproduced utilizing Modelsim apparatus and blended for Xilinx Straightforward 3E with Gadget XC3S500E with 200 MHz frequency. This advanced circuit might be used further for the structuring of low power figuring gadgets.

V. Shukla O. P. Singh et. al., [6] Number-crunching digital handling sub-frameworks are considered as one of the major segment of any electronic processing framework. The adder/subtractor circuit is one of the imperative piece of registering frameworks, for example, number juggling logic unit of any PC. Moreover, inclination of productive low misfortune preparing gadgets are the essential need of the time. This need is the essential inspiration for analysts to advance in the field of reversible circuit configuration approach. Low power VLSI circuits, DNA registering, optical figuring, signal preparing, quantum processing and nanotechnology and so on are a portion of the dynamic fields with the use of the reversible logic ideas. In this work, it is have proposed a way to deal with plan n-bit adder/subtractor circuits with accessible reversible logic gates as it were.

K. Ghosh et. al., [7] Ternary quantum logic assumes an important job for structure fast and proficient advanced PCs. It has a few points of interest over old style processing and double quantum circuits. In this work, the acknowledgment of essential ternary circuits for adder/subtractor, encoder and priority encoder are proposed and structured. These circuits are fundamental for the development of different computational units of quantum PCs and other complex computational frameworks. Structure of reversible circuits can be improved by diminishing the quantum circuit cost. This work utilizes some rudimentary parts and run of the mill ternary gates (summed up ternary gate, M-S gate and so forth.) to perform number juggling expansion, subtraction and encoding tasks. At last, it assesses the ideal cost for each circuit.

M. Sangsefidi et. al., [8] Notwithstanding high mix thickness of QCA circuits, other one of a kind determinations, for example, rapid and low power utilization urge scientists to use this innovation rather than CMOS innovation. In this work, another format of XOR gate is introduced in QCA innovation, at that point, it is abused to plan a 8-bit controllable inverter. At last, utilizing the proposed structure and last adder circuit given independent from anyone else in our past work, a 8-bit adder/subtract or is planned. It is the most important segment of an ALU. All the structured circuits have utilized coplanar clock-zone based hybrid. The most noticeable qualities of planned circuits incorporate extremely high activity speed, low multifaceted nature, little region, totally coplanar structure, and likewise keeping away from turned cells in us plans for Evasion of Development Difficulties QCA Circuits.

R. Bardhan et. al., [9] propose a productive adder/subtractor circuit utilizing QCA 3-dot cell. This model is very capable to register both expansion and subtraction tasks. it is additionally appeared here a solid subtractor circuit. Moreover, our new and novel plans has least number of QCA cells till now. The proposed structures carry out more recipient than the present ones, e.g., the proposed 32-bit subtractor circuit improves 73% on QCA cell, 99% on territory and the proposed 32-bit adder/subtractor circuit improves 90% on QCA cell, 99% on region than the current best known one.

N. J. Lisa et. al., [10] In this work, it is available an advanced plan for the quantum ternary adder/subtract or circuit. it is propose the structure of quantum Ternary Peres Gate (TPG). The structure of our proposed quantum ternary adder/subtract or circuit comprises of two sections: a) Right off the bat, it has the plan of a quantum ternary full-adder circuit utilizing the proposed TPG gates, and b) Besides, it structures the proposed adder/subtract or circuit by utilizing the built full-adder in an) and M-S gates. it is additionally propose a heuristic to structure a minimal ternary adder/subtract or circuit. Our circuits perform much superior to the current ones.

A. K. Chowdhury et. al., [11] lately, reversible calculation has gotten much consideration in the field of low power circuit structure. In this work, an irreversible IG-A gate is exhibited. The gate is additionally used to plan irreversible full adder/subtractor (IAS). Furthermore, IAS square is used to develop n-bit adder and subtractor. Proposed IAS configuration is examined and analyzed against the current reversible strategies. Highlights, for example, equipment cost, logic computation and gate check are investigated to demonstrate the proficiency of the plan. Transistor level structure and recreation of IG-A circuit are demonstrated utilizing Rhythm OrCAD Light. The one-bit IAS reenactment results are confirmed utilizing Altera Quartus II and ModelSim programming. Reproduction results demonstrate that the circuit offers decreased equipment unpredictability when contrasted with the current reversible full adder plan.

A. Rahman et. al., [12] IEEE 754 standard twofold accuracy (64-bit) paired skimming point number-crunching unit is regularly important in complex digital sign preparing applications. The essential tasks, gliding point expansion and subtraction, should be streamlined to effectively figure drifting point multiplier, divider and square root. Notwithstanding, the fundamental test is to plan the gliding point math unit equipment that utilizations less logical assets of FPGA and ASIC and has a most extreme working frequency with a less number of clock cycles. This work proposes another, productive equipment structure strategy for executing twofold exactness skimming point expansion and subtraction. The pipeline equipment configuration is actualized on Virtex-6 and Virtex-5 Xilinx FPGA.

III. CONVENTIONAL FULL ADDER CIRCUIT

The fundamental entity that needs to be created is the Full Adder. The purpose of this entity is to find the sum and carry when two 1-bit numbers are added. Though a full adder can be constructed in more than one way, the AND-OR-Invert (AOI) studied. This entity has three 1-bit inputs and two 1-bit outputs: *a* and *b* (the numbers to be added), *c_in* (the carry in, also added), *c_out* (the carry out), and *s* (the sum of *a*+*b*+*c_in*).

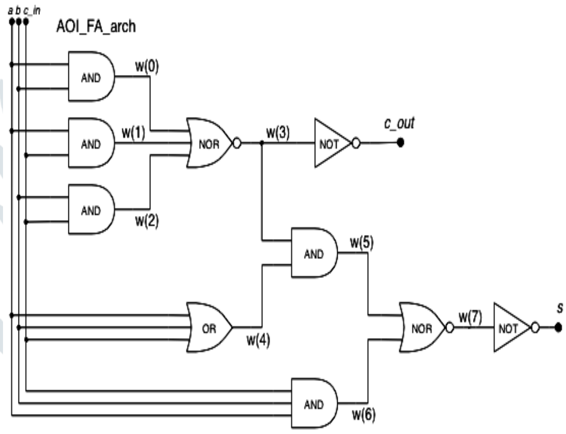

Figure 2: Full adder

Before proceeding further the terms carry and sum should be clearly defined, which can be best done through an example. Consider the addition of the following decimal numbers: 5+6. When adding this decimal number, we cannot correctly represent the number “11” in the 1s place, so we carry a 1 to the 10s place, leaving a sum of 1 in the ones place. An equivalent process occurs for binary. When adding 1+1 in binary, you cannot represent “2” in the 1s place, so you carry a 1 to the 2s place, leaving a sum of 0. This is the case with the full adder. The sum (*s*) represents the remainder of the total sum *a*+*b*+*c_in*, after a carry (*c_out*) has been made, if necessary. The purpose of the full adder then is to find the sum of two 1-bit numbers and a 1-bit carry in.

The AOI_FA entity was written using dataflow, joining inputs with Boolean operators such as “and”, “or” and “not.” There is more than one way to construct the AOI_FA using VHDL dataflow descriptions. This project described each gate individually, connecting the output of one gate to the input of another using a wire. Alternately the outputs *c_out* and *s* could have been described as a combination of operators in a longer concurrent statement, reducing the number of internal wires needed. This project chose to represent each gate individually to reduce possibility for error when writing a single long concurrent statement. The entity AOI_FA is shown in Figure 3.

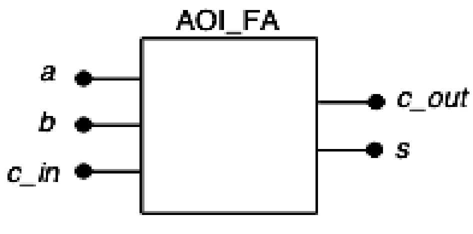

Figure 3: AOI_FA

After constructing the AOI_FA shown in Figure 4 using VHDL, we must test its function. Since there are three inputs to the entity, there are 2^3 unique combinations of inputs to test.

IV. CONCLUSION

Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nano-computing and optical computing. Reversible logic gates are widely known to be compatible with future computing technologies which virtually dissipate zero heat. This paper reviews of the reversible realization of adder-subtractor circuits. The lowest level entities, XOR_GATE and AOI_FA, were described using the dataflow method. These entities were combined together using the structural description method to make a 1-bit adder/subtractor, which was repeated and ultimately created the 8-bit adder/subtractor.

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