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A Comprehensive Study Of Design And Verification Of DDR SDRAM Controller Using Verilog

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Abstract : In the modern era of Advance science and technology today the performance of the memory is the main part of the computer system that needs to be improved. In computer applications including laptops, networking and DSP processing systems DDR SDRAM is frequently used. Memory controllers enable efficient data control between the processor and memory. Any design flow must include verification because it is finished before silicon development. It is carried out during the product development process to verify for quality and fix design bugs. A memory controller for Double Data rate synchronized dynamic random-access memory (DDR SDRAM) is designed in this work, and a coverage-driven constraint random verification environment is built for the designed memory controller. The DDR SDRAM controller do many tasks like refresh, initialization and timings that is unaware to the user. The use of appropriate commands, such as Read and Write accesses, appropriate active and pre-charge commands, etc is another goal in the design of DDR SDRAM controller. System Verilog is used for the verification while the code is written in Verilog HDL. Although the DDR SDRAM controller's core functions are the same as those of SDR (Single Data Rate) SDRAM, but the circuit design is different. DDR merely uses complex circuit techniques to achieve high speed. DDR SDRAM employs a double data rate design to increase the number of operations per clock cycle. Data is sent on both the rising and falling edges of the clock in DDR SDRAM, also referred to as DDR (Double Data Rate). The DDR controller is made with the intention of providing the correct commands for SDRAM start, read/write operations, routine refresh operations, appropriate active and pre-charge commands, etc. Verilog HDL is used to implement the DDR SDRAM controller, and ISim and Xilinx ISE Design suite 14.7 are used for simulation and synthesis, respectively.

IndexTerms **- DDR , SDRAM, Verilog, Memory Controller.**

I. INTRODUCTION

Memory performance is the key barrier preventing the computer system from achieving higher performance levels. The entire performance is greatly influenced by memory. Memory controllers regulate the flow of information between the processor and the memory. It connects several memory types to the CPU bus. It is a crucial component of a computer system that controls memory and is in charge of transferring data between the CPU and memory. The greatest quantity of memory that a computer system may use, the number of memory banks, the kind and speed of memory, the data depth and breadth of memory particles, and other crucial factors are all determined by a memory controller. It impacts the computer system's memory performance, which has a significant impact on the computer system's overall performance. We are aware that SDRAM, which is faster and more expensive, is employed in cache memory. While main memory uses DRAM. It is more affordable than SRAM and faster. Now, if we look at the different generations of dynamic RAM, we will notice an increase in speed as well as a decrease in power usage. The very first generation of DRAM was an asynchronous dynamic, meaning that the RAM and CPU clocks were not in sync. The problem that this type of RAM had was that the CPU did not know the specific timing at when the data from the RAM on this input output bus will be available. This problem has been resolved by the following generation of RAM, known as the synchronous DRAM. As a result, in the case of this SDRAM, the RAM and CPU clock are in sync. The advantage of using SDRAM right now is that the CPU, or more precisely, the memory controller, precisely knows when or how many cycles will pass before data is made available on the bus. As a result, the CPU doesn't have to wait for a memory access. And as a result, we can speed up memory read and write operations.

There are actually two different frequency types for RAM. I/O clock frequency comes first, followed by RAM internal clock frequency. The rate at which data is moved from the RAM to the memory control is known as the I/O clock frequency.The frequency that a RAM uses for its internal activities is known as the internal clock frequency of a RAM. The internal clock frequency and the I/O clock frequency for SDRAM are both 100 to 133 Mhz. Let's assume that if the bus is 64 bits wide and the clock frequency is 100 MHz, the data rate will be 800 Mb/s (100 MHz x 64 bits). Modules for SDRAM run at 3.3 volts. Due to the fact that data in SDRAM is only transferred at the rising edge of each clock cycle, it is also known as signal data rate SDRAM. However, the following generation of synchronous DRAM is referred to as DDR RAM because data is transferred twice during each clock cycle in this type of memory. both a positive and a negative edge.

DDR1 RAM is the abbreviation for the first DDR RAM generation. Voltage has been decreased from 3.3 v to 2.5 v in comparison to SDRAM. In the case of DDR RAM, data is transferred during both the rising and falling edges. Therefore, we may say that in a single clock cycle, two bits are being pre-fetched instead of one, which is known as two bits pre-fetching. Internal clock frequency and input

output bus clock frequency are both the same in this DDR1 RAM, which is typically operated between 133 Mhz and 200 Mhz. Data that the input output bus will double.

The data is doubled compared to the previous generation with DDR2 memory, which is operated at 1.8 volts and has an internal clock frequency that is the same as before. This is accomplished by increasing the amount of bits that are pre-fetched during each cycle. Therefore, in the case of DDR2 RAM, 4 bits are pre-fetched during each cycle as opposed to 2 bits, or, to put it simply, the internal bus of this RAM has been doubled. The internal clock frequency is doubled for I/O.

The voltage is further reduced for DDR3 to 1.5v. In comparison to the previous generation, the RAM's internal clock frequency is now better. In comparison to the second generation, RAM's internal data bus width has doubled. DDR4 operation voltage has been reduced to 1.2v. Again, here the number of bits that is being pre-fetched us same as the previous generation i.e 8 bits per cycle but the internal clock frequency of the RAM has been increased.

The CPU uses a physical address to access data that is kept in memory. However, the CPU delegated control of this operation to a separate circuit known as the memory controller, or MCC, rather than handling it directly (memory control chip). The read-in and write-up logic for data to the computer's main memory is contained in the MCC. The MCC is positioned on the main board within an inexpensive component called the northbridge in the design, but it is now included within the CPU. While the effects of the integration of the CPU are not limited to only one type of memory, this innovative design has significantly reduced memory latency. The memory controller is linked to the CPU through the addresses and the external data bus. The CPU requests data from the server when it needs it. The location of the necessary data, which is currently kept in DRAM, is contained in the MCC for this request. The information is located by the MCC, which is connected to DRAM by the multiplexer, and is then sent to the CPU. The memory controller's duties go beyond simple data reading and writing, for example. RAM is typically volatile memory; as a result, the memory controller frequently performs capacitive refreshment in order to maintain the data. A memory controller is present in Flash Memory, a RAM and ROM hybrid, although unlike RAM, Flash Memory does not require power to maintain data retention. As a result, the memory controller's only functions are to read and write data. Memory scrambling is a technique that we employ to control the user information before writing it into the user. It helps to prevent cold boot attacks. sensitive information is obtained directly from the memory module in these cases, making the memory controller essentially a middle man who assumes some of the CPU's duties in their place.

II. DESIGN OF DDR SDRAM CONTROLLER

DDR SDRAM controller receives Control signal and address from buses. The controller generates signal according to that signal data that is being read or write to specific part of memory location. The SDRAM controller block diagram and architecture is shown in below figure 1.

It has three modules:-

1. SDRAM main control block.
2. SDRAM signal generation block.
3. SDRAM data path block.

1. SDRAM Main Control Block : Two State machine, a refresh counter are present in the main control block. The two state machine are used for SDRAM initialization and for generating the SDRAM commands.In accordance with with the system interface control signals, they provide istate and cstate output.Now depending upon the istate and cstate the signal generation module generates the address and command signal.The read and write operations between the buses and DDR are handled by the data path module. Some of the key characteristics of the SDRAM controller includes the following:

- The controller simplifies the SDRAM read and write operation.
- Internally developed Independent state machine are used to initialized the SDRAM controller.
- The Read and write cycle Access time is optimized based on the SDRAM CAS latency and Burst Length
- The controller performs the DDR SDRAM auto refresh
- The primary or main control consist of three submodules.

The main control module contains a programmable 16-bit counter (finite state machine) that is utilised to carry out the auto refresh operation. The WRITEA, NOP, READA, PRECHARGE, REFRESH, and LOAD MODE signal commands are provided to the controller interface module after it receives the processor's commands and decodes them. In order to load the two registers REG1 and REG2 from address ADDR signals, the LOAD REG1 and LOAD REG2 signals must be decoded. The DDR SDRAM employs two distinct clock signals: CLK and CLK' (the positive edge of the clock is simply defined as the crossing of CLK going high and CLK' going low). The commands are taken down only on the positive edge of the clocks. The fundamental commands used to access the SDRAM memory are the two signals READ and WRITE. The DDR SDRAM will offer programmable READ/WRITE operations with burst lengths of 2, 4, or 8 locations. As soon as access to SDRAM is initiated at any place, it will continue until the burst length is reached. READ and WRITE signal operation is only started by activating signal commands. The figure 2 shows the finite state machine that makes up the controller Interface. The initial state is regarded as the ideal condition, and the controller can move between these states depending on the request from the processor that is PRECHARGE, REFRESH, LOAD MODE, or ACTIVATE.

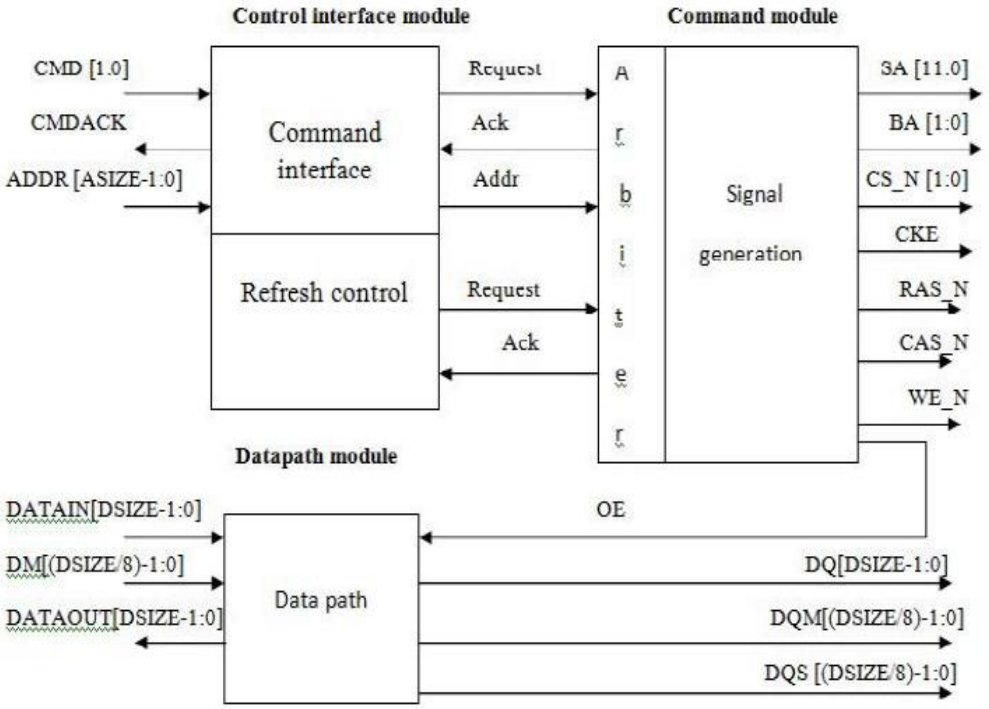

Fig 1. DDR SDRAM Memory Controller Block Diagram

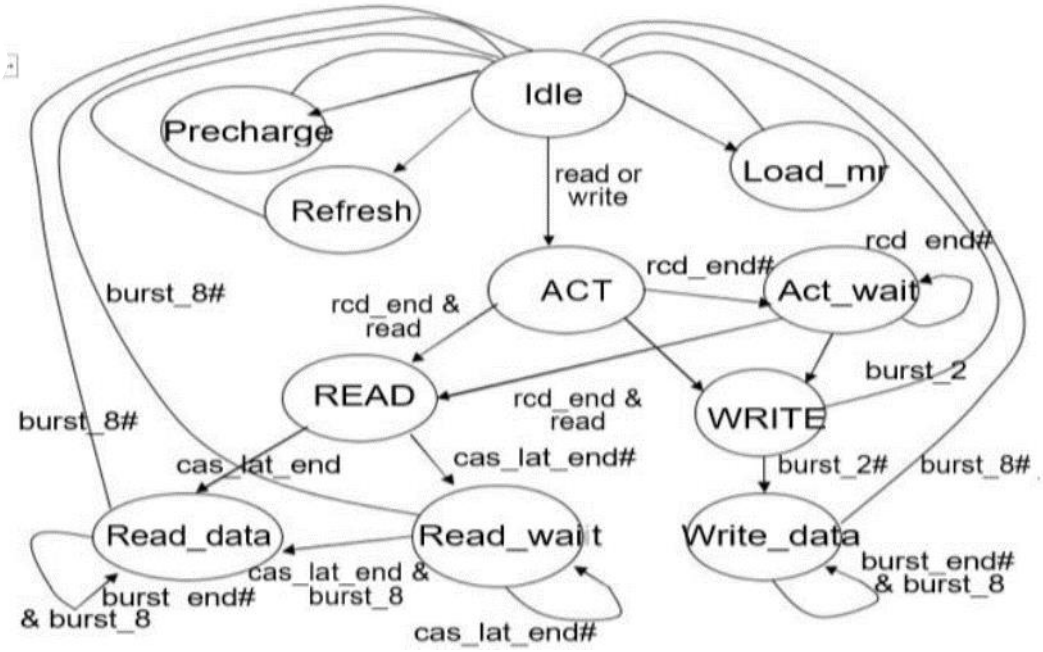

Fig 2. DDR SDRAM Finite state machine

2. SDRAM signal generation block : Three shift registers, an arbiter, and a multiplexer are present in the signal command block. When several requests originate from various devices, an arbitrator is used. High priority dev ices are given higher priority when both high priority and low priority devices need to transfer data at the same time. Until the high priority device has transferred all of its data, the low priority device cannot transfer any data. The operation of REFRESH control is given top importance in my work. Therefore, if the REFRESH operation is running when a command from the host arrives, the controller will first carry out the refresh operation before completing the command requests and holding the command acknowledgement (CMDACK). As soon as the refresh procedure is completed the command module will begin carrying out the requested commands from the hosts. Shift registers, a module inside a command module, are used to keep the timing between the command signals sent to the SDRAM memory controller. The multiplexer, which is utilised to multiplex the address, is another module that it contains. When the command signal ACTIVATE (RAS) is issued, the row address is multiplexed to SDRAM. During a signal READ (WRITE) instruction, another column component is likewise multiplexed with the address to SDRAM address outputs.

3. SDRAM Data Path Block : The purpose of a data path block is to store write data and compute the value for the read data path. Its primary functions are data production and data sampling for DDR. Data from the module data path is sampled during the READ operation. Data will be transmitted one word at a time, synchronizing with the clock signal. The user interface receives the data at a rate of one word per clock cycle when the WRITE operation is used. The module data path will resynchronize the data, and it will transmit at a speed known as DDR double data rate. The processor and memory were connected by the data path block, which served as an interface. Between

the host and Memory, the data path module carries out the two actions known as latching of the data and dispatching of the data. The tristate buffer on the module data path is managed by the OE signal from the module command. Any data that has to be written is received on the DATAIN pin during the WRITE operation, and data is delivered on the DATAOUT pin during the READA operation.

III. VERIFICATION OF DDR SDRAM CONTROLLER

In VLSI industry The most important component of the VLSI configuration stream is verification. In order to prevent it from turning out to be dangerous later on in the design process, it aims to find the problems in the RTL (Register Transfer Level) plan early on. During the verification process, distractions occur about 70% of the time. Prior to the production of the chip, verification aims to guarantee that the design's functionalities are accurate. RTL simulations are carried out to guarantee functionality. Bugs discovered at this level are fixed in the RTL, and debugging is simple. Any functional problems would be deadly and extremely expensive once the chip has been taped out. The verification step is regarded as a very important component of the design life cycle because any significant design flaws that are not found before manufacturing will necessitate the use of newer processing, raising the overall cost of the design process. Block diagram for verification environment and flow chart is shown below figure.

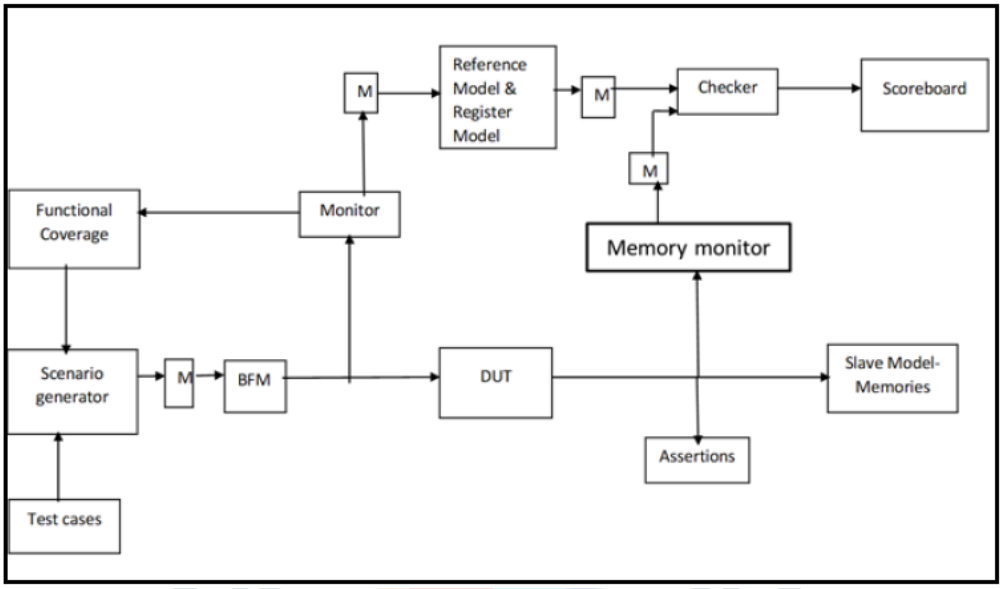

Fig 3. Verification Environment of memory controller

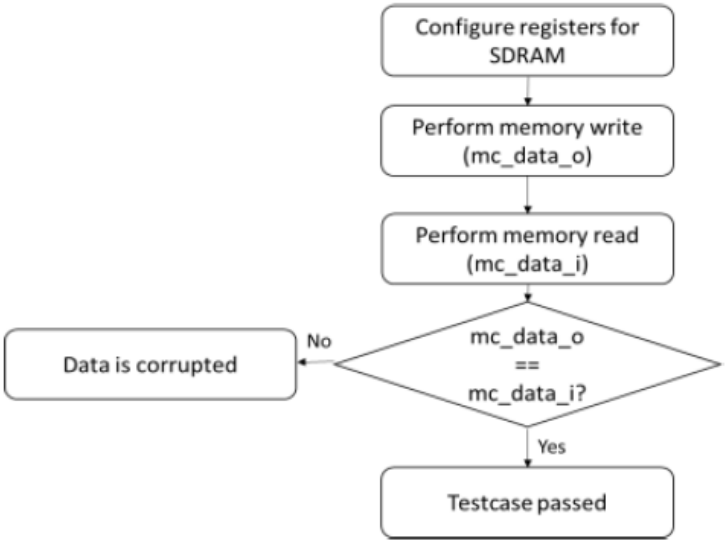

Fig 4 . DDR SDRAM flow chart of write-read testcase

IV. SIMULATION AND SYNTHESIS RESULT

After the designing of DDR SDRAM controller, the simulation and verification done using Xilinx ISE 14.7 and ISim simulation tool. We got the following observation.

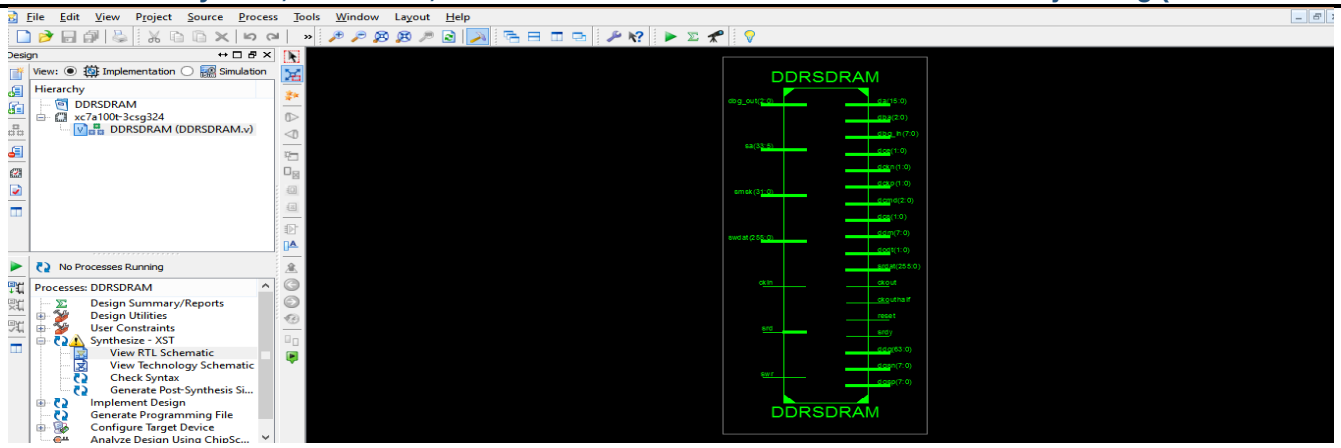

Fig 5. Top level view of Memory controller

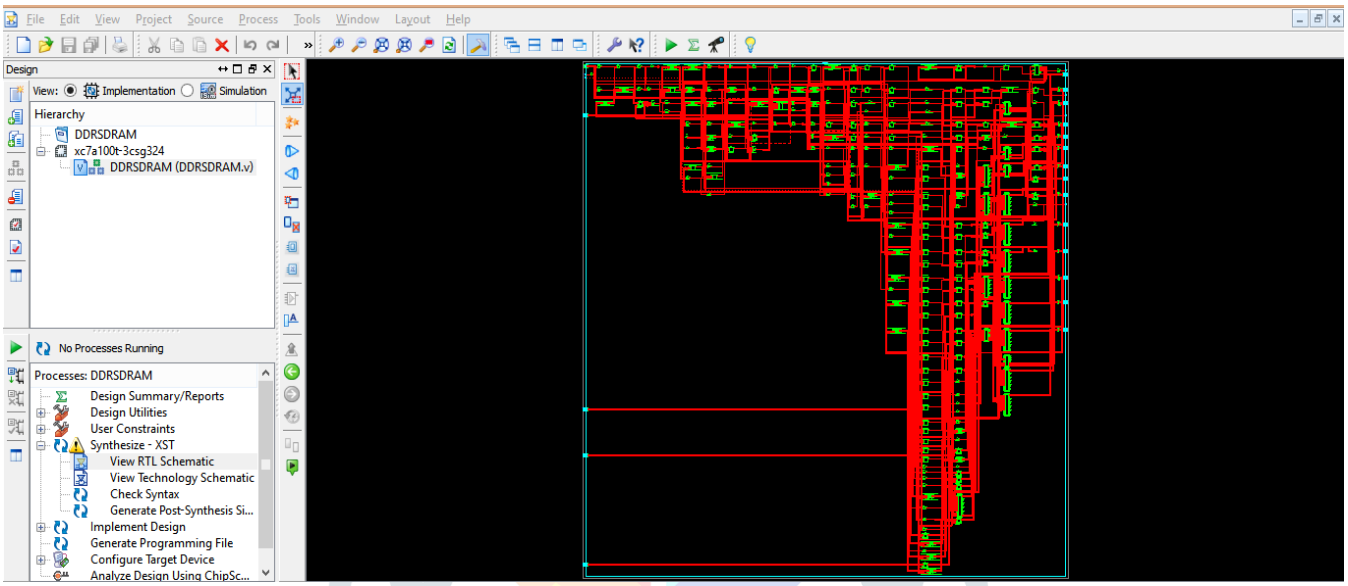

Fig 6. Internal view of DDR SDRAM Controller

Simulation result:

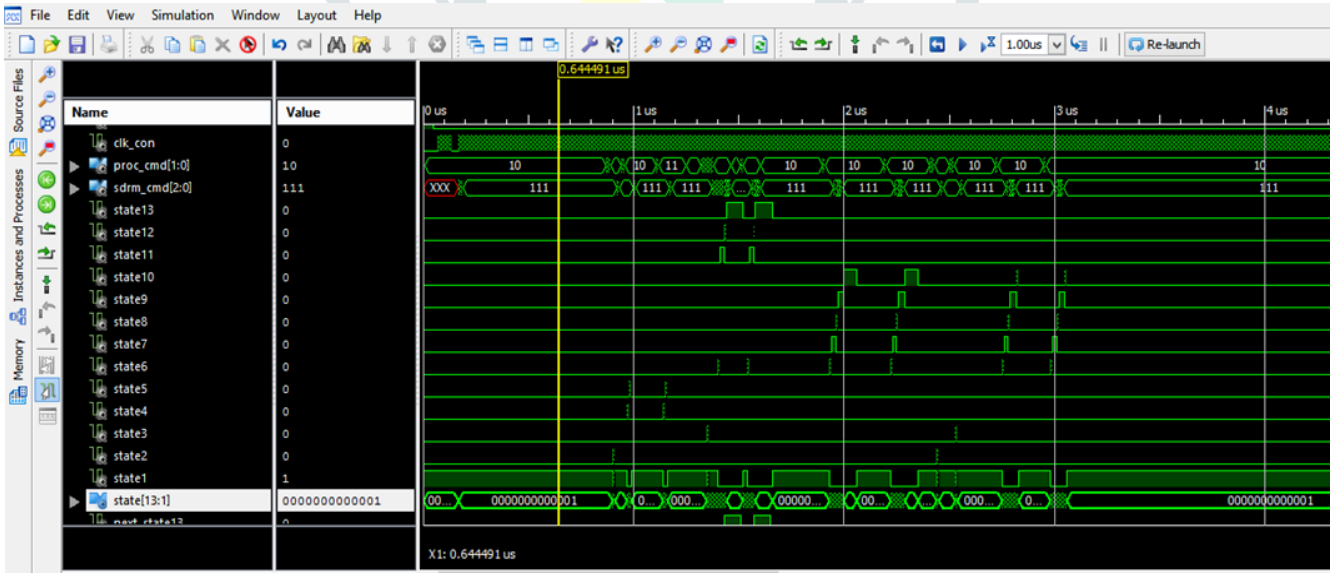

Fig 7: Simulation waveform for Controller Write Cycle

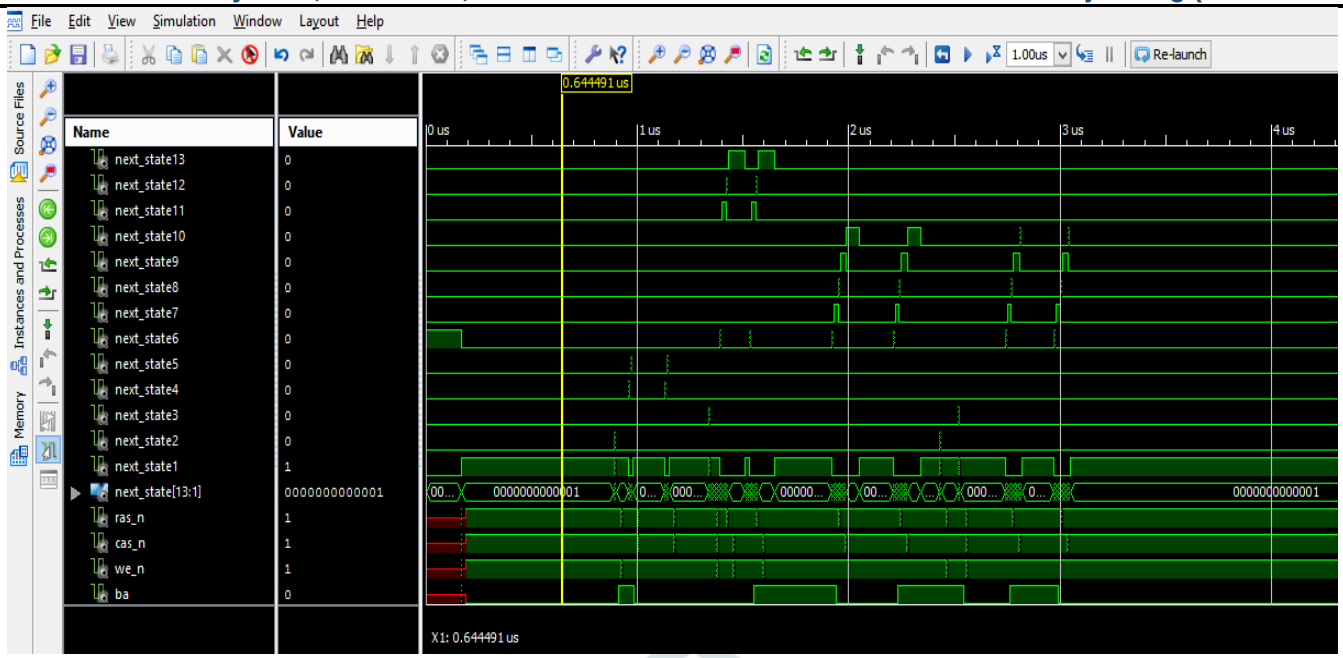

Fig 8: Simulation waveform for Controller Read Cycle

V. CONCLUSION

In this paper it has been demonstrated that this DDR synchronous dynamic random-access memory controller verification method is more time-effective than the other time-consuming directed test method. In this research, a coverage-driven constraint random-based coverage model and reusable, scaleable, and adjustable environment are presented to check the functionalities of a memory controller in a microprocessor. The results demonstrate that this method for verifying memory controllers is quicker than the directed test method. Application of low power design methodologies in the memory controller design would bring further value. Low power techniques significantly reduce the system's overall power consumption. Also, in terms of power and area and results can be used to improve the implementation practices.

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