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ATE CHARACTERIZATION AND TEST TIME REDUCTION TECHNIQUES IN VALIDATION ENVIRONMENT

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Abstract: Each technology node brings a new set of challenges and complex changes to the designs. Increase in the memory blocks requires large amount of area in the chip with the increased test time and faults are observed at each cell. As the memories are designed very dense, results in the escaping of many faults during the testing. Built in self-test (BIST) is the one of the optimistic methodology to test the memories. This work presents the Ratio test method to detect the escaping faults which intern helps to reduce the production test cost with specific set of BIST algorithms. In order to remove the test time problems, we proposed the test time reduction techniques which defines the time to market goals. Ratio test method shows the early detection of design issue bugs and test time is reduced upto 70%.

IndexTerms **- Built in self-test (BIST), Ratio test method, Test time Reduction techniques, Memory block.**

I. INTRODUCTION

Verification of today's complex microprocessors has become the bottleneck of the design cycle. Despite massive pre-silicon verification efforts, chips are still released with devastating bugs. Memory coherence and consistency, which provide guarantees as to the order of memory operations are significant sources of escaped bugs and are likely to become more error prone as designs move from buses towards complex non-deterministic interconnects. The system-level properties related to memory operation policies are difficult to verify due to the vast state space they encompass. As technology moves towards large multiprocessor chips, the verification problem worsens. With the growing density and capacity of integrated chips, their test time is growing rapidly. As test cost is directly related to the time each product stays on the tester, test time reduction has long been an important issue. To overcome these shortcomings, BIST (Built-in self-test) is found to be one of the promising technique to verify the memories, which is an additional hardware and software features into the integrated circuits to allow them to perform self-testing with Distinctive test methodologies and time reduction techniques. Memory BIST(MBIST) and Programmable BIST(PBIST) are the widely used industrial BIST architectures. The fabricated chip (usually called Device under Test) is employed within an Automatic Test Equipment (ATE) which allows to apply dedicated test stimuli to the chip. The stimuli are thereby generated, directly from the user or from other components, sensors, etc. Vice versa, ATE provides an interface which maps the output signals produced by the DUT to the corresponding user outputs, actuators, etc.

II. TEST METHODOLOGY

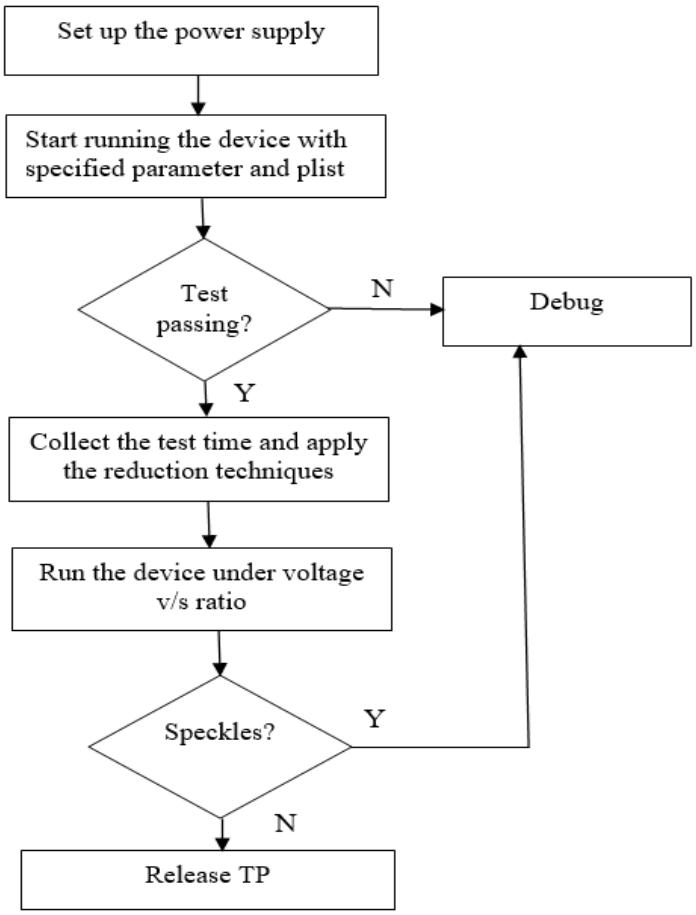


Figure 1. Ratio Test flow

We presented Ratio test method which bounds the different characteristics of the chip at different parametric condition. With optimistic Ratio test methodology, different types of error prones are detected in early stages. Test time reduction techniques are used along with the test method to encounter the yield, market goals. Figure 2 shows the flow chart of Ratio test implementation.

With the multiple power domain, turning off one or more domains is necessary in low power applications. power management unit is designed to handle different sleep modes, multiple power domains with sleep on-off modes are implemented in the test method. Plist is the set of patterns or Algorithms used to test the device, each pattern defines the device behaviour at different parametric condition which helps to detect faults. Chip parametric conditions include check point levels, check point Frequency, wait stage, test mode. when the device starts running with specified parameters, it undergoes the checkpoint testing to make sure device is passing at expected points and runs all the patterns to make sure all the patterns are working properly.

What is ratio? Ratio is the value (example: ratio(min)1 = 0.25v, 0.3ghz, ratio(max) 2 = 1.1v, 1.9Ghz) which defines the voltage and frequency. when device starts running with the ratio and voltage, defines the characteristic of the device, say for chip should be exposed to the all the frequency ranges, consider Fmin to Fmax and voltage ranges, consider Vmin-Vmax. Implemented ratio techniques helps to predict the device aging, device speed along the early detecting bugs.

Two Test programs are developed, one defines the frequency ranges corresponds to the ratio value and other defines the wait stage given at each frequency, wait stage is the delay given between the two start cycles of BIST engine. Based on the device behaviour, debug process starts. we were able to analyse the different types of device behaviour which helps to determine the defect types (hard defect, soft defect) and able to cover all the type of defects.

2.1 Fault Detection Table

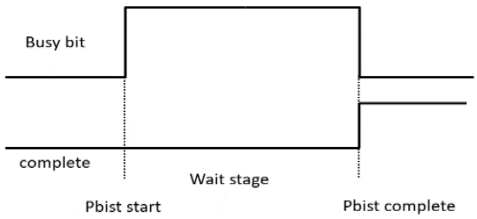
The algorithm describes the logical sequence in which the data is written and read in the array. Table 1 shows the fault detection model we used which connects the test items, the fault set that each of the test items covers, and the test time associated with each test item.

Table 1. Fault detection Model

Fault or defect	Description	Algorithms that detect it
Stuck-at Faults	Cell cannot be written to a zero or one.	Any Algorithm
Transition Faults	Changing state of one cell causes another cell to change state	March, Pmovi
Address Faults	One address to two cells, two addresses to one cell, etc.	Butterfly, Gal, Slidediag
Coupling Faults	Writing a particular value causes another cell to change state	Butterfly, Gal, Walkdiag
Neighborhood Sensitivity	State of neighbouring cells influences fault	March, Butterfly, Movifull
Stability Faults	Read after write flips cell	Pmovi, Movifull, Cellstress, STM
Retention Faults	If we just wait, does array "forget?"	Data retention

2.2 Test Time Reduction Techniques

Wait stage optimization: Wait stage is the delay given between start cycles of the BIST. Delay should be given while running between the patterns in the form of loop (ex: 1000 which means BIST should wait till it executes the 1000 cycle). At high number of loops, all the pattern passes, with certain number of runs, delay will be reduced, say for 1000 cycles to 200 cycles. Number of loops is proportional to BIST execution time function, As the number of loop decreases, BIST function increases which reduces the time.



Optimizing pattern initialization: Every Pattern should run a preamble (Burst on) to check the functionality of each pattern where the test time is very high but running the patterns in the Burst off mode gives optimized test patterns, that pattern which passes all the test is disabled from the pattern list so that to save the test time in running the pattern.

Optimize the vmin search: This is one of the sustained approaches in the industrial environment provides major contribution in the test time reduction. At initial stages, test starts running with the lowest possible vmin (say for example 0.4V), when the test start passing minimal voltage, at next round of test, minimal voltage is shifted to next higher Vmin (say for example 0.6V). This also helps to predict the voltage behavior on the integrated circuits.

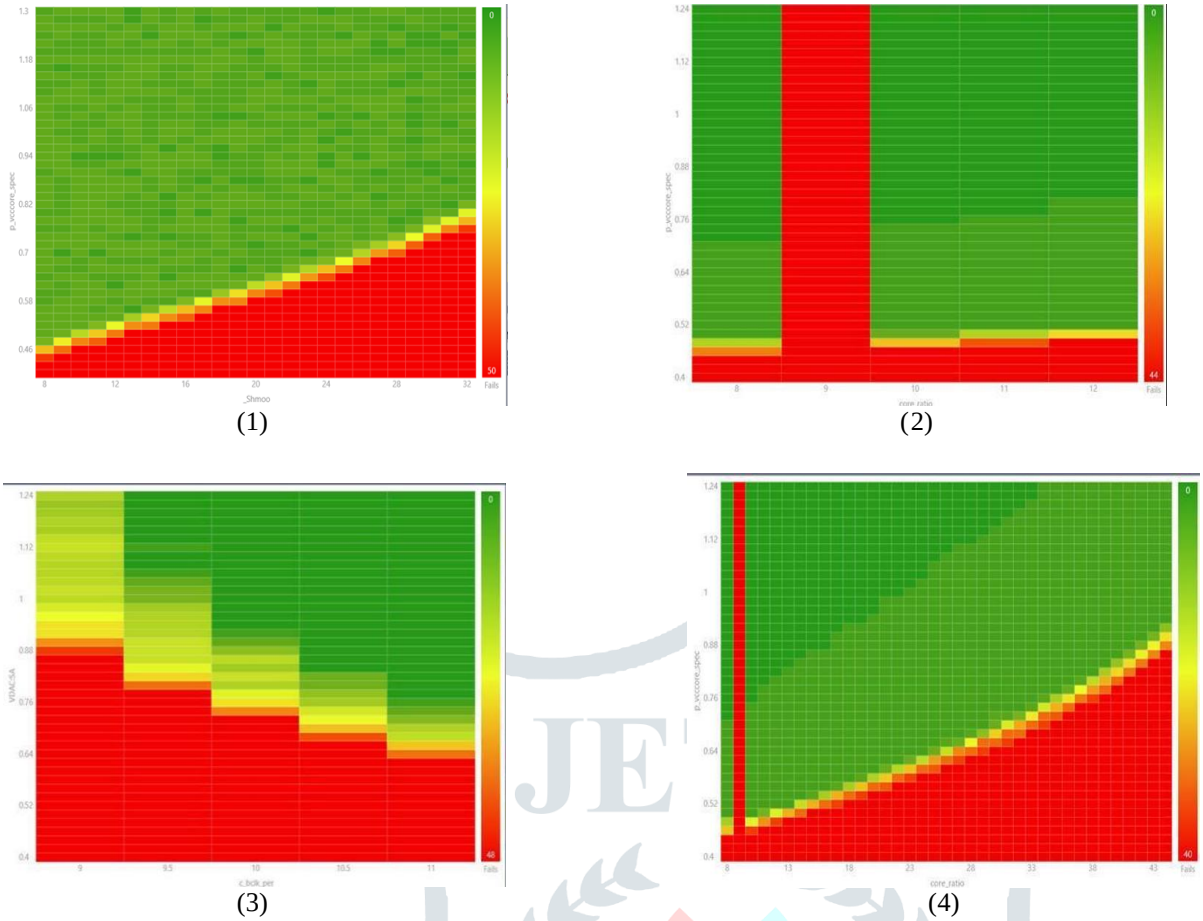
Test 1 vmin= 0.4v
Test 2 vmin= 0.6v
Test 3 vmin= Test2 vmin = 0.6v

Smart Test Condition: Each test needs to be power up and power down at different power domains and voltage settings, which adds the test time of approximately 20ms to each test. Introducing the test condition, so that instead of powering down, it undergoes the level and power domain switching without affecting the other test factor eventually contributes the test time reduction.

III. RESULTS AND DISSCUSSION

We used an industrial silicon set to verify the Ratio test methodology and shows the result from the commercial tester, 100's of packed silicon chips is tested. There are specific industrial tools to implement the test method and test time calculation tools and verified with the different frequencies, with both hot and cold temperature.

Figure 2 shows that various kinds of device responses from ratio test method which assures the early detection of bugs. (1) shows the speckles and instability detection on the devices which may cause early aging of devices. (2) shows the wall on the 0.8Ghz frequency, failure of all the devices. (3) shows the 50% passing result out of 100 devices. (4) shows the wall at 0.8Ghz and instability in the passing devices.



(1) (2)

(3) (4)

Figure 2. Various kinds of device responses

We applied the test time reduction techniques on the different Array domains to meet the test time market goals, Table 2 shows the reduction of test time from 600s to 120s and then from 120s at stage 1 to 60s at stage 2, and at the other domain we observed test time reduction from 900s to 500s to 200s at another domain. Table 2 shows the TTR experimental results with different techniques.

Table 2. Test time Result

ARRAY Domain	Original test time	Stage 1	Stage 2
ARR_1	600s	120s	60s
ARR_2	900s	500s	200s

IV. CONCLUSION

we have proposed the systematic approach to detect the faults in early stage which shows the drastic reduction in the production Test cost. Ratio test Method gives the Behavior of the chips at precised stages and with the different reduction techniques, we were able to achieve the greater reduction the test time. we used different industrial tools to implement the method and to analyze the test time data.

V. ACKNOWLEDGEMENT

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