JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

DESIGN OF TWO STAGE OPERATIONAL AMPLIFIER AND IMPLEMENTATION OF FLASH ANALOG TO DIGITAL CONVERTER

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Abstract: **- In this paper, a 3-bit flash analog-to-digital converter (ADC) using pass transistors is presented. Using DSCH and MICROWIND software tools, a circuit schematic with three comparators, pass transistor switches, and a 3-bit digital-to-analog converter (DAC) is designed. The gates of the pass transistors, which are managed by the comparator outputs, are coupled to the DAC's output. The circuit layout is then created using MICROWIND, and its functionality is checked using a simulation. The circuit's final mask layout is then produced. With the ability to convert analog signals into digital signals with high accuracy, the developed 3-bit flash ADC employing pass transistors is suited for a wide range of applications, including data collection systems, instrumentation, and communication systems. The simulation results demonstrate that the developed ADC performs well in terms of conversion speed and accuracy. The proposed design could, all things considered, be a viable answer for high-speed and high-accuracy ADC applications.**

Index Terms **– Flash ADC, Resistive ladder network, Pass transistors.**

I. INTRODUCTION

The implementation of two stage operational amplifier is the most essential building blocks of the electronics system. In CMOS technologies the design of operational amplifiers continues to pose a challenge as the supply voltage and transistor channel lengths scale down. At different aspect ratio, there is a trade-off among speed, power, gain and other performance parameters. The design and implementation of a CMOS OPAMP is more difficult to get considerable DC gain with high unity gain frequency. In this paper the aim of the design methodology is to propose straightforward yet desired equations for the design and implementation of high gain two staged CMOS operational amplifier. To do this, a simple analysis with some meaningful parameters phase margin, gain bandwidth, etc. is performed. The method manipulates a very wide variety of amplifier architectures, but in this paper, we apply the method to a specific two stage CMOS operational amplifier. The presented paper simulation results have been obtained by 180nm CMOS technology. After the simulation, in ordered to optimize the better performance most of the transistor's size still needed to be modified. The advantages of two stage op-amp have good gain, high output swing, low noise and good bandwidth over folded cascade. And it needs compensation, low PSRR value compared to folded cascade. Now a day design of an operational amplifier is to get high gain and simultaneously optimizing all process parameters has become mandatory.

In wireless communication world entire signals are analogues. But we are surrounded by Digital devices. Everything in the universe measures all signals with analog only. But how analog parameters are in digital devices? Most of the applications are in digital signal processors only. Like microcontrollers, microprocessors. Analog to Digital converters are the mixed signals of both analog and digital for processing the information or data. Present days most of the electronic applications are in digital only. Because of digital have finite set of occurrences. And also, important factor is low power consumption, low operating voltage with a high-speed data transmission. So, we focus on efficient analog to digital converter. We have different types of analog to digital converters like Successive Approximation (SAR), Dual slope ADC, Sigma delta ADC and Flash ADC. Among those most cases we prefer only flash ADC. "Because of its better tradeoff between its all-performance metrics".[1] Some of the basic factors which depend on the performance of ADC are input signal bandwidth, resolution, quantization error, SNR, differential non linearity and integration non linearity. But resolution always inversely proportional to conversion rate of the device.

II. LITERATURE SURVEY

Digital signal processing has advanced intensely due to the rapid expansion of science and technology. In the majority of the digital domains, signal processing offers several advantages such as flexibility in design and programmability, reduced silicon area, high accuracy, as well as a smaller amount of power consumption. The design process is cost-effective and faster. Hence it is possible to design a system with a lesser area along with high speed. It is required to have an analog to digital

converter that offers much higher speed in wireless communication, image processing, etc. [1].

It is preferred to have digital systems that are portable and have prolonged battery life. This can be only possible by developing applications that consume less power. Since ADC's act as front-end components in the majority of mixed-signal systems, we focused to design ADC that consumes less power which in turn offers higher speed. We have various types of ADC architectures for instance successive approximation type ADC, Flash type, sigma-delta, etc. Among these Flash ADC is preferred since it offers high speed because of its parallel architecture, the conversion time is not limited by resolution hence these ADC's are utilized in those systems where bandwidth with a wide range and high speed is required [2].

Al-Ahsan Talukder and Shamim Sarker have implemented flash ADC with 3-bit employing threshold inverter quantization (TIQ). The main feature of this technique is the absence of separate reference voltage power supplies, unlike other Flash ADC implementations. It is possible to set the switching voltage of the inverter by choosing nmos as well as pmos transistors with suitable width to length ratios. This architecture comprises of TIQ comparator, the thermometer to the binary encoder in addition to gain booster. Because of the change in the dimensions of comparator Area changes [3].

Sonu Kumar and Anjali Sharma proposed a strategy employing CMOS technology that is demonstrated for implementing op-amp. They preferred CMOS technology for designing an operational amplifier due to the fact that CMOS devices consume low static power and these devices are highly withstanding noise. The two-stage operational amplifier performance parameters are obtained whose gain is 44.98dB, the phase margin is 63 degrees, the gain-bandwidth product is 33.4MHz, power consumption 276µW[4].

Mirza Nemeth Ali Baig and Rakesh Ranjan have implemented high-speed flash ADC for wireless LAN applications. The designed 3-bit flash ADC is implemented using seven operational transconductance based comparators with the reference voltage of 250mV and a high-speed encoder is implemented using full adders. This design is a flash-based ADC converter with a finite output resolution of three bits and power consumption of about 223µW and resides in a chip area of 0.089287 mm2. The high-speed flash ADC is being designed and verified using the CADENCE Virtuoso tool with CMOS 180 nm technology. Since ADC is implemented by utilizing a full adder-based encoder, The area is limited by the resolution [5].

Sarojini Mandal and J.K.das had implemented a 3-bit flash ADC using cascading full adder by using pass transistor logic that makes the circuit much faster. They have improved the efficiency of flash ADC by improving the working of the comparator by scaling down the length to width ratio of transistors assuming transistors operating in the saturation region. The gain of comparator increased by proper sizing of transistors. The encoder circuit is designed using a full adder with 10 transistors. Chip complexity and area are reduced using pass transistor logic employed in a full adder circuit. As full adder is designed using pass transistor, logic levels will deteriorate [6].

Jayesh. J. Vyas implemented flash ADC comprising 3-bit resolution employing 180-nanometer technology files using NG spice tool for high-speed applications. The response time of the ADC and the comparator was calculated as 4.9 ns and 3.7ns. Power consumed by ADC is given as 50µW. Encoder circuit is implemented using basic gates. The gate delay for the inverter, two-input, three-input, and four-input NAND gates are given as 0.29ns, 0.51ns, 0.37ns, 1.06ns respectively with 2ns rise time and fall time for inputs. Comparator sensitivity and comparator gain are calculated as 11mV and 29dB respectively. the main drawback is delay increases linearly with resolution since NAND gates were used [7].

Piyush V. konodiya had implemented flash ADC for highspeed ultra-wideband communications (it's a form of technology whose signal bandwidth is greater than 500MHz). Flash ADC employing ROM based encoder is designed and reported Conversion time, as well as the power consumption of the circuits, are given as 13.64mW and 1.135ns respectively. It is not possible to suppress bubble errors utilizing a ROM encoder because it is slow [8].

III. PROPOSED SYSTEM

A 3-bit flash analog-to-digital converter (ADC) using pass transistors has been designed using DSCH and MICROWIND software tools. The design process involved creating a circuit schematic for the ADC consisting of three comparators, pass transistor switches, and a 3-bit digital-to-analog converter (DAC). The output of the DAC is connected to the gates of the pass transistors, which are controlled by the comparator outputs. The circuit layout was then designed using MICROWIND, and a simulation was run to verify its functionality. The final mask layout for the circuit was then generated. The designed 3-bit flash ADC using pass transistors can convert analog signals into digital signals with high accuracy, making it suitable for various applications such as data acquisition systems, instrumentation, and communication systems.

Design of Two Stage Operational Amplifier

The designed circuit is to meet the required specifications is shown in fig.4.1 The topology of this circuit is that of a standard CMOS op-amp. The designed CMOS operational amplifier circuit consists of three subsections, namely differential gain stage, second gain stage and bias strings. The main aim of this topology was able to successfully meet all of the design specifications. The circuit operation has explained below.

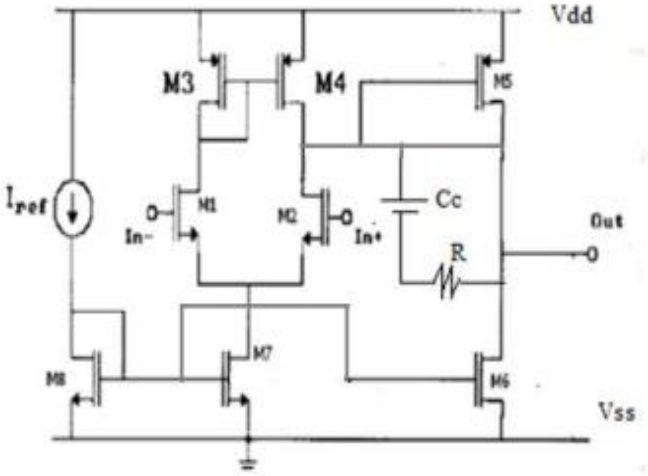


Fig.3.1 Circuit diagram of two stage operational amplifier

Differential Gain Stage

The differential gain stage consists of M1, M2, M3 and M4 form the first stage of the operational amplifier. Transistors M1 and M2 are standard NMOS which form the basic input stage of the differential amplifier. The gate of M1 and M2 are the inverting and non-inverting inputs with respect to transistors. The two main resistances that contribute to the output resistance are that of the input transistors and also the output resistance of the active load transistors, M3 and M4. The gain of the two-stage operational amplifier is the

Transconductance of M2 times the total output resistance at the drain of M2. A differential input signal applied across the two input terminals that will be amplified according to the gain of the differential stage. In this circuit have advantages by using the current mirror active load transistors M3 and M4. The use of active load devices gives a very large output resistance. The current mirror topology helps to conversion of the input signal from differential to single-ended. And load helps with common mode rejection ratio. The current from M1 is mirrored by transistors M3 and M4 as shown and subtracted from the current from M2. The differential current from M1 and M2 multiplied by the output resistance of the first stage will gives the single-ended output voltage. And also, which constitutes the input of the second gain stage.

Second Gain Stage

This stage consists of transistors M5 and M6, as the name indicates, is to provide additional gain in the amplifier. Output from the drain of M2 and amplifies it through M5 which is called as common source configuration. Similar to the differential gain stage, this stage employs an active device M6, to serve as the resistance for M5. Gain of this stage can be determined by the Transconductance of M5 times the effective load resistance comprised of the output resistance of the M5 and M6. Where M5 acts as the load, M6 is acts as the driver.

Bias String

The biasing of the operational amplifier is achieved with four transistors. Transistors M6 and M7 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. In this circuit proper biasing of other transistors in the circuit (M1-M5) is controlled by the node voltages. M5 is biased by the gate to source voltage (VGS) set up by the VGS of the current mirror load as are the transistors M1 and M2 as shown in above fig.4.1. The designed and implemented in this project is a two-stage operational amplifier with an n-channel input pair. And op-amp uses a dual-polarity power supply Vdd and Vss so the given ac signals can swing above and below ground. At the output the capacitance is to be connected as shown in fig.2.The design of two stage op-amp includes all the process parameters into account and which contribute in performance of overall gain of the system. High gain, bandwidth, and good power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) are some of the desired features of a good operational amplifier.

FLASH ADC

The General block diagram for a 3-bit Flash ADC is given in below Fig -4.2. A Flash ADC is framed of mostly three blocks Resistor ladder, Comparator array and Thermometer to Binary code encoder. Resistor ladder is utilized for producing different reference voltages. The incoming analog signal is compared with these generated reference voltages using the comparator array and the corresponding thermometer code will be generated. These thermometer codes are given to the advanced encoder which will change over them to the relating binary codes.

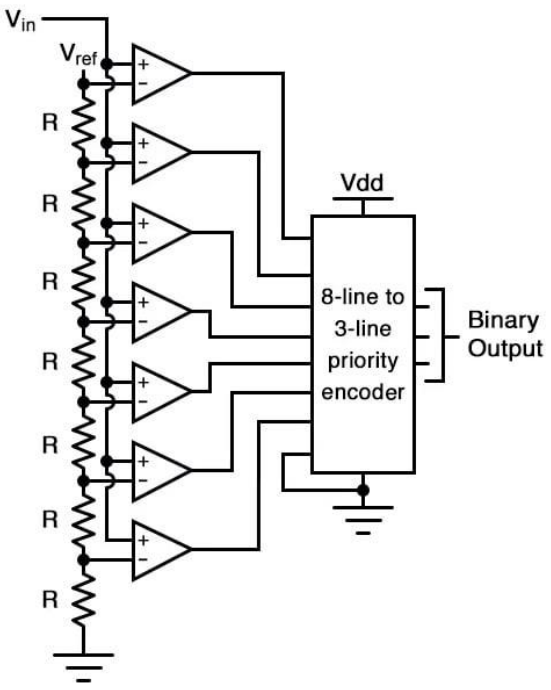


Fig 3.2: Block Diagram of 3-Bit Flash ADC

CONVENTIONAL FLASH ADC

Among the different types of ADC's flash ADC have its more advantages. The main important factor of ADC is high conversion speed. It compares analog input along with reference threshold voltage and identifies which the value is closest through encoder and converts into digital. Basic block diagram of flash ADC shows below. In conventional type of ADC have resistor ladder, comparator and encoder modules. Among those key component is comparator. Because when n bits conversion requires 2N-1 comparators are required. So that overall performance depends on the comparator module. And also, it has an impact on overall power consumption. only the comparator module operates at a high operating voltage. When we want to design a comparator, we must have a minimum three architectures. First one is an amplifier must have high gain and single ended output, second one type of latches used in comparators. And third one is holding the input circuit and track it. Majorly it requires more gain. For MOS structure it is impossible to get high gain, so we used a greater number of stages

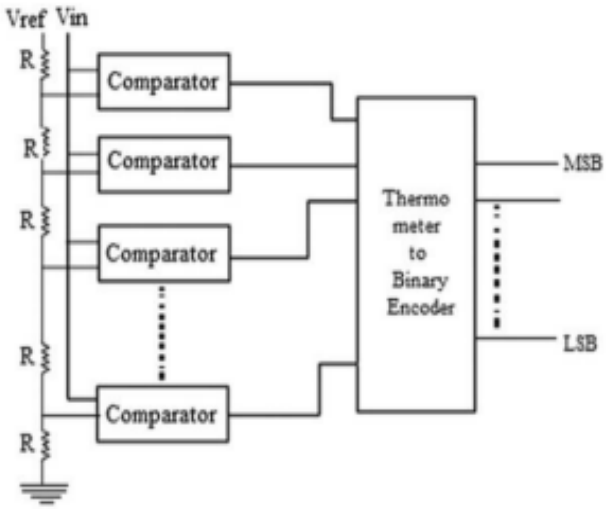


Fig.3.3 Basic Block diagram of conventional ADC

3-BIT FLASH ADC

To implement N bit flash ADC, we require 2N-1 comparators are needed. Similar to op-amp, the comparator comprises of two inputs where analog input is given to the inverting terminal and reference voltage is applied to noninverting terminal. Comparators are divided with the help of the resistive ladder network. 2N resistors are utilized to form a resistive ladder network of N bit. Since we have implemented 3-bit, the number of resistors required will be eight. The reference voltage is generated across the resistive ladder network between reference voltage and ground is equally distributed and is differed by the least significant bit. the comparator compares the reference voltage signal with the input analog signal and indicates output as logic high whenever analog input exceeds reference voltage and indicates logic low output when analog input is smaller than reference voltage.

The output of comparators forms a thermometer code. Further, we need to translate thermometer code into binary code [9]. The output generated mainly depends on the resolution. But the major disadvantage is as the resolution increases, the number of comparators required will get increases. For example, if we need to implement flash ADC of 9 bit, we need 511 comparators which occupy a huge die area and dissipates a large amount of power. Hence, we need to reduce the power and area of flash ADC as they are major constraints. Resolution of flash ADC does not determine accuracy; it just indicates the total bits that are obtained at the output side.

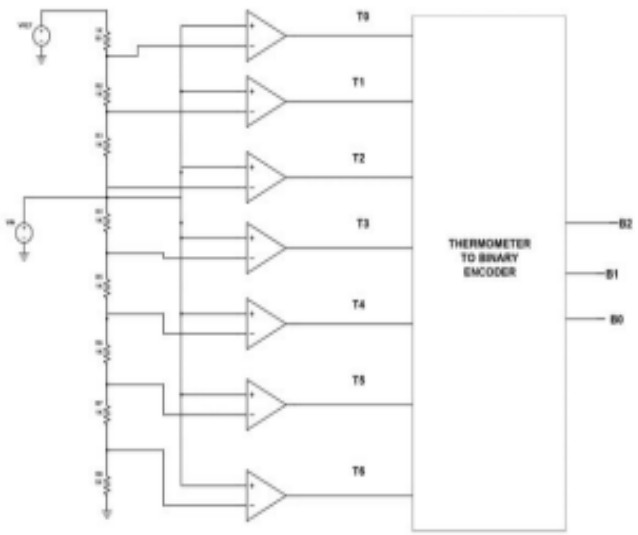


Fig 3.4: 3-bit Flash ADC block diagram

RESISTIVE LADDER NETWORK

The Figure 3.5 shows resistive ladder network. In this paper, we have implemented 3-bit flash ADC comprises of resistive ladder network. It is possible to provide a steady reference voltage to the comparators utilizing the resistive ladder network. 2N resistors are required to design N-bit Flash ADC.

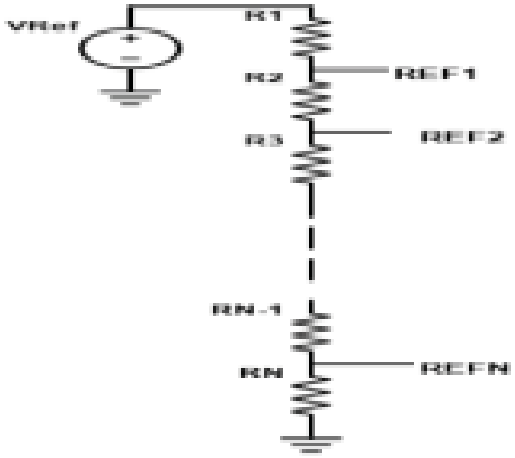


Fig 3.5: Resistive Ladder Network

The main function of this ladder network is that it divides reference voltage across all resistors such that the difference between the reference voltage of the corresponding two comparators will be the least significant bit value. Since we have given reference voltage of 1.8 volts, each comparator reference voltage will be differed by 255mV.

THERMOMETER TO BINARY ENCODER

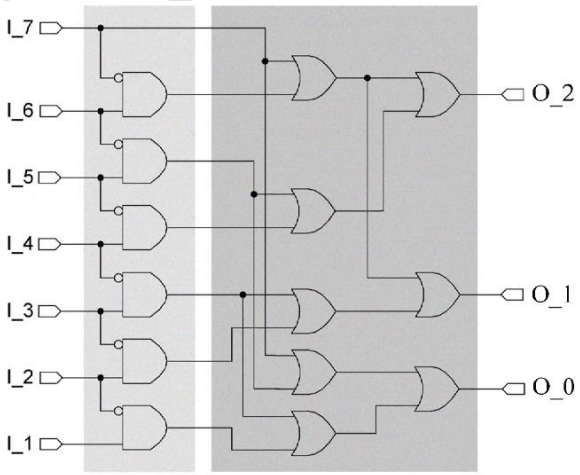


Fig 3.6: Thermometer to binary Encoder

A thermometer to binary encoder is a digital circuit that converts a thermometer code into a binary code. In a thermometer code, the number of bits set to logic high (1) represents the input voltage level. For example, in a 3-bit thermometer code, the input voltage can be represented as 111 (highest voltage level), 110, 101, 100, 011, 010, 001, or 000 (lowest voltage level).

The operation of a thermometer to binary encoder can be explained using a 3-bit encoder as an example. The input of the thermometer to binary encoder is a 3-bit thermometer code generated by a flash ADC or other ADC circuits. The output of the thermometer to binary encoder is a 2-bit binary code that represents the input voltage level. The circuit consists of a series of AND gates and inverters. The AND gates generate the binary code by combining the thermometer code bits. The inverters are used to complement the outputs of the AND gates to generate the proper binary code. For example, for a 3-bit thermometer code, the circuit diagram would look like this: In this circuit, the

thermometer code is input to the AND gates, which produce a binary code output. The inverters are used to complement the binary outputs such that only one bit is set to logic high at a time, representing the input voltage level.

For example, if the input thermometer code is 110, the first AND gate produces a logic high output for bits 1 and 2, and a logic low output for bit 3. The second AND gate produces a logic high output for bits 2 and 3, and a logic low output for bit 1. The third AND gate produces a logic high output for bits 1 and 3, and a logic low output for bit 2. The outputs of the AND gates are inverted, and the resulting binary code output is 10, representing the input voltage level.

In summary, a thermometer to binary encoder circuit is a digital circuit that converts a thermometer code into a binary code using a series of AND gates and inverters. The output represents the input voltage level and is used in conjunction with ADC circuits to convert analog signals into digital signals.

PROPOSED FLASH ADC

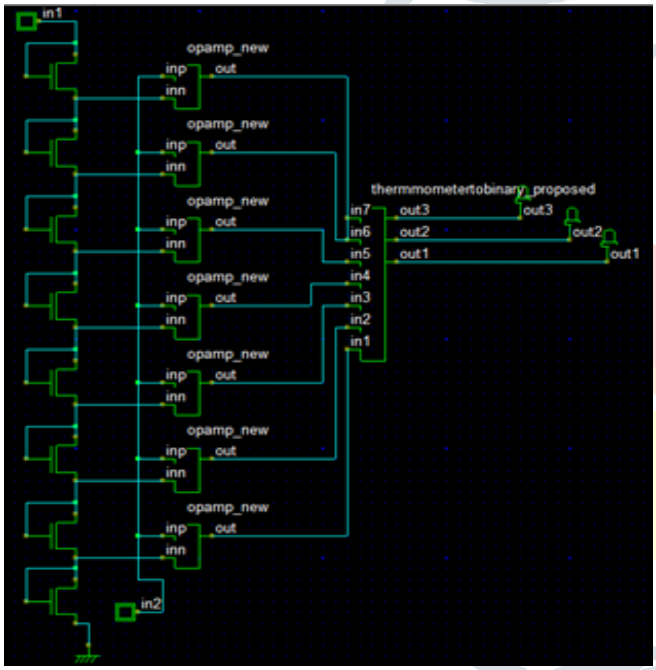
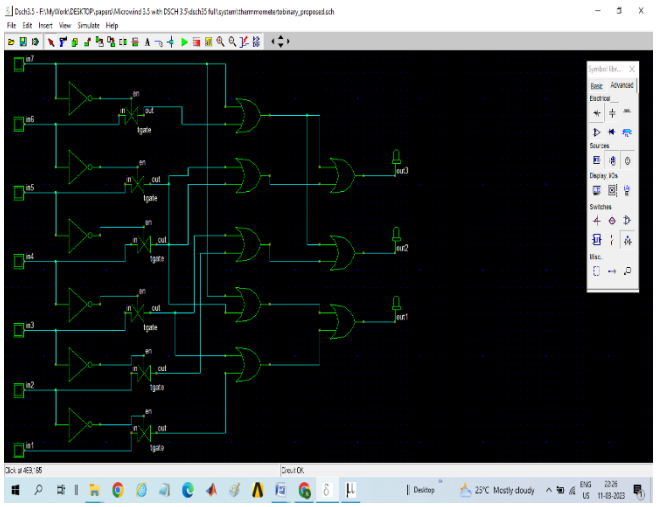


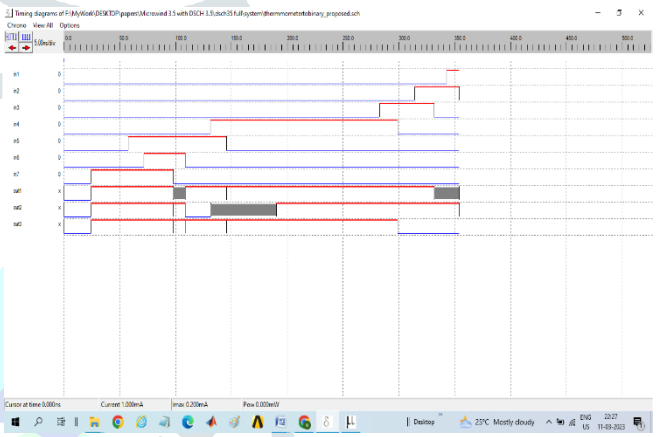
Fig 3.7. 3-bit Flash ADC using Pass transistors

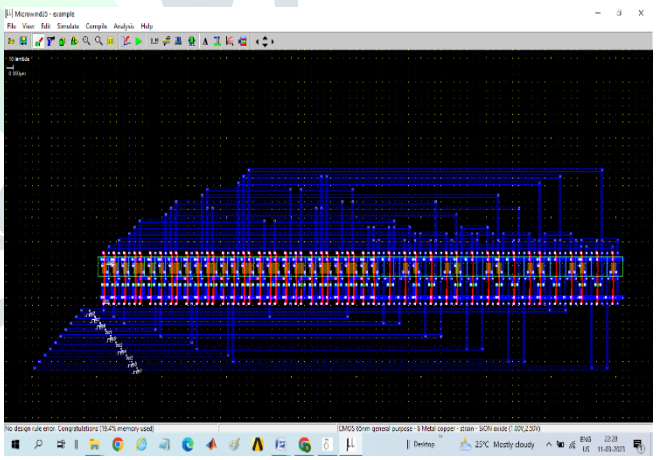
This paper aims to design a 3-bit flash ADC using pass transistors, an op-amp comparator, a thermometer to binary encoder, and output using DSCH and MICROWIND. The ADC circuit uses pass transistors to compare an input voltage with three reference voltages, and the output is connected to an op-amp comparator circuit. The op-amp comparator output is then connected to a thermometer to binary encoder circuit that converts the thermometer code to a binary code. The circuit is simulated using DSCH and optimized if necessary. The layout is generated using MICROWIND, and verified using the DRC and LVS tools. Finally, the layout is simulated using the extracted netlist, and the GDSII file is generated for fabrication.

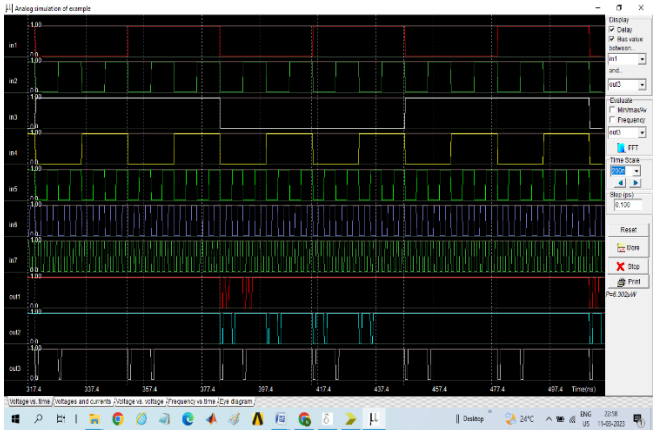
IV. SIMULATION RESULTS

Proposed Thermometer to binary

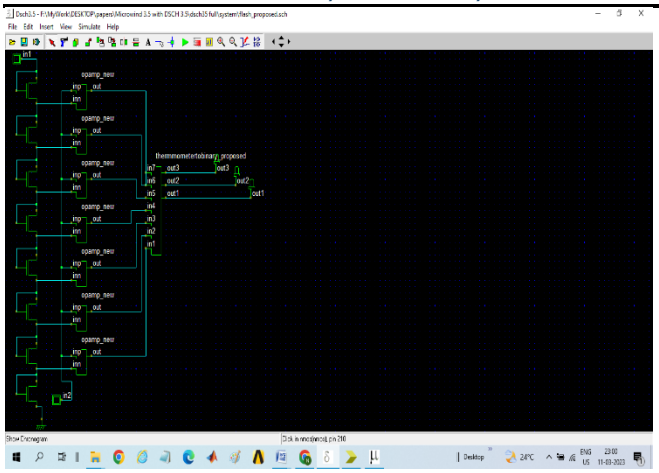


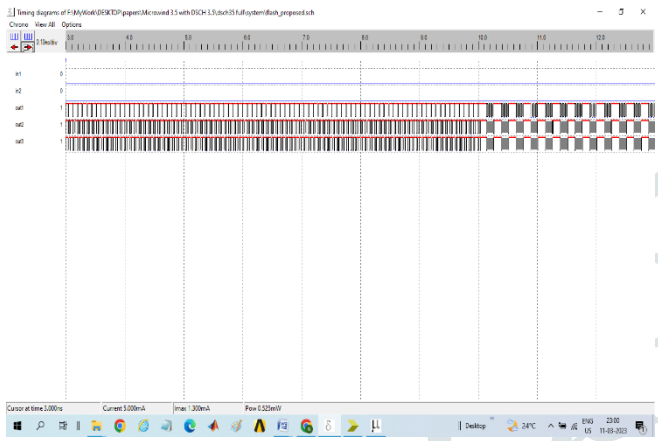


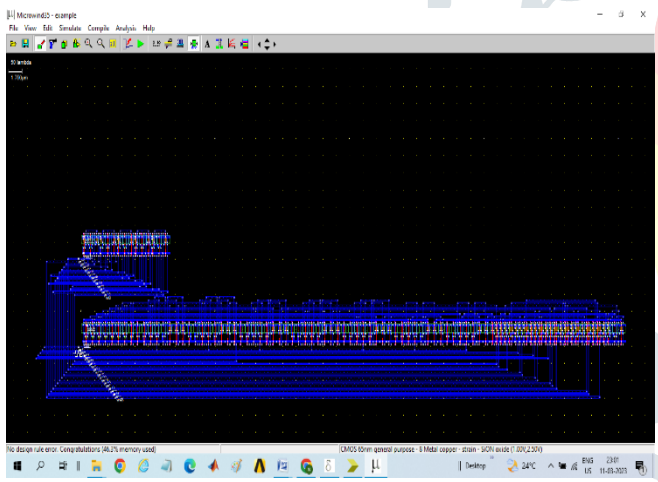


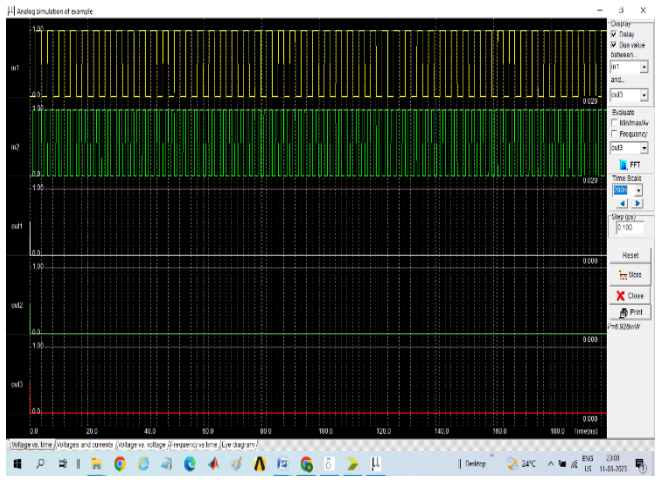


Proposed Flash ADC









V. CONCLUSION

Based on the outcomes of the simulations performed using DSCH and MICROWIND Tools, the 3-bit flash ADC with pass transistors, op-amp comparator, thermometer to binary, and output can be regarded as a successful design. An accurate translation of analog input signals to 3-bit digital outputs was demonstrated by the developed ADC. The design's advantages of simplicity, high speed, and low resolution make it a good fit for a variety of applications that call for quick and low-resolution ADCs. It is important to note that the design can be changed to improve the resolution while preserving the same speed and ease of use by incorporating more thermometers and comparators into the binary decoders. As a result, the suggested design can act as a starting point for the creation of high-performance ADCs in the future.

FUTURE SCOPE

1. The designed ADC can be modified to increase its resolution by adding more comparators and thermometer to binary decoders. With the increase in resolution, the ADC's accuracy can be improved, making it more suitable for a wide range of applications.
2. Integration into larger systems: The ADC can be integrated into larger systems, such as microcontrollers or digital signal processors (DSPs), to perform specific functions like data acquisition or signal processing.

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