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"ANALOG TO DIGITAL CONVERTER IN CADENCE"

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Abstract : An Analog-to-digital converter (ADC) is a crucial component in modern electronic systems, enabling the conversion of continuous Analog signals into digital values. In this project, an ADC was designed and implemented in Cadence Virtuoso, a widely-used electronic design automation tool. In this thesis, we develop a 7 stage 8-bit pipeline ADC circuit in process. The complete design methodology, from system simulation to schematic entry, from circuit simulation to post signal analysis is proposed. The operation frequency of the pipeline ADC is pushed to the upper limit of the process used. The ADC is designed and simulated in Cadence environment. Post simulation signal analysis is done in Virtuoso in order to verify its performance.

Index Terms **- Pipeline ADC, 1-bit stage, Virtuoso Cadence.**

I. INTRODUCTION

Analog signals are continuous in respect to both time and amplitude. To use Analog signals in digital devices the amplitude is limited to a finite number of levels, and is converted to a time discrete signal by sampling the Analog signal at a fixed interval. The conversion of an Analog signal to a digital signal is done by an Analog-to-digital converter (ADC).In the field of Analog-to-digital conversion; the Pipeline ADC architecture has gained significant popularity due to its ability to achieve high-speed and high-resolution conversion. Pipeline ADCs are widely used in various applications, including telecommunications, data acquisition systems, image sensors, and many more. Cadence is a leading provider of electronic design automation (EDA) software, offering a comprehensive suite of tools for designing and verifying integrated circuits. Cadence tools are extensively used in the industry for designing and simulating complex Analog and digital systems, including the design of Pipeline ADCs. The design process of a Pipeline ADC involves several stages, starting from the architectural definition and transistor-level design to layout, simulation, and verification. Cadence provides a range of tools that facilitate each step of this process, enabling designers to create robust and efficient Pipeline ADCs.

One of the primary advantages of using Cadence tools for Pipeline ADC design is their ability to accurately model and simulate the behaviour of the ADC at different levels of abstraction. From transistor-level simulations to system-level simulations, Cadence tools provide a comprehensive platform for performance evaluation and optimization. The Cadence Virtuoso platform offers a powerful environment for designing Analog and mixed-signal circuits, including Pipeline ADCs. It provides a user-friendly interface for schematic capture and layout design, allowing designers to create and modify the ADC's circuitry with ease. Furthermore, Cadence Spectre and Spectre RF simulators enable accurate and efficient circuit-level simulations, helping designers to evaluate the performance of the Pipeline ADC under different operating conditions. To ensure the robustness and reliability of the designed Pipeline ADC, Cadence tools offer advanced verification capabilities. From functional verification using Cadence Incisive Enterprise Simulator to parasitic extraction and circuit reliability analysis using Cadence Quants Extraction Solution, these tools allow designers to identify and address potential design issues before tape-out.

II. RELATED WORK

Compared with other ADC pipelined ADC make use of less number of comparators with leads to high latency. In data convenient devices and wireless communication systems pipelined ADC serves as a prominent component as it can produce an efficient output with high speed and better resolution. The 1 bit ADC block made of a sample and hold circuit, a comparator and a MDAC which multiplies the reference voltage to that of a input basic signal SAR control logic and DAC inside the SAR ADCs contribute to power consumption [1]. An Analog-to-Digital converter is a basic device, which translates an analog voltage signal into a corresponding digital number. Whenever we relate to the real world mainly of the signals are analog in nature [2]. Pipelined Analog-to-Digital Converter is a building block which offers the attractive arrangement of low power dissipation, high resolution and improved high speed. Hence the Pipelined ADC is an finest solution for low power applications like wireless communication systems [5].

III. CADANCE VIRTUOSO

Cadence software is a comprehensive suite of electronic design automation (EDA) tools that enable engineers and designers to design, verify, and analyse integrated circuits (ICs) and electronic systems. It offers a wide range of software tools tailored for various stages of the design process, including schematic capture, simulation, layout design, and verification. One of the key components of Cadence software is the Virtuoso platform, which provides a user-friendly environment for schematic entry and design capture. With Virtuoso, designers can create circuit schematics using a rich set of library components, drag-and-drop functionality, and intuitive drawing tools.it also includes tools for layout design, such as the Virtuoso Layout Suite. This suite provides a robust set of tools for creating physical layouts of ICs, including placement, routing, and optimization capabilities. Designers can precisely place and route components, define power and ground networks, and ensure compliance with design rules and manufacturing constraints. The suite also includes features for design rule checking (DRC) verification to ensure layout accuracy and adherence to design specifications.

IV. PAGE LAYOUT

Creating a page layout for a Pipeline ADC design using Cadence, it is important to consider the organization and arrangement of various components to ensure a clear and concise representation of the design. Here's a suggested page layout for a Pipeline ADC in Cadence.

Block Diagram: Provide a block diagram illustrating the overall architecture of the Pipeline ADC. Include labelled blocks for each stage of the ADC, such as sample-and-hold, amplifier, comparator, and digital logic. Use clear connections and arrows to indicate the data flow and signal paths between the different blocks.

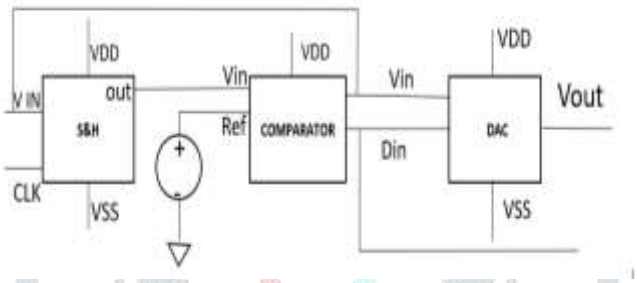

Fig.4 1bit pipeline architecture

V. SIMULATION RESULT

Schematic Diagram: Create a schematic diagram that represents the detailed circuitry of the Pipeline ADC. Organize the schematic by grouping related components together. Clearly label and annotate each component, including transistors, capacitors, resistors, and other active and passive elements. Use consistent and readable font sizes for text labels and annotations. Highlight key components or nodes that require special attention.

1-bit pipeline Analog-to-digital converter (ADC) is a type of electronic circuit that converts an Analog input signal into a digital output signal with high speed and high resolution. It uses a pipeline architecture that is composed of a series of stages, each of which contributes to the overall conversion accuracy.

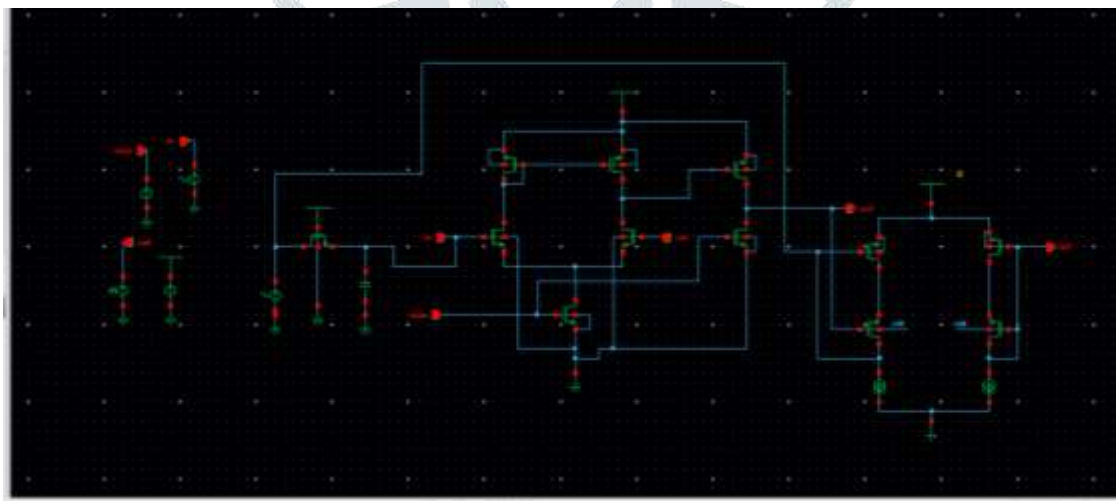

Fig.5.1: 1-bit pipeline ADC

1-bit ADC: The basic blocks used to design a 1-bit ADC are Comparator, Multiplexer, Sample and Hold.

Comparator: A comparator is an electronic circuit that compares two input voltages and produces an output voltage that indicates which input is higher. It is commonly used in electronic systems for signal conditioning, control, and measurement applications. We are using six transistor CMOS in which four are CMOS and three are PMOS. The two PMOS and NMOS transistor are connected in series such that it forms inverter and the last two NMOS transistor work as access transistor which are connected in series to world line. The access transistor is active only when we give the input word line as high Basically, Comparator performs three operations which are Sample and Hold, operations.

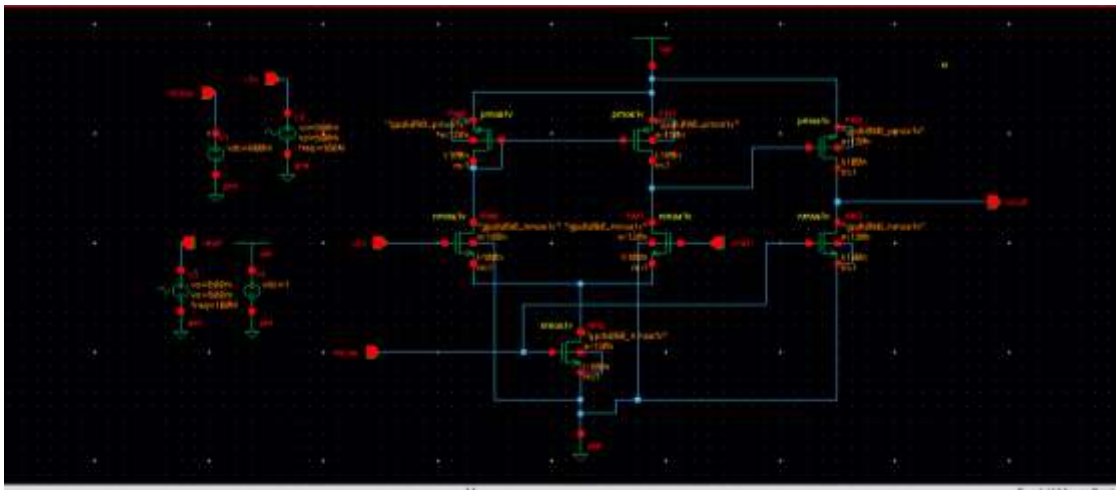

Fig.5.2 Schematic Diagram of Comparator

A single-input DAC, or digital-to-Analog converter, is a type of electronic circuit that converts digital signals into Analog signals. It takes a digital input signal, usually represented as a series of binary values, and converts it into a corresponding Analog output signal.

A multiplying digital-to-analog converter (DAC) is a type of DAC that generates analog output voltages by multiplying a digital input code by a reference voltage. It is commonly used in various applications, such as audio processing, instrumentation, communication systems, and signal conditioning. the digital input code is typically represented by a binary word, and each bit of the code corresponds to a weighted current source or a switch. The reference voltage is multiplied by the weighted currents or selectively connected to the output through the switches, producing an analog output voltage proportional to the input code.

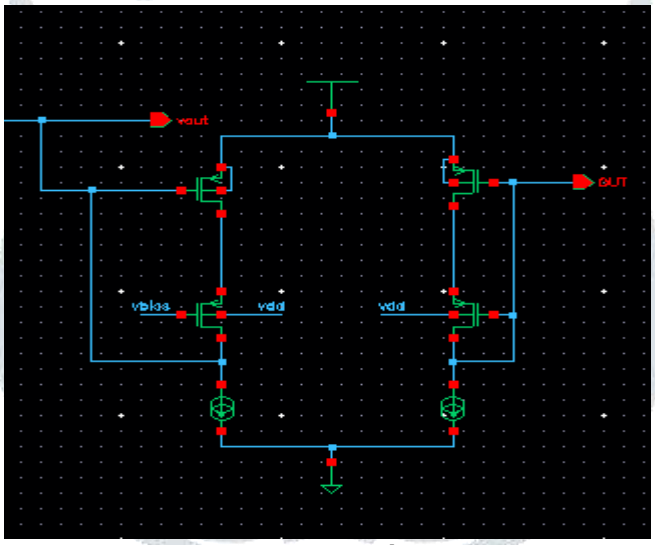

Figure 5.3. DAC Schematic

Once the layout is complete, the designer can use Cadence's **Design Rule Checker** (DRC) tools to ensure that the layout is correct and matches the original schematic. Any errors or discrepancies must be identified and corrected before the IC can be fabricate.

Design Rule Check (DRC) and Layout Versus Schematic (LVS): Allocate space for DRC and LVS error messages and violations, if applicable. Include tables or lists to document any DRC or LVS issues encountered during the layout process.

The output waveforms are shown in Fig.5.4 where the levels are compared.

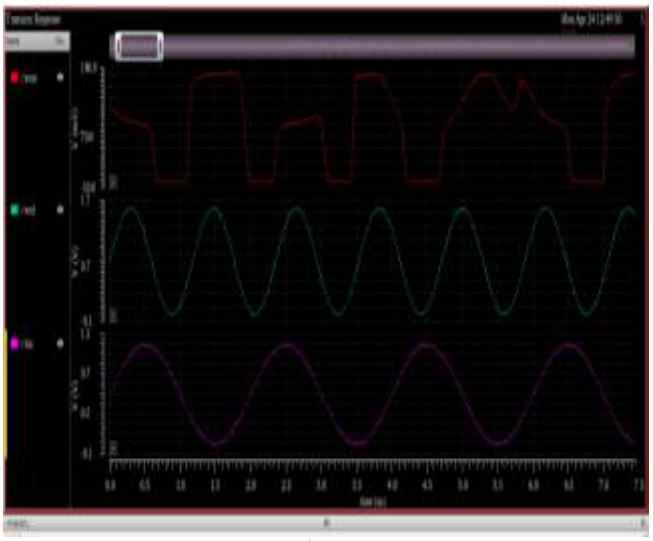

Figure 5.4Waveform of Comparator

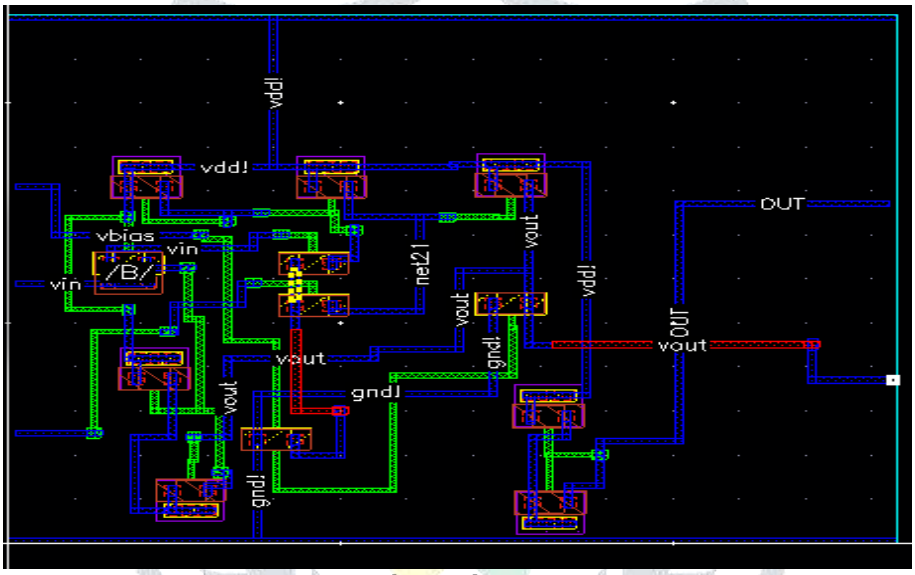

Figure 5.5 1-bit pipeline ADC Layout

The output waveforms of 1-bit pipeline ADC are shown in Fig.5.6

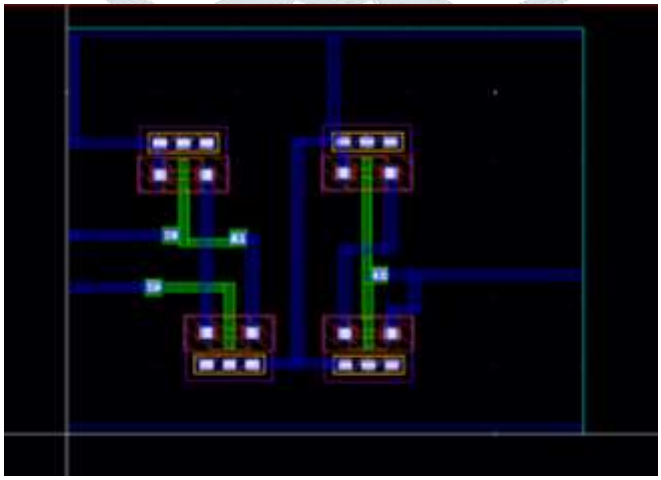

Figure 5.6 - *Layout of DAC*

The output waveform of a 1-bit pipeline Analog-to-digital converter (ADC) is a digital signal that represents the input Analog signal in a binary format. The waveform is a series of digital values, with each value representing the voltage level of the input signal at a specific point in time.

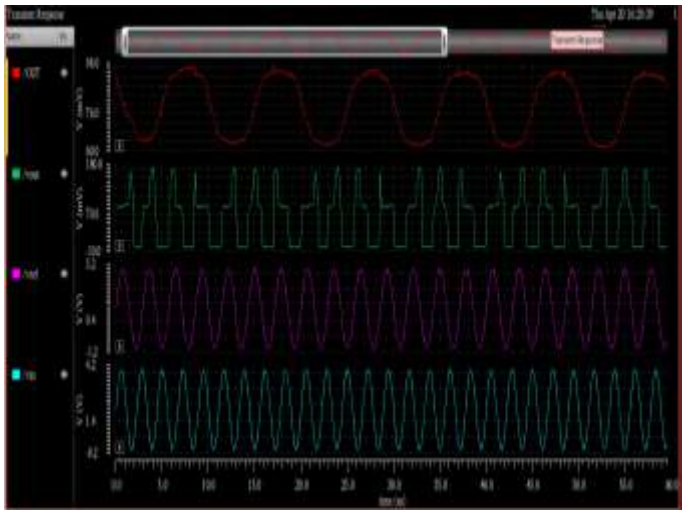

Figure 5.7. Output waveform of 1-bit Pipeline ADC

VI. CONCLUSION

In conclusion, the Pipeline ADC architecture has proven to be a highly effective solution for achieving high-speed and high-resolution analog-to-digital conversion. Through its segmented structure and interleaved operation, Pipeline ADCs offer excellent performance while minimizing complexity and power consumption. Overall, the Pipeline ADC design process using Cadence tools enables engineers to overcome the challenges associated with high-speed and high-resolution analog-to-digital conversion. It facilitates the development of robust, efficient, and high-performance Pipeline ADC designs, positioning them as crucial components in a wide range of applications, including telecommunications, data acquisition systems, image sensors, and beyond.

REFERENCES

[1] Dr. C. Gomathy, Athirai. C et.al 2018 in his title "Design of 8-bit Pipeline ADC Using AHDL", the purpose of Design of 8-bit Pipelined ADC using AHDL, International Journal of Pure and Applied Mathematics, Volume 119 No. 15, ISSN: 1314-3395, 2018.

[2] G. M. Anitha Priyadarshini, Dr. G. A. E. Sathish Kumar et.al 2018 in her title "A Dynamic Threshold MOS Logic Based Low Power 8-Bit Pipeline ADC for Wireless Communications", the purpose is A Dynamic Threshold MOS Logic Based Low Power 8-Bit Pipeline ADC for Wireless Communications, International Journal of Science and Research (IJSR), Volume 7 Issue 4, ISSN: 2319-7064, April 2018.

[3] Nahid Mirzaie, Ahmed Alzahmi et.al 2018 in his title "Three-Dimensional Pipeline ADC Utilizing TSV/ Design Optimization and Memristor Ratioed Logic", the purpose of Three-Dimensional Pipeline ADC Utilizing TSV/ Design Optimization and Memristor Ratioed Logic, IEEE Transactions On Very Large Scale Integration (VLSI) Systems, ISSN: 1063-8210, April 2018.

[4] Jie Yuan, Nabil H. Farhat et.al 2008 in his title "Background Calibration with Piecewise Linearized Error Model for CMOS Pipeline A/D Converter", the purpose of Background Calibration with Piecewise Linearized Error Model for CMOS Pipeline A/D Converter, IEEE, Volume. 5, issue 1, February 2018.

[5] C Ashwini, Prof Naveen I G et.al 2016 in his title "A Design of 8-bit Pipelined ADC for High Speed Applications Using Cadence Virtuoso", the purpose of A Design of 8-bit Pipelined ADC for High Speed Applications Using Cadence Virtuoso, International Journal of Innovative Research in Science, Engineering and Technology, ISSN: 2319-8753, Vol. 5, Issue 9, September 2016.

[6] Himanshu Raj Pashine, Jayanthi K Murthy et.al 2015 in his title "12bit, 80MHz, 230Mw Pipeline ADC Using 3bit Flash ADC", the purpose of 12Bit, 80MHz, 230mW Pipeline ADC using 3Bit Flash ADC, International Journal of Science and Research (IJSR) Volume 4 Issue 4, ISSN: 2319-7064April 2015.

[7] Krzysztof Wawryn, Robert Suszyński et.al 2015 in his title "Low Power Low Voltage Current Mode Pipelined A/D Converters", the purpose of Low Power Low Voltage Current Mode Pipelined A/D Converters, World Academy of Science, Engineering and Technology, Vol. 4, May 2015.