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Different PWM control analysis for reduced switch count and cascaded H bridge multi level inverter topology

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Abstract : Power conversion with high performance, low switching loss, and low THD values related to voltage and current necessitate the design of a multilevel inverter. In a multi-level inverter, the optimal output value is determined by the harmonic quantities to raise the output levels. The harmonic performance of the nine-level cascaded H bridge (CHB) converter is remarked in this paper and results are monitored for various Pulse width modulation techniques and different loads like resistor, inductor values. The same amount of voltage level is developed using reduced switch count multilevel inverter (RSC-MLI) named cascaded T type topology, this circuit control algorithm uses a smaller number of carrier signals compared with CHB-MLI. To validate the operation of the nine level CHB and RSC-inverter module topologies, MATLAB simulation results are presented.

IndexTerms **- Multilevel inverter, PWM, Switching loss, THD.**

I. INTRODUCTION

There is a huge demand these days for industrial robotic, automotive, and automation systems that can be driven by the movement and retain the high efficiency of the batteries used in these devices due to energy conversion. Thus, in this case, multi-level converter producing more than two voltage levels which are more suitable for many high-power medium voltage applications due to its advantages like efficiency and power. The total harmonic distortion (THD) is a critical factor in audio, communication, and power systems, it is one of the parameters used to determine how much voltage and current distortion is caused by the signal's harmonics[10]. Since the output voltage levels are amplified in a multilevel inverter, lower-order harmonics can be decreased which reduces the cost of the filter. [1-4].

Multi-level inverters are mainly categorized into three types. [6,7] diode clamped inverter (DCI), flying capacitor (FCI), and cascaded H bridge(CHB) inverter, out of these three inverters it is proved that CHB multilevel inverter topology is made up of a collection of power conversion cells that can be scaled easily. This topology also provides fewer harmonics, better efficiency, and less switching losses compared to the DCI and FCI topologies [1,2]. Despite the benefits listed above, in the case of CHB-MLI, it has been taken into account that the use of anti-parallel diodes results in higher switching and conduction losses. To reduce the switching losses researchers are investigating for reduced switch count multi-level inverters with different topologies,[7,8] and it has been noticed to be difficult due to the advancement of better battery use [9-15].

Contribution of the paper including details

a) In this paper, nine-level CHB and RSC multilevel inverter operation and voltage harmonics were analyzed for various loads.

b) Multi carrier, level-shifted PWM schemes Phase Disposition(PD), Alternate Phase Opposition Disposition(APOD), Phase Opposition Disposition(POD) are implemented for CHB topology, to examine voltage and current THD.

c) Reduced switch count nine-level inverter using two five-level T network topologies are analyzed with generalized PWM control scheme.

The left-over portion of the paper is divided as Section 2 includes CHB and RSC-MLI operation. Simulation results & assessment study is provided in Section 3 and 4, the paper conclusion is explained in section 5.

II. SYSTEM DESCRIPTION

2.1 Cascaded H bridge nine level inverter topology:

Among the classical MLI, configurations reported cascaded H bridge MLI is the most popular one. The key merits of the configuration are modularity scalability, uniform device ratings equal utilization of DC sources multi switching redundancy's asymmetric ability, and tolerant ability.

Modularity is the ability of the configuration to be extended to higher values without affecting the device ratings and structure of the connected switching devices. The key reason for the modularity of CHB is, the involvement of the H bridge structure such that the H bridge is the building i.e, each basic unit of CHB MLI. Thus, each building block of CHB MLI involves an H bridge interconnected with an isolated DC voltage source.

Assuming stiff voltage of Vdc across the DC source, each H bridge can 3 levels i.e. (+Vdc), zero (0 volts), and negative (-Vdc).

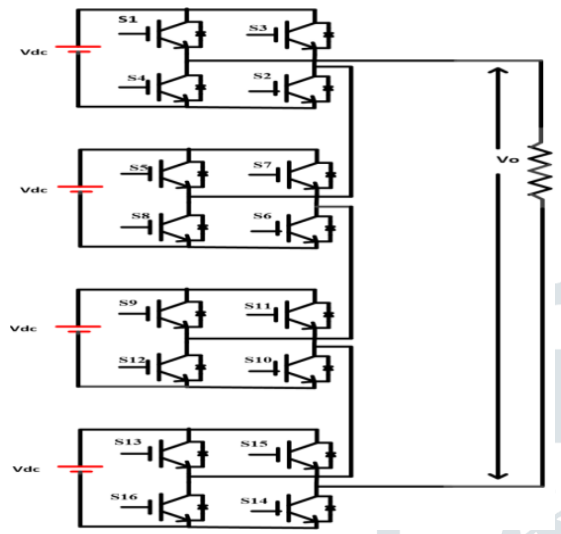


Fig. 1. Nine-level CHB-MLI topology

Table-1 9 Level CHB-MLI Switching conditions √*ON state, X* OFF state

Voltage -Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16
10 V	√	√	X	X	X	√	X	√	X	√	X	√	X	√	X	√
20 V	√	√	X	X	√	√	X	X	X	√	X	√	X	√	X	√
30 V	√	√	X	X	√	√	X	X	√	√	X	X	X	√	X	√
40 V	√	√	X	X	√	√	X	X	√	√	X	X	√	√	X	X
0 V	X	√	X	√	X	√	X	√	X	√	X	√	X	√	X	√
-10 V	X	X	√	√	X	√	X	√	X	√	X	√	X	√	X	√
-20 V	X	X	√	√	X	X	√	√	X	√	X	√	X	√	X	√
-30 V	X	X	√	√	X	X	√	√	X	X	√	√	X	√	X	√
-40 V	X	X	√	√	X	X	√	√	X	X	√	√	X	X	√	√

Table 1: CHB-MLI switching states

In general, per phase structure of CHB with 'n' H-bridges involves 4n unidirectional switches, n numbered isolated DC sources, and produces 2n+1 level in phase voltage.

Assuming symmetrical cascaded connections for n=4, per phase structure of nine level CHB is shown in fig 1. this configuration has the potential to produce the nine-level voltage with the peak value of 4Vdc, operates with the step size of Vdc.

However, it is to be noted that multiple redundancies i.e., alternate switching states available for various positive and negative levels in phase voltages i.e. of 0, Vdc, 2Vdc, and 3Vdc permits the configuration to operate with the convectional level shifted and phase-shifted algorithms.

The reported CHB-MLI working approach is studied with level shifted PWM based on POD, PD, APOD modulations [5]. The sinusoidal reference signal is of amplitude 1 with required output frequency is compared with eight triangle (carrier) signals, where these carrier signal minimum and maximum values depends on the number of output voltage level. For 'n' level inverter, (n-1) triangle signals are required and its minimum to maximum level difference is 1/((n-1)/2) considering that reference signal peak magnitude is one.

In phase disposition all carrier signals are in phase. In POD scheme, all triangle signals and the reference signal both are in phase with an above zero, and are 180^0 out of phase with a reference signal below zero. Where as in APOD all the face-to-face triangle signals are out of phase by 180^0.

2.2 Nine level inverter with reduced switch count (RSC) :

Fig. 2 showed cascaded RSC MLI developed by cascading two five-level T-type configurations . A single T network [14] consists of two stiff dc sources(Vdc1, Vdc2) and six power-switching devices (s1 to s6).

Nine voltage levels can be generated with the cascaded combination of two similar T networks (like CHBMLI), as compared with nine level CHB-MLI four CHBs are connected in cascade, here two T networks are connected in cascade, despite the fact that the number of input voltages needed is the same, this design has the advantage of requiring fewer switching devices, therefore cost of the system and switching losses are less.

In the circuit of Fig. 2 the source voltage magnitudes are equal, and they are Vdc1=Vdc2=Vdc3=Vdc4=10 volts, the number of switching devices are twelve (S1 to S12).

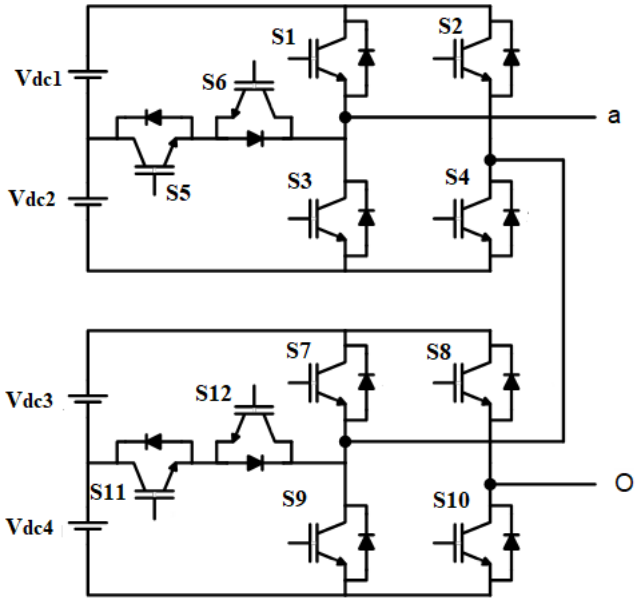


Figure 2. Circuit diagram for 9 level RSC-MLI.

2.2.1 Operating switching modes:

Referring to table 1, it is observed that nine level reduced switch count MLI for any of the nine levels only four controlled switches are conducting i.e from top T network 2 switches and from bottom T network 2 switches, which results in less conduction losses as compared with 9-level CHB network, because in 9 level CHB configuration for any voltage level 8 power switches are conducting.

Table .2: 9 Level RSC-MLI switching conditions √*ON state, χ* OFF state

Voltage - Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
10 V	χ	χ	χ	√	√	χ	√	√	χ	χ	χ	χ
20 V	√	χ	χ	√	χ	χ	√	√	χ	χ	χ	χ
30 V	√	χ	χ	√	χ	χ	χ	χ	χ	√	χ	√
40 V	√	χ	χ	√	χ	χ	√	√	χ	χ	χ	χ
0 V	√	√	χ	χ	χ	χ	√	√	χ	χ	χ	χ
-10 V	χ	√	χ	χ	χ	√	√	√	χ	χ	χ	χ
-20 V	χ	√	√	χ	χ	χ	√	√	χ	χ	χ	χ
-30 V	χ	√	√	χ	χ	χ	χ	√	χ	χ	√	χ
-40 V	χ	√	√	χ	χ	χ	χ	√	√	χ	χ	χ

The conduction path for nine various voltage levels is shown in Fig 3. Considering that all DC link voltage sources are fixed at 10 volts, the maximum and minimum output voltage magnitude is 40 volts. For various loads (resistor and inductor) voltage and current THD are monitored and are listed in table 3.

For better total harmonic distortion, the circuit is realized with the PWM technique. By using the generalized level-shifted reduced carrier technique 9 level-RSC-MLI is producing less THD. This generalized control technique requires half of the controlled voltages as compared with the conventional PWM technique. i.e from the above discussed 9 level inverter, 8 carrier signals for CHB configuration, and 4 for RSC-MLI are used.

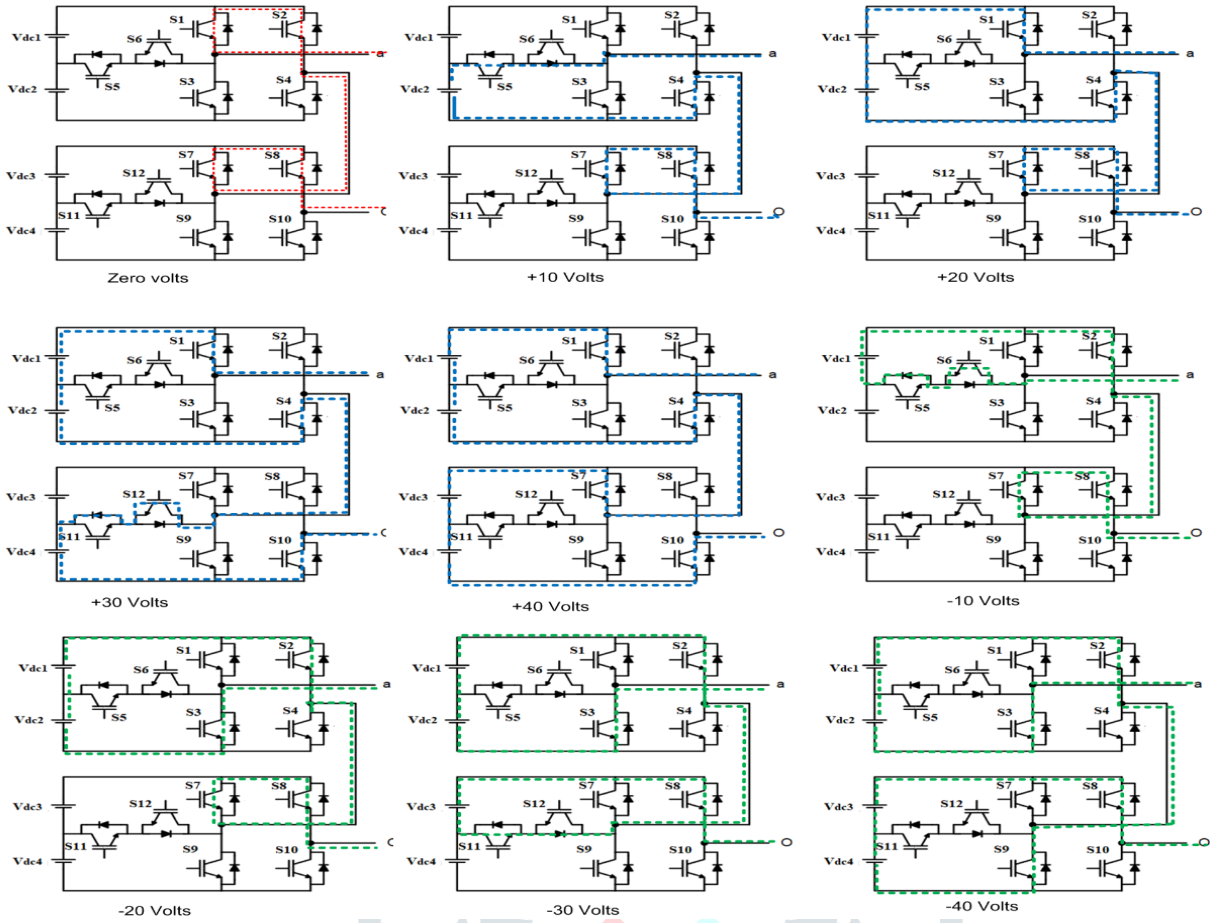


Figure 3. Nine level RSC-MLI operating paths.

III. SIMULATION RESULTS

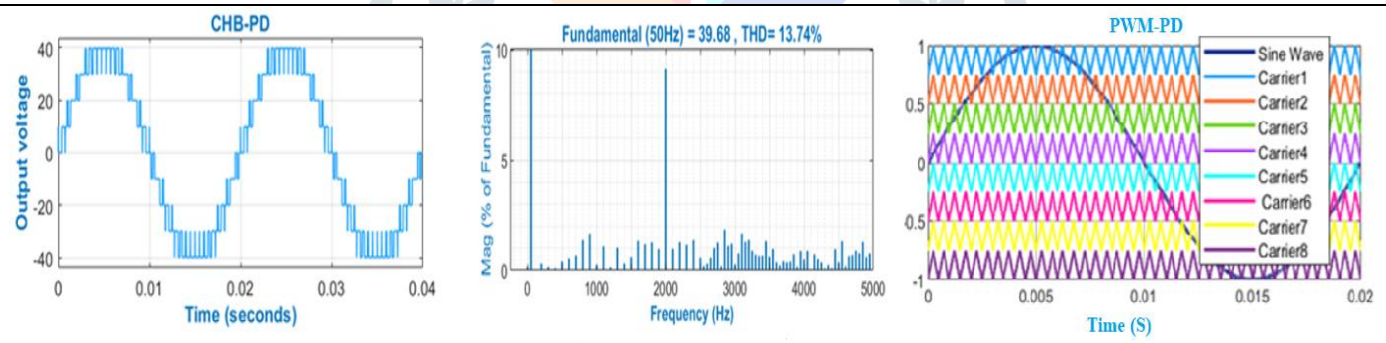


Figure 4a. PD-PWM

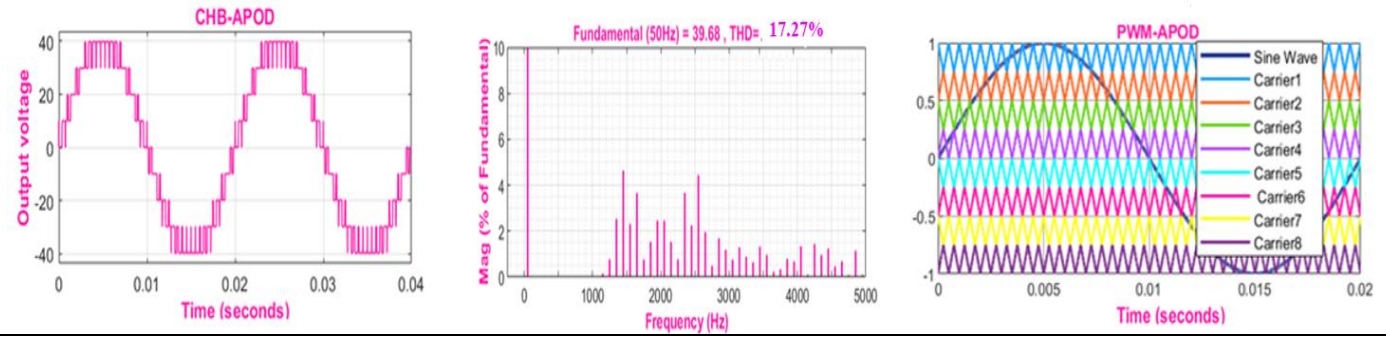
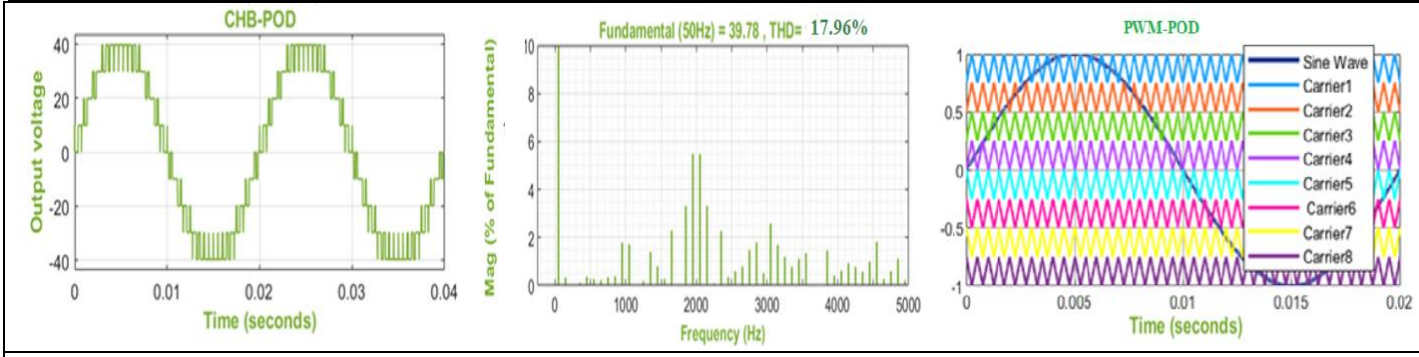


Figure 4b. APOD-PWM



4c.). POD-PWM

Figure 4 Output voltage , carrier arrangement and THD of cascaded 9 level H bridge inverter.

Simulation results for different level-shifted PWM techniques (PD, APOD & POD), total harmonic distortion spectrum, and the respective voltage wave forms are shown in Fig. 4a,4b,4c. Performance expressed in this system as THD for different loads, listed in table 3.

3.1 Simulation of RSC-MLI control circuit :

The block diagram representation of RSC-MLI is shown in Fig. 5, from this it is observed that 12 gate pulses for the inverter switches are generated from the programmable circuit,which depends on PWM control, this control circuit contains modulated sinusoidal signal, four different magnitude carrier signals are compared to generate gate pulses for one cycle of the output,this reference and carrier signals are illustrated in Fig. 6.

Figure 5. Control circuit block diagram

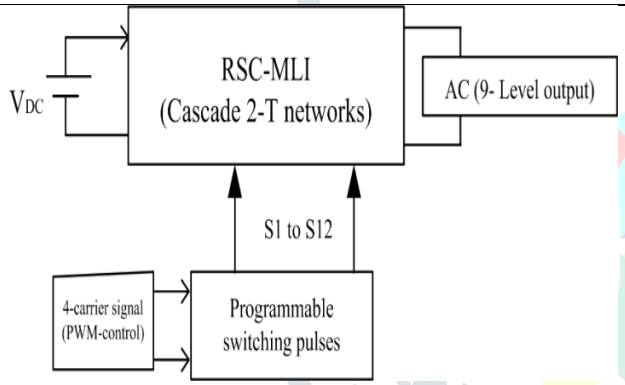


Figure 6. Simulated Reference and carrier signals

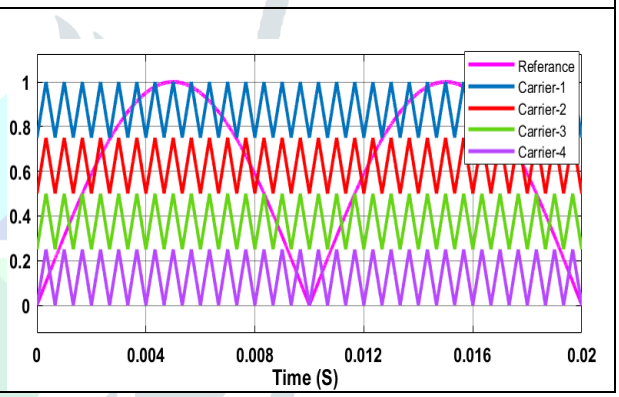
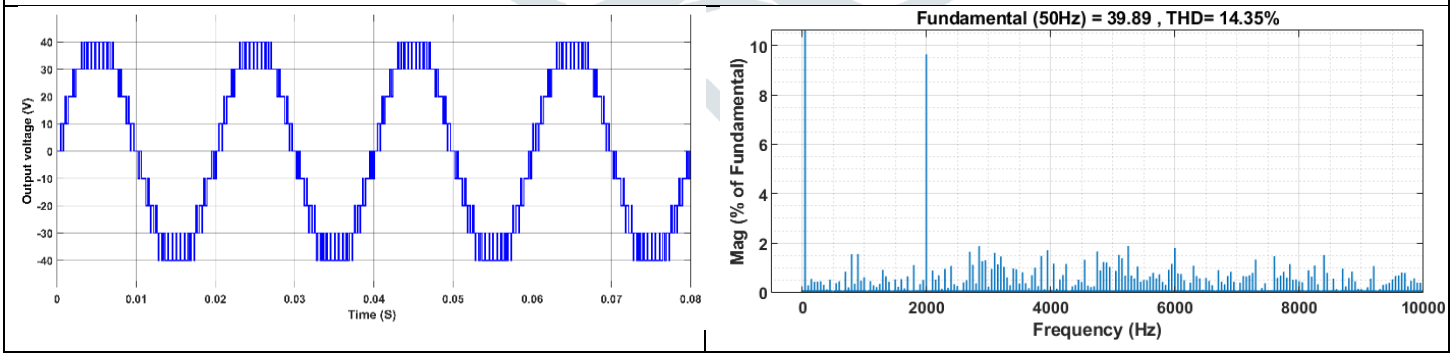


Figure 7. shows the RSC-9 level inverter output voltage waveform and its THD .



LOAD		RSC - MLI		CHB - MLI Voltage THD%			CHB - MLI Current THD%		
RESISTOR (OHM)	INDUCTOR (HENRY)	Voltage-THD%	Current-THD%	PD	POD	APOD	PD	APOD	POD
10	1	17.76	6.97	13.72	17.27	17.96	4.19	9.96	11.7
10	0.1	18.24	2.62	13.72	17.27	17.96	0.45	3.34	3.76
50	10	17.66	6.48	13.72	17.27	17.96	2.68	9.56	12.25
50	0.1	17.02	2.9	13.72	17.27	17.9	0.6	5.2	5.3
100	1	18.29	2.62	13.74	17.28	17.96	0.45	3.71	3.7
100	0.1	16.78	2.41	13.74	17.28	17.96	1.05	11.33	11.8
10	0	14.36	14.36	13.73	17.27	17.96	13.73	17.27	17.96

Table 3: THD performance of RSC,CHB 9level inverter configuration for various control algorithms

IV. *CHB AND RSC - MLI INVERTER COMPARISON RESULT :*

Table 3 gives the THD analysis of presented nine level RSC and CHB 9 level inverter topologies for R and RL loads. Figure 8 compares the outcomes of simulated LSPWM methods using 8 carrier signals for CHB-MLI topology and 4 carrier signals or the reduced carrier PWM control strategy for RSC-MLI architecture. The Reduced carrier approach in RSC-MLI topologies and PD method in CHB topology both produce less THD at output voltage when compared to POD and APOD PWM techniques.

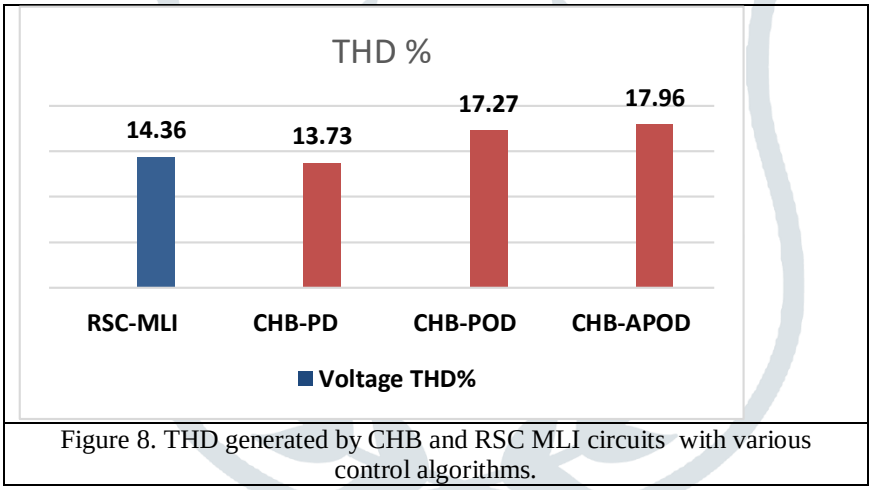


Figure 8. THD generated by CHB and RSC MLI circuits with various control algorithms.

V. *CONCLUSION*

This paper submits the simulation model of two different nine level inverter configurations using various control PWM techniques. The developed nine-level CHB and RSC inverters are studied on basis of the percentage of harmonics in output voltage and current wave forms using LSPWM and reduced carrier PWM techniques respectively. The THD for both inverters are compared for various resistor and inductor loads. The operating principle of the circuit is explained, and a detailed simulation is presented using MATLAB/SIMULINK.

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