Design of Low-Power High-Performance Operational Transconductance Amplifier

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Abstract

The growing demand for smaller and more power-efficient electronic devices has led to a critical need for reducing the size, power consumption, and improving the performance of operational transconductance amplifiers (OTAs). The focus of this work is to address the challenges associated with electronic devices, particularly operational transconductance amplifiers. OTA often consume significant power and occupy large areas, which is undesirable. By employing various low power consumption techniques, the work aims to design and implement a low power, low voltage OTA that offers high gain and improved overall performance. Overall, the work seeks to enhance the design of OTAs by incorporating low power consumption techniques, ultimately leading to better performance in terms of gain, speed, and overall efficiency.

Keywords: Operational Transconductance Amplifier, Optimisation, Gain.

I. Introduction

In response to the growing demand for energy-efficient and portable devices with extended battery life, there is a rising trend towards low power design. Operational Transconductance Amplifiers as shown in Figure 1 have emerged as vital components in modern analog and mixed signal circuits. Unlike operational amplifiers (op-amps) that function as voltage-controlled voltage sources (VCVS), OTAs serve as voltage-controlled current sources (VCCS) by employing a differential amplifier at the input. The primary characteristic of an OTA is its transconductance, which denotes the ratio of output current to input voltage.
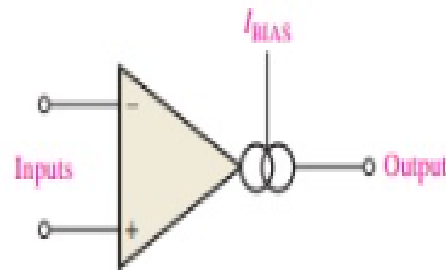

Figure 1: Circuit Symbol of OTA

OTAs are commonly utilized as high impedance differential input stages, enabling precision control of amplifier gain or filter frequency over a wide range. Their unique feature is the ability to operate in both open-loop configurations without negative feedback and closed-loop configurations with negative feedback, making them versatile in linear applications. Furthermore, the OTA's high output impedance, when combined with an output buffer amplifier, allows for the conversion of the OTA's current output into voltage, transforming it into a functional operational amplifier.

This work aims to explore the field of operational transconductance amplifiers and examine different low-power enhancement techniques. Section 2 will delve into prior research conducted on OTAs, while Section 3 will focus on the circuit implementation of conventional two-stage double-input and fully differential OTAs, providing an analysis based on a 180nm channel length.

II. Related Work

The operational transconductance amplifier is a widely used amplifier type in analog and switching applications, particularly in low power amplifiers. Researchers have focused on understanding the concepts and challenges related to OTA design, and several studies have contributed to this field.

In [2], authors proposed different architectures for OTA and explored power enhancement techniques. For instance, the Telescopic Cascode configuration offers high gain and bandwidth with reduced power consumption, albeit with a potential signal swing degradation. Another study [3] discussed power minimization techniques for CMOS, highlighting the issues of leakage in submicron scaling processes.

In reference [4], a DTMOS OTA model was proposed and compared with conventional OTAs. The research specifically used a channel length of 180nm. Reference [5] presented the design and analysis of two low-voltage, low-power OTAs using the DTMOS (Dynamic threshold MOSFET) technique. One OTA design employed a two-stage architecture, while the other utilized a current mirror configuration.

Reference [6] summarized the findings, emphasizing a high-performance three-stage single-Miller CMOS OTA that eliminates the upper limit of load capacitance (CL). This flexibility allows for greater versatility in circuit design. The paper discussed the potential impact of this OTA in various applications and highlighted the need for further research and advancements in the field.

These references provide valuable insights into the design, optimization, and performance evaluation of DTMOS OTA. It presents different techniques and approaches to achieve desirable characteristics such as high slew rate, low power consumption, and overall performance improvement in OTA designs.

III. Implementation

The implementation of a conventional OTA typically involves several key components and design considerations. The OTA usually begins with a differential input stage, which consists of two input transistors M6, M7 as shown in Figure 2, configured in a differential pair arrangement. This stage helps provide a balanced and linear response to differential input signals, another circuit i.e., transistors M9-M11, M10-M12, and M8-M5 are the current mirror.

A current mirror circuit is often used to replicate the current from the differential input stage. It ensures that the current flowing through the output stage matches the current in the input stage, enabling accurate amplification, another important factor is the gain stage and biasing circuitry, The gain stage is responsible for amplifying the input signal.

It typically consists of one or more amplifier stages, such as common-source or cascode amplifiers, to achieve the desired gain. Biasing is crucial for setting the operating point and ensuring stable operation of the OTA. It involves the generation of suitable bias currents and voltages to bias the transistors within their desired regions of operation.

Now coming to the output stage, the output stage converts the amplified voltage signal into a corresponding current output. Commonly used output stages include the common-drain or source follower configuration, which provides low output impedance and voltage gain close to unity. Some compensation techniques are employed to maintain stability and prevent oscillations in the OTA. This may involve the use of compensation capacitors and resistors to achieve the desired frequency response and phase margin.

The specific implementation details and circuit topologies can vary depending on the desired performance requirements, technology used (such as CMOS, bipolar), and the target application of the OTA. It's important to consider factors such as gain, bandwidth, slew rate, power consumption, and noise in the design process. The output voltage of an ideal OTA is a product of the output current and the load resistance. Hence, the voltage gain on the output is a product of the load resistance and the transconductance of the OTA. The transconductance is directly proportional to an amplifier bias current, which is used to control the transconductance.
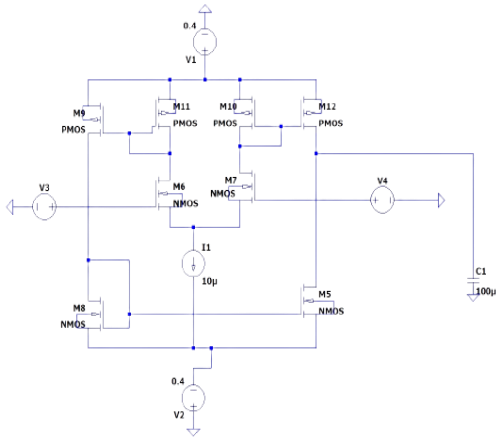
Figure 2: Circuit Diagram of Conventional OTA

The implementation of DTMOS in an OTA involves incorporating DTMOS transistors into the circuitry as shown in Figure 4. DTMOS is a technique that utilizes transistors with dynamically adjustable threshold voltages to optimize the performance of the OTA. To cope with the challenges arising from reducing the supply voltage, a highly efficient DTMOS technique for supply voltage scaling is implemented in this context.
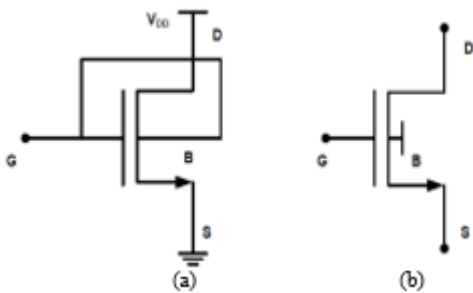

Figure 3: DTMOS technique based (a) NMOS transistor (b) Symbol

This technique involves connecting the body of a DTMOS transistor to its gate terminal, as depicted in Figure 3 [7, 8]. By employing this technique, it offers exceptional benefits such as significantly high transconductance, minimized parasitic capacitance, and remarkable current driving capability even when operating under very low supply voltages, below ± 0.6 V.

From Figure 3(a), An observation reveals that as the gate voltage V_{GS} of a DTMOS transistor increases, there is a corresponding increase in the source-to-body voltage V_{SB}, resulting in a decrease in the threshold voltage V_{TH} as indicated in Equation 1.

$$V_{TH} = V_{TH0} + \gamma(\sqrt{2\,|\phi_F| - V_{SB}} - \sqrt{|2\phi_F|}) \qquad (1)$$

Where V_{TH0} is zero body bias threshold voltage, γ is the body effect coefficient, and ϕ_F is the surface potential at threshold its value is $|-2\phi_F|$. Though, increment in V_{SB} must be limited by the value of $2|\phi_F|$, to uphold the negligible leakage current. But when V_{SB} is equal to $2|\phi_F|$ then it gives the minimum threshold voltage $V_{TH,min}$ as shown in Equation 2.

$$V_{TH,min} = 2|\phi_F| + V_{FB} \qquad (2)$$

The decrease in threshold voltage V_{TH} due to this change turns on the DTMOS device and enhances the mobility of the charge carriers. As a result, the output current and transconductance of the device increase. This increase in transconductance leads to a suitable improvement in the transistor's bandwidth. Equation 3 gives the DTMOS transconductance.

$$G_{md} = g_m + g_{mb} \qquad (3)$$

where g_m and g_{mb} are the gate and body transconductance of the conventional MOS transistor.

Consequently, it is particularly well-suited for low voltage operations, effectively addressing the complexity and performance degradation issues associated with reduced supply voltage. This feature allows for enhanced performance and flexibility in the OTA design. Efficient biasing techniques are crucial for DTMOS OTA implementation. These techniques ensure that the DTMOS transistors operate in their desired regions and maintain proper bias conditions. Common biasing techniques, such as current mirrors or biasing networks, are employed to generate the necessary bias currents and voltages. Similar to conventional OTAs, DTMOS OTAs often start with a differential input stage consisting of DTMOS transistors in a differential pair configuration. These transistors provide the desired input differential voltage response. Coming to the gain stage and output stage the gain stage amplifies the input signal and typically incorporates DTMOS transistors. Various amplifier configurations, such as common-source or cascode amplifiers, can be used to achieve the desired gain and performance and the output stage of a DTMOS OTA can use DTMOS transistors in configurations like common-drain or source follower.

The choice of the output stage depends on the desired output impedance and voltage gain.

It's important to note that the specific implementation details of DTMOS OTAs can vary depending on the design requirements, process technology, and target application. To further enhance the slew rate of DTMOS OTA, an additional slew rate enhancement circuit consisting of transistors M1, M2, M3, M4, M13, M14 has been employed to improve the large signal response of the DTMOS OTA as shown in figure 5.
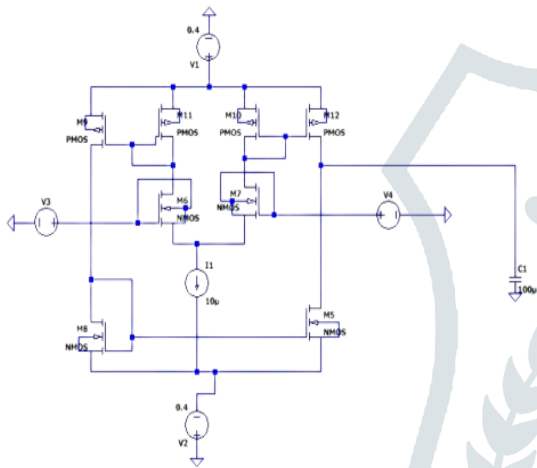

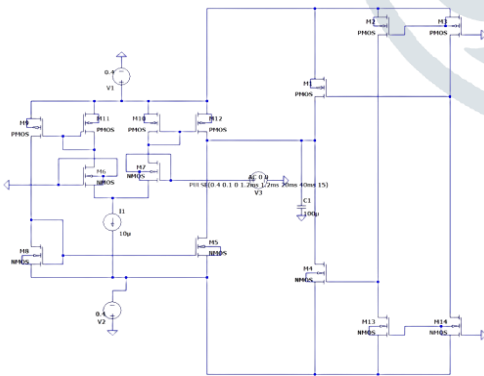Figure 4: Circuit Diagram of DTMOS OTA

Figure 5: Circuit Diagram of DTMOS OTA with slew rate enhancement circuit

IV. Simulation Results

The detailed circuit simulations have been carried out to achieve the desired performance parameters such as high slew rate, high gain with low power consumption, and optimised performance. To examine its performance of conventional OTA, DTMOS OTA and DTMOS OTA with slew rate enhancement circuit, the AC, DC, and transient analysis has been performed with ±0.4V power supply and 180nm CMOS technology. Table 1 shows the simulation results of different OTAs which illustrates that the gain obtained of the DTMOS OTA is 77.69dB which is higher as compared to bulk driven OTA and conventional OTA by respectively. It is also illustrated that the gain-bandwidth product (GBW) obtained of the DTMOS OTA is 1136MHz which is higher as compared to bulk driven OTA and conventional OTA by respectively.

Table 1: Simulation Results of Different OTAs

Parameters	Conventional OTA	Bulk Driven	Proposed OTA
Technology	180 nm	180 nm	180 nm
Linearity	0.21 V	0.28 V	0.23 V
I bias	10 uA	10 uA	10 uA
Supply Voltage	±0.4 V	±0.4 V	±0.4 V
Gain	62.36 dB	64.4 dB	77.69 dB
GBW	595MHz	966 MHz	1136 MHz
Phase Margin	85 °	150 °	104 °
THD	-195 dB	-220 dB	-180 dB

Slew rate was also calculated for the given circuits and is presented in tabular form below:

Table 2: Calculated Slew Rate of Different OTAs

Parameters	Conventional OTA	OTA without Enhancement Technique	OTA with Enhancement Technique
SR+	109.3 V/us	105.8 V/us	294.4 V/us
SR-	173.9 V/us	173.5 V/us	296.4 V/us

Table 2 shows the simulation results of different OTAs which illustrates that the slew rate obtained of the Enhanced DTMOS OTA is 294.4 V/us which is higher as compared to bulk driven OTA and conventional OTA by respectively.

V. Conclusion

The proposed work on DTMOS in the context of OTAs showcases several notable advantages. From the simulation results, it can be concluded that there is a significant increase of 24.58% and 20.6% in gain as compared to conventional OTA and bulk driven respectively. Moreover, there is a significant increase of 90.92% and 17.59% in GBW as compared to conventional OTA and bulk driven respectively. The slew rate of the OTA with enhancement technique is increased by 178.2% as compared to the OTA without enhancement technique. It leverages the inherent benefits of DTMOS technology, including improved linearity, higher gain, higher slew rate with low-power consumption which shows that the proposed OTA is suitable for low power analog and mix signal applications.

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