JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

Design of a New Reversible Full Adder using MCT and MCF Reversible Gates.

K. Saritha Raj[1], Dr. M. Satyanarayana[2], Dr. P. Rajesh Kumar[3]
[1]*Department of ECE, JNTU-Kakinada, India.*
[2]*Department of ECE, MVGR College of Engineering-Vizianagaram, India.*
[3]*Department of ECE, Andhra University College of Engineering-Visakhapatnam, India.*

Abstract: *Reversible Gates (RGs) have always been an attraction for most digital circuit designers for their numerous advantages in providing high speed, low power dissipation and reduced chip area. Most recent applications include designing larger circuits like 16/32-bit adders, multipliers, ALUs, registers, decoders etc. RGs provide a wide range of flexibility in designing new types of reversible logic circuits. The common reversible gates can be modified easily to be accommodated into the required circuit design. The design presented in this paper is a new reversible full adder circuit which uses Multiple Control Toffoli (MCT) and Multiple Control Fredkin (MCF) reversible gates. This proposed circuit is compared with the existing designs of full adder circuits in terms of various performance parameters like the Gate Count, Transistor Count, Ancilla Input, Garbage Output, Quantum Cost and Power dissipation. When compared with the existing designs, this new reversible full adder proves to have the least power dissipation with a slight compromise on Quantum cost. Hence this circuit is the best option to be used in the implementation of larger circuits like multipliers.*

Index Terms: **Multiple Control Toffoli gate, Multiple Control Fredkin gate, Ancilla Input, Garbage Output, Quantum Cost.**

1. INTRODUCTION

The phenomenal growth in the electronic industry over the past few decades is mainly due to the technical advancements in VLSI design methods. The cutting-edge technologies of the present day, namely, the high-resolution videos with low bit-rate, cellular communications, quantum computing, DNA technology, optical computing, DSP applications and nanotechnology need minimum processing power, low area (portable circuits) and high-speed circuits. Moore stated that, there would be a dramatic increase in the number of components on a single chip, which approximately would double for every 18 months. This statement made the researchers to deduce the fact that, the greater the number of components on a single chip the more is the power dissipation associated with the digital circuits. In this context, we shall consider the findings of R. Landauer, who demonstrated that with the loss of each bit of information there shall be a marginal amount of energy loss. This energy loss escapes as heat into the environment. Landauer proved that this loss of energy is equal to (KTln2) Joules which is dissipated as heat, where T (absolute room temperature) and K (Boltzmann constant) = 1.38×10^{-23} J/K. Considering room temperature of 300K, the heat dissipation would be approximately 2.9×10^{-21} J, which is noticeable. In VLSI circuits, there is high amount of power dissipation due to rapid internal signal switching. Therefore, in implementing the digital circuits, the reversible logic gates proved to be of great advantage, because they can achieve zero power dissipation in logic circuits if it is a reversible circuit. Moreover, the design of digital circuits using reversible gates will ensure that there is no information loss in the circuit. Subsequently, it is evident that the fundamental issue for VLSI circuits is power dissipation, as heat is dissipated during logical operations.

RGs are those gates which produce unique outputs for each set of unique inputs. A gate is said to be reversible if, for each individual distinct input there is a distinct output assigned. Hence, a reversible logic gate must possess equal number of inputs and outputs. In the case of irreversible gates like NAND, NOR etc, the circuits do not map the inputs uniquely to the outputs. Hence, they result in loss of information which in turn results in loss of energy irrespective of the circuit that they realise. The methods used to realise irreversible circuits cannot be applied to realise reversible circuits. This proves to be the reason for having different algorithms to realise the reversible gates. Reversible computing is an innovative method employed for the design of low power VLSI circuits in the fields of cryptography and thermodynamics. Our main focus is to minimise the power dissipation by totally eliminating the information loss.

The recent advancements in higher-level integration and fabrication processes have paved way to better logic circuits, thereby, drastically reducing the energy loss during the last few decades. This trend of heat reduction during computations has its physical limit as stated by R. Landauer. He proved that in all irreversible digital circuits, every bit erasure resulted in energy loss as had been discussed earlier. Conventional digital systems have information loss due to loss of bits during logic operations which results in appreciable amount of power loss. The reversible computations minimise the probability of information loss by preserving the output bits of the circuit. We may note that, the energy dissipation can be zero if a system returns to its initial state irrespective of the number of states that it traversed in between. It

is very important for every reversible gate to be both physically and logically reversible. Note that, during the logical operations, heat is dissipated. Hence, we can deduce that the power dissipation is the most important issue for circuit analysis.

2. REVERSIBLE GATES

This section deals with the advantages and disadvantages of RGs, the performance metrics of RGs and elaborates the various types of RGs

2.1 MERITS AND DEMERITS OF REVERSIBLE GATES

The following may be summarised as the advantages of Reversible Gates:

- There is no loss of information in Reversible logic gates.
- Reversible logic gates have high speed, and low power dissipation.
- They can be modified into many variants and used.
- They are very flexible.
- Any function can be realised using reversible gates.
- Zero power dissipation is possible in logic circuits which use reversible logic gates.

The advantages of Reversible gates are, reduced chip area, improved power dissipation and reduced timing delay such that they can be frequently used as basic building blocks in the construction of larger circuits like multipliers, ALUs, decoders and registers.

The only limitations of reversible circuits are, fan out is not possible and the feedback from gate outputs to inputs is not permitted (Fan-out defines the maximum number of digital inputs that can be fed by the output of a single logic gate). Yet, an irreversible gate can be modified to a reversible gate by making certain modifications. The following are the characteristics for any gate to become a reversible gate:

- Make both the number of inputs and outputs equal.
- Use minimum number of input constants.
- Minimize the garbage outputs.
- Feedback is not allowed in reversible logic.
- Reversible logic gates do not allow fan-out.
- Minimize the number of reversible gates used.

2.2 PERFORMANCE METRICS OF AN RG:

The following are important terminology associated with the performance parameters of a reversible logic design. They are:

- Ancilla inputs
- Garbage output
- Gate count and
- Quantum cost

Ancilla Inputs (AI): The constant inputs appended to convert the design into reversible circuit are called ancilla inputs. They also refer to the total number input terminals being set to a constant value of 0 or 1 to acquire the prerequisite function.

Garbage Output (GO): The extra outputs that are included to maintain the reversibility of the gate are called garbage output. These outputs are not used for any further computations. Hence, large number of garbage outputs should be avoided in a reversible circuit.

Gate count (GC): Gate Count is the number of reversible logic gates used that are used to implement a design.

Quantum Cost (QC): Quantum Cost of a gate refers to the number of primitive gates i.e 1*1 and 2*2 gates that are essential for the computation of the reversible circuit.

The performance of an RG is measured based on the efficiency of the design using reversibility concept. This performance is assessed by optimizing these performance metrics. Ideally, a reversible gate that is used to synthesize a logic circuit, should have the following features:

- Least GO;
- Least AI;
- Least GC.

Minimizing these parameters becomes the basis of any innovative work using reversible circuit design.

2.3 TYPES OF REVERSIBLE GATES

There are different types of Reversible gates. They are:

(i) Fredkin Gate(FRG)
(ii) Feynman Gate(FG)
(iii) Toffoli Gate(TG)
(iv) Peres Gate(PG)

Fredkin Gate: FRG is a 3 input-3 output reversible logic gate which is also known as Controlled SWAP(CSWAP) gate. The figure 1 shows that the input A is mapped directly to the output P. If the input A is set at constant 0, then B is mapped directly to Q and C is mapped to output R. If A is set at constant value 1, then swap operation happens and B gets mapped to R, and C is mapped to Q.

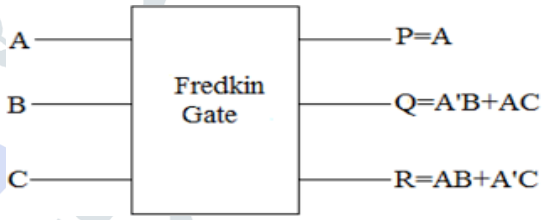


Figure 1.

Feynman gate: FG is a 2x2 reversible gate, also known as Controlled-Not gate (l-CNOT). The first input (A) is used to control the second input (B) as shown in the figure 2. If one input is "0" then 2x2 Feynman gate can be used to duplicate the input.

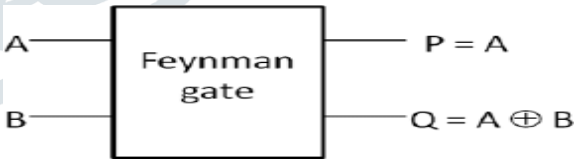


Figure 2.

Toffoli gate: The other name for TG is Controlled- Controlled - Not (CCNOT) gate. It is a universal RGs designed by Tommaso Toffoli. Any type of reversible circuit can be deigned using RGs. It has 3I/p and 3O/p. When the initial two input bits are both assigned to 1, the third bit is inverted; otherwise, all bits remain unchanged. This gate passes the first two inputs to output unchanged (as control signals) and inverts the last input (as target signal). A 3x3 Toffoli gate is depicted in figure 3. Toffoli gates are very important cells in reversible circuits. Most reversible logic synthesis methods use *nxn* Toffoli gates. The main reason for success of Toffoli gates over the other gates is their completeness and relativeness in using them.

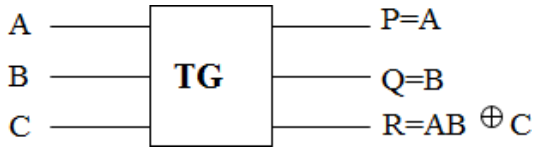


Figure 3.

Peres gate: A New Toffoli Gate (NTG) which combines one Toffoli gate and one Feynman gate is designed and is called as PG. It is a 3x3 reversible logic gate. The PG is used everywhere in place of the Toffoli gate as the latter is expensive gate. A 3x3 Peres gate can work like a half-adder when its third input is a constant at 0.

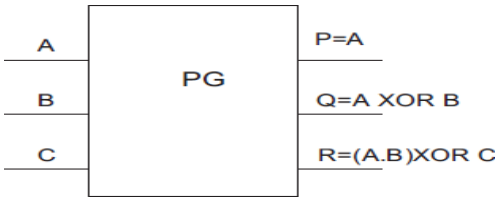


Figure 4.

The quantum cost of frequently used R G s are given below in table 1:

Table 1

Gate	Quantum Cost
Fredkin	5
Feynman	1
Toffoli	5
Peres	4

The above discussed reversible gates are few basic ones. Many new types of reversible gates can be designed with the modifications of the existing ones or by using a combination of two or more reversible gates.

3. LITERATURE SURVEY

Jagadeesh Pujar *et al.*[11], proposed a new Reversible Full Adder(RFA) circuit design using two Feynman Gates in Stage 1 and one Feynman Gate in Stage 2 and one Fredkin Gate in Stage 3 as shown in figure 5.

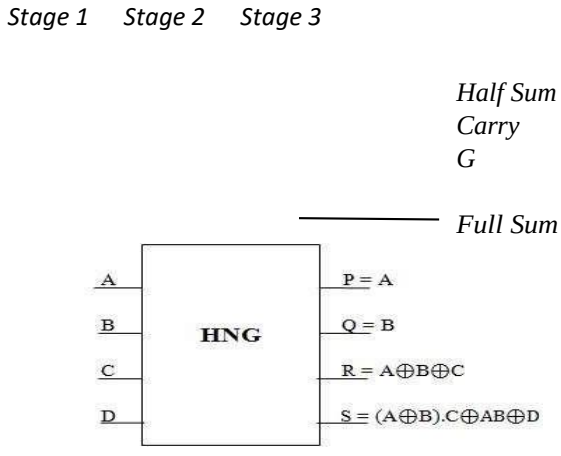


Figure 5.

Sujata S,Chiwande *et al.*[9], presented the implementation of a another type of RFA circuit which uses two Peres gates to generate output Sum and Carry. This circuit has four inputs (P, Q, 0, & Cin) and fouroutputs (G1, G2, Sum, and Cout).

The circuit diagram of this Reversible Full Adder is given below in figure 6. This Peres gate based full-adder according to [9] produces less garbage compared to the Conventional Full Adder circuit using NAND gates as proved and stated in [9]. We can create exceptionally large reversible systems by using a Peres fulladder.

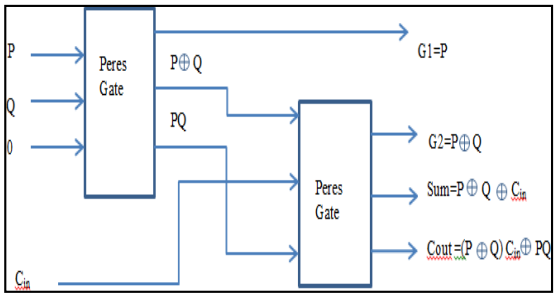


Figure 6.

The RTL view of this proposed circuit is:

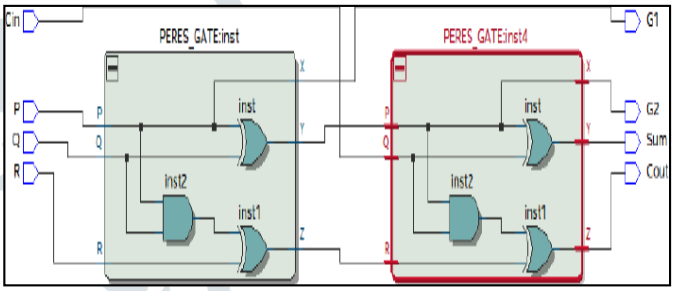
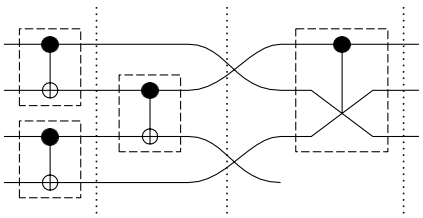


Figure 7.

From the given RTL view of the proposed circuit, the internal diagram of each Peres Gate can be seen, which consists of two OR gates and one AND gate. The advantage of this circuit is that it produces less garbage output.

Jagannatha KB *et al.* [12] proposed a 4-bit Reversible Full Adder/Subtractor(RFA/S) circuit which comprises of four Feynman Gates and four HNG gates. When compared to the normal adder/ subtractor circuit implemented using the irreversible gates, this RFA/S proved to be better in terms of delay and power dissipation. However, it has a drawback of too many garbage outputs, which tends to increase the power dissipation when the number of bits increase.



The Hybrid New Gate (HNG gate) in figure 8 is a universal reversible gate which can realise all types of Boolean functions.

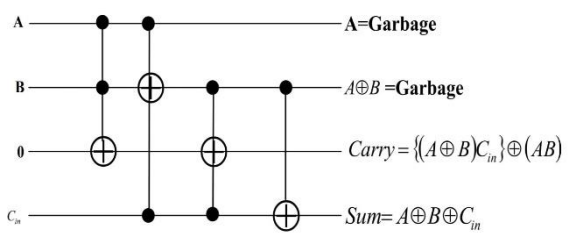


Figure 8.

The given HNG gate can also be used to work as a Reversible Full Adder(RFA) when operated singly. To make this gate work like a Full Adder, the fourth input must be a constant input at 0 i.e D=0. The Quantum Cost of HNG gate is 6.

The 4-bit Reversible Adder/Subtractor circuit design given below in figure 9 which shows that four FGs and four HNGs are required.

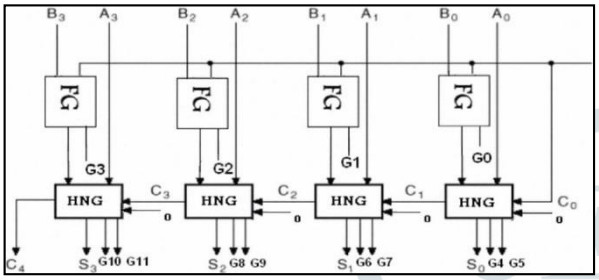


Figure 9.

Gowthami.P et. al[10] showed that a single 4x4 HNG gate itself can work as a RFA. In order to ensure the HNG gate works like a full adder, the fourth input should be a constant input. The advantage of this gate compared to [9] is that it requires only one HNG gate whereas in [9] it requires two Peres gates. Therefore, the QC of [10] is 6 while that of [9] is 8.

4. PROPOSED REVERSIBLE FULL ADDER (RFA)

The proposed RFA is designed utilizing MCT and MCF RGs. This circuit design reduces the complexity of the hardware with higher speed, lower area, and lower power consumption. The proposed design uses two RGs, such as MCT and MCF gates in place of a single reversible gate. It contains additional benefits for reducing the garbage being produced, which helps to reduce the overall delay and power consumed by the RG. All previous designs had conceded to unwanted outputs, unwanted inputs, associated quantum cost of this design as the power dissipation is the greatest merit of this design.

Figure 10.

The performance analysis and comparison of different reversible full adder architectures is given in table 2.

Table 2.

Adder Type	GC	AI	GO	QC	Power Dissipated (μW)
Proposed Reversible Full Adder 2019- [11]	4	1	1	8	12.45
Peres Gate based Full Adder Design 2022-[9]	2	1	2	8	50
4 bit Reversible Full Adder/ Subtractor 2012-[12]	8	5	12	44	6.62
Reversible 16-Bit HNG Ripple Carry Adder 2016-[10]	16	16	32	96	--
Proposed RFA using MCT and MCF	4	1	2	20	0.515

(GC= Gate Count, TC= Transistor Count, AI= Ancilla Input, GO= Garbage Output, QC= Quantum Cost)

4.CONCLUSION AND FUTURE SCOPE

A successful circuit design with optimised power dissipation has been implemented in this paper and compared with various other existing designs. This novel Full Adder circuit was designed using two types of multiple control reversible gates. While using the reversible gates, we can also reduce the delay of the architecture. The future scope of this work is to use this RFA as an adder cell in designing low power circuits like multipliers as has be implemented in designing a Baugh-Wooley Multiplier using Multiple Control Toffoli and Multiple Control Fredkin reversible logic gates.

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