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ANALYSIS OF MINIMAL SWITCH COUNT CASCADED MULTILEVEL INVERTER WITH MODIFIED CARRIER APPROACH FOR POWER QUALITY ENHANCEMENT

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Abstract: Multilevel inverters (MLIs) are essential for achieving superior power quality output and higher power ratings through reduced harmonic distortion. Cascaded multilevel inverters are frequently used because of their ease of manufacture and control. This paper focuses on MLI with minimal switches to attain a lower harmonic distortion with a greater output levels. Even so, the harmonic content can be reduced with the right choice of pulse width modulation (PWM) approaches. The goal is to introduce a new carrier-based PWM control method for a new single phase MLI switches. Better fundamental output voltage and outstanding spectrum quality are obtained from the updated version of Multi Carrier PWM (MCPWM). The main goal is to design a new MCPWM layout by altering the carrier signal which has an M-W shape, is referred to as an M-W PWM technique that generates less distortion of harmonics at low switching frequencies. The suggested novel carrier signal focuses on analyzing its application in a power circuit that functions in both symmetrical and asymmetrical configurations for a decreased MLI. The methodology considers the suggested carrier-based modulation strategy in response to an enhanced output voltage spectrum and uses MATLAB simulation to ascertain performance.

Keywords - Cascaded multilevel inverter, Multi Carrier PWM, Harmonic distortion, M-W PWM technique

1. INTRODUCTION

For medium power applications, the conventional two-level inverter leads to higher switching losses and a high amount of total harmonic distortion [1]. The multilayer inverter was introduced in 1975 [2] as a solution to these problems. The three level inverter introduced the term "multilevel," which has now been expanded to N levels. Typically, a multilevel inverter combines the step voltage waveform from different DC input voltage levels. When compared to a traditional two-level voltage source inverter, the MLI is utilized to lessen harmonic content, electromagnetic interference, and switching losses. It represent applications that vary from medium to high voltage, including applications that involve power quality, strong induction motor drives, etc. It provides a way to raise the working voltage of the inverter beyond the voltage margin of most semiconductor devices [3]. However, it also has disadvantages, such as the need for more switching devices at higher levels, their size, and their cost.

As these MLI topologies are advanced, control along with modulation of these inverters has become more challenging. The stepped voltage that comes out of the inverter contains lower order harmonics, which can cause disoperation and voltage swings, both of which can lower power quality. Therefore, selecting an appropriate modulation strategy is necessary to raise the system's overall performance. THD is mostly influenced by the inverter's level and the switching devices' controlling mechanism. THD can be reduced by using an effective control strategy and raising the inverter's output waveform level. Reduced switches multilevel inverters are being proposed as a solution to the conventional topologies issue.

2. PROPOSED MODULATION TECHNIQUE

The multilayer inverter is the device that uses Multicarrier PWM (MCPWM) approaches which is most frequently employed to generate pulses. Although MCPWM produces minimal harmonic distortion at the load output voltage, there are significant switching losses [5]. The modified carrier signal produced from the high-frequency sinusoidal pulse is displayed in Figure 1. Because the altered carrier signal has an M-W shape, it is referred to as an M-W pulse width modulation (PWM) technique. According to [6], this system also falls within the Multicarrier PWM (MCPWM) approach.

Nonetheless, at high switching frequencies, the THD in MCPWM approaches is lower. This could shorten the devices' lifespan and increase the circuit's switch-related losses. However, the M-W MCPWM approach results in reduced harmonic distortion when switching at a low frequency. It is believed that the reference modulating signal has a sinusoidal fundamental frequency of 50 Hz.

The modified carrier's (fc) frequency is assumed to be 1 kHz. To produce gating pulses for the switches, the M-W shaped signals are contrasted to the modulating sine reference wave.

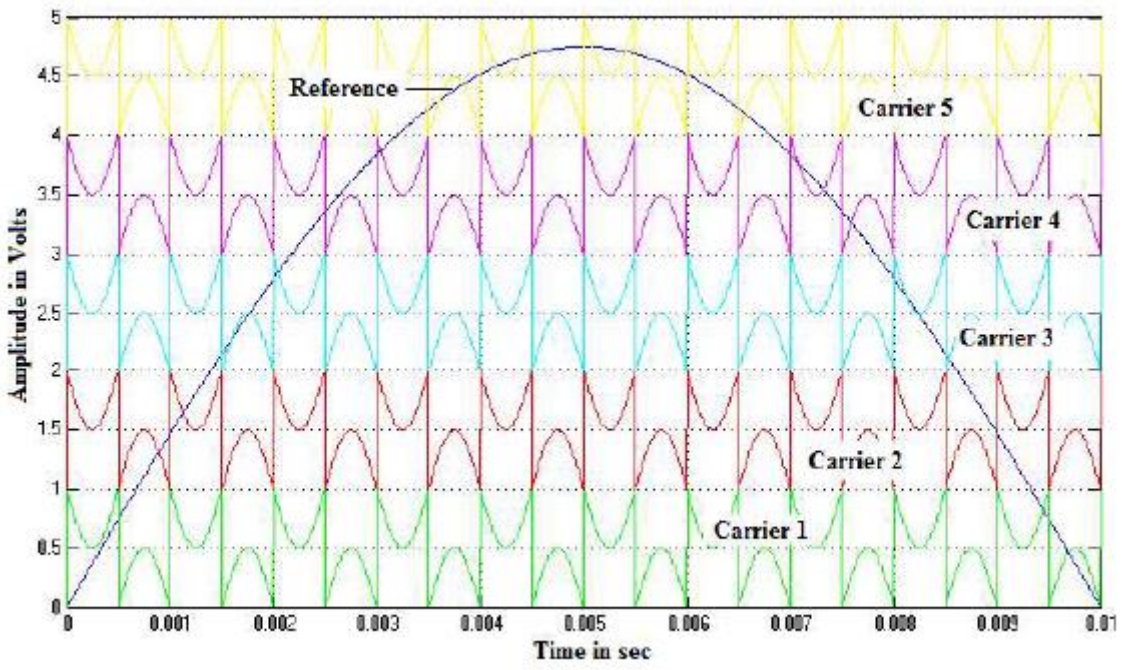


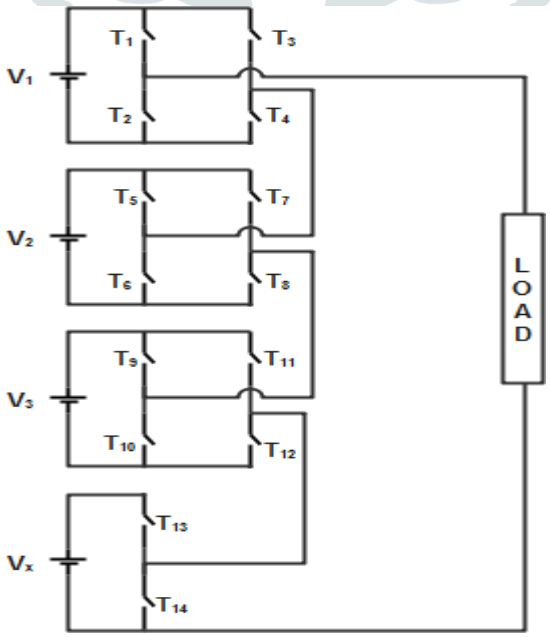
Figure 1 Modified carrier M-W MCPWM technique

3. POWER CIRCUIT

3.1 Symmetrical Operation

Figure 2(a) shows a novel form of MLI, which is made up of nth CHMLI connected in series to a single half-bridge inverter [7-10]. The circuit's output level can be doubled by using a half-bridge (DLC). The DLC approach was not applied, even though the CHMLI structure with half bridge had previously been in place [8]. The primary objective of the DLC is to decrease the quantity of switches along with their voltage rating while simultaneously increasing the output voltage levels to closely double that of the conventional CHMLI output voltage.

With levels of (2n+1), the AC inverter output voltage pattern is generated by the general symmetric CHMLI. The suggested MLI comprising three CHMLI with a half-bridge inverter arrangement is shown in Figure 2(b). Half of the initial source H bridge value in CHMLI is represented by the DC source value in the DLC circuit. The circuit operates symmetrically because the three CHMLI voltage sources have a ratio of 1:1:1. The circuit produces seven output voltage levels in the absence of DLC. The new circuit's output voltage has 13 levels when using DLC. Consequently, in the presence of DLC, the inverter's output voltage doubles.



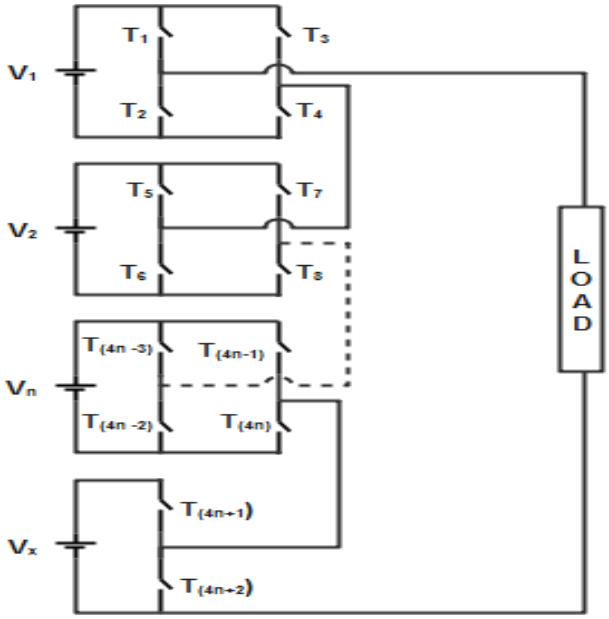


Figure 2 (a) New MLI in a generalized manner (b) New single-phase MLI with three CHMLI and a DLC

Additionally, in the event that CHMLI operates in a symmetric mode, the DC source values is provided by

$$V_1 = V_2 = V_3 = V_4 \dots \dots \dots \dots = V_n = V \quad (1)$$

The suggested MLI's output voltage level is provided as

$$m = (2(2n + 1) - 1) \quad (2)$$

Table 1 provides the switching pattern for the 13 level recommended MLI with DLC. The number of components employed in the standard symmetrical CHMLI and the suggested MLI in symmetrical mode are contrasted in Table 2.

Table 1 Switching sequence for an inverter with thirteen levels

Levels in voltage	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}
V_x		✓		✓		✓		✓		✓		✓	✓	
V_1	✓			✓		✓		✓		✓		✓		✓
(V_1+V_x)	✓			✓		✓		✓		✓		✓	✓	
(V_1+V_2)	✓			✓	✓			✓		✓		✓		✓
$(V_1+V_2+V_x)$	✓			✓	✓			✓		✓		✓	✓	
$(V_1+V_2+V_3)$	✓			✓	✓			✓	✓			✓		✓
0	✓		✓		✓		✓		✓		✓			✓
$-V_1+V_x$		✓	✓			✓		✓		✓		✓	✓	
$-V_1$		✓	✓			✓		✓		✓		✓		✓
$-V_1-V_2+V_x$		✓	✓			✓	✓			✓		✓	✓	
$-V_1-V_2$		✓	✓			✓	✓			✓		✓		✓
$-V_1-V_2-V_3+V_x$		✓	✓			✓	✓			✓	✓		✓	
$-V_1-V_2-V_3$		✓	✓			✓	✓			✓	✓			✓

The DC sources' values for the newly implemented MLI in symmetric manner are provided as

$$V_j = V \quad \text{where } j = 1,2 \dots \dots . . n \quad \text{and} \quad V_x = \frac{V}{2} \quad (3)$$

Table 2 Comparison of a new MLI with CHMLI in symmetrical mode

Multilevel inverter	Symmetrical Mode	
	Cascaded H bridge	New MLI (CHMLI + DLC)
Main switches	2(m-1)	(m-1)+2
Bypass diodes	-	-
Clamping diodes	-	-
DC split capacitor	-	-
Clamping capacitor	-	-
DC sources	(m-1)/2	((m-1)/4)+1

3.2 **Asymmetrical Operation**

With lesser switches, DC sources, as well as driver circuits, a higher number of levels may be reached in the asymmetrical mode of operation. The main benefit of employing asymmetric MLI is that it can produce more levels by eliminating redundant switch configurations for a particular voltage level.

Natural Progression:

In the natural progression, the DC voltage sources have values between 1:2:3 and n. The new DLC circuit can produce 25 levels in the output voltage since it is integrated with the three CHMLI series (3 CHMLI+DLC) in a natural progression.

In the natural progression, the DC voltage source's value is provided as

$$V_j = jV \quad \text{where } j = 1,2 \ldots \ldots n \quad \text{and} \quad V_x = \frac{V_1}{2} \tag{4}$$

In the asymmetrical natural progression, the highest output voltage is expressed as

$$V_{omax} = \left(\frac{n^2+n}{2}\right) V \tag{5}$$

Table 3 Positive switching sequence for a twenty-five level inverter

Levels in voltage (V)	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}	T_{11}	T_{12}	T_{13}	T_{14}
0		✓		✓		✓		✓		✓		✓		✓
0.5		✓		✓		✓		✓		✓		✓	✓	
1.0	✓			✓		✓		✓		✓		✓		✓
1.5	✓			✓		✓		✓		✓		✓	✓	
2.0		✓		✓	✓			✓		✓		✓		✓
2.5		✓		✓	✓			✓		✓		✓	✓	
3.0	✓			✓	✓			✓		✓		✓		✓
3.5	✓			✓	✓			✓		✓		✓	✓	
4.0	✓			✓		✓		✓	✓			✓		✓
4.5	✓			✓		✓		✓	✓			✓	✓	
5.0		✓		✓	✓			✓	✓			✓		✓
5.5		✓		✓	✓			✓	✓			✓	✓	
6.0	✓			✓	✓			✓	✓			✓		✓

Table 3 provides the positive switching pulse sequence for a 25 level inverter. Table 4 contrasts the DC sources, bypass diodes, clamping diodes, and clamping capacitors required for the natural progression of the new MLI's asymmetrical operation with those of the conventional asymmetric CHMLI.

Table 4 Comparison of a new MLI with CHMLI in asymmetrical natural progression mode

Multilevel inverter	Asymmetrical Mode – Natural Progression	
	Cascaded H bridge(without DLC)	New MLI (CHMLI + DLC)
No. of levels	$2 \times \left(\sum_{j=1}^{n} j\right) + 1$	$2 \times \left[2 \times \left(\sum_{j=1}^{n} j\right) + 1\right] - 1$
Main switches	4n	4n+2
Bypass diodes	-	-
Clamping diodes	-	-
DC split capacitor	-	-
Clamping capacitor	-	-
DC sources	n	n+1

4. SIMULATION RESULTS

4.1 Symmetrical operation

The methodology explores the performance of the novel M-W PWM method with ISPWM technique using a suggested MLI with DLC to generate an output voltage with thirteen levels. The power module specification lists half of the full-bridge inverter with a load resistance of 100 ohms, three full-bridge dc sources, every having a voltage of 100V, and a half-bridge DLC circuit voltage of 50V. The output inverter voltage and spectrum analysis for M-W PWM and ISPWM, respectively, with the modulation index of 0.9 at a switching frequency of 1 kHz are shown in Figures 3, 4, 5, and 6.

The comparison of ISPWM and M-W PWM techniques with respect to total harmonic distortion and fundamental output voltage is presented in Table 5. It stated that so as to produce an output voltage with thirteen levels, the two PWM approaches use the identical number of switches with DC sources. Additionally, the inverter output voltage is nearly achieved using the ISPWM method. One of the first techniques to produce less harmonic distortion is the M-W PWM method.

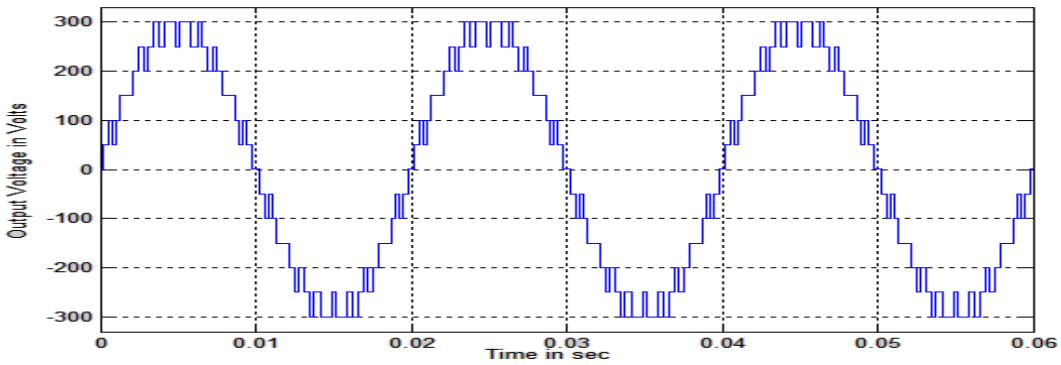


Figure 3 13-level output voltage utilizing the ISPWM approach

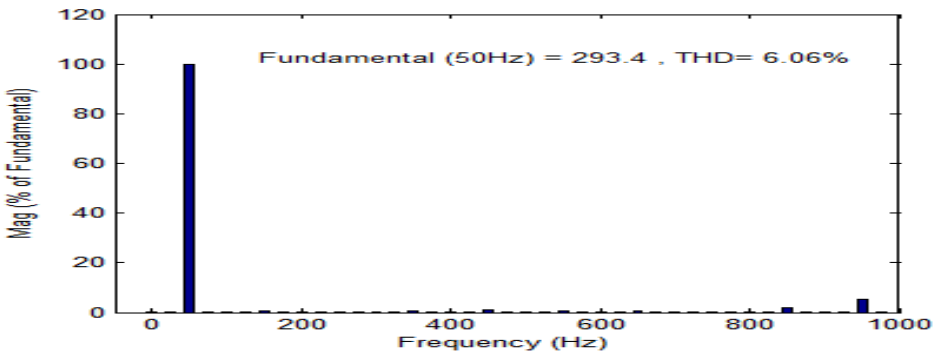


Figure 4 13 level FFT analysis utilizing ISPWM approach

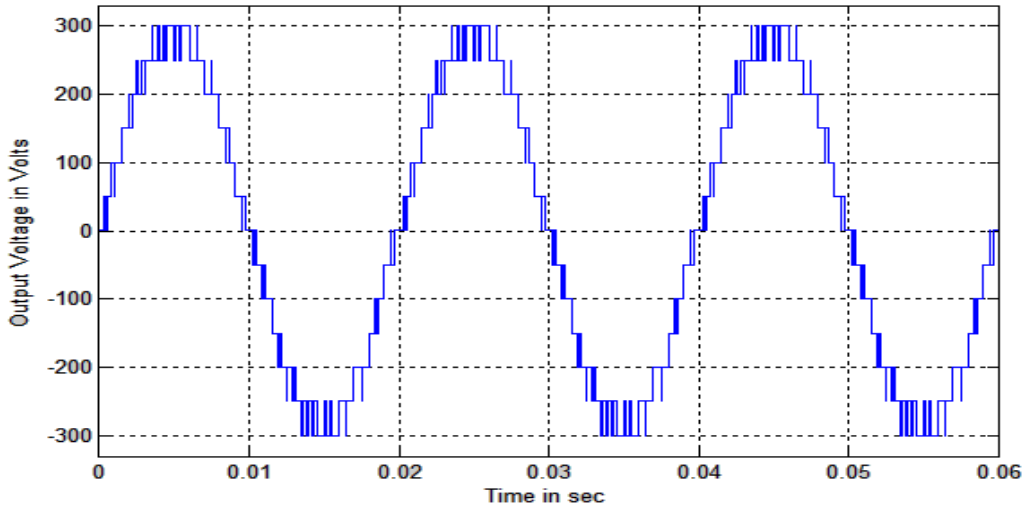


Figure 5 13-level output voltage utilizing the M-W modulation approach

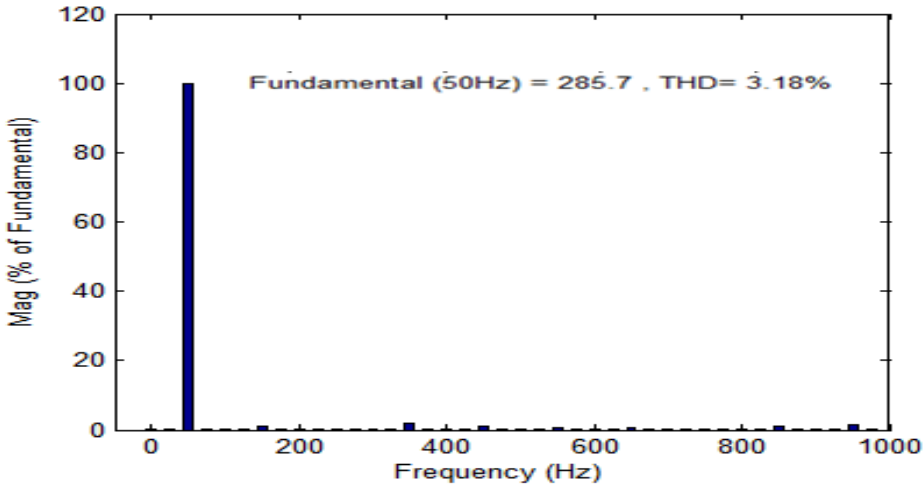


Figure 6 13 level FFT analysis utilizing the M-W modulation approach

Table 5 Comparison of ISPWM and M-W PWM in symmetrical mode

Modulation Techniques	No. of DC sources	No. of Switches	No. of Levels	Inverter Output Voltage (V)	Total Harmonic Distortion (%)
ISPWM	4	14	13	293.4	6.06
M-W PWM	4	14	13	285.7	**3.18**

3.2 Asymmetrical operation

Intending to achieve twenty-five levels in the inverter output, the proposal draws the CHMLI using the DLC circuit in an asymmetrical natural progression with the DC sources in the ratio of (V1:V2: V3) 1: 2: 3. On a MATLAB R2013A platform, the reference frequency is engage to 50 Hz along with the load resistance is set to 100 Ω. To activate the switches with V1 = 100V, V2 = 200V, V3 = 300 V, and Vx = 50V, a carrier frequency of 1 kHz was selected. The load output voltage for ISPWM and M-W PWM techniques is shown along its harmonic spectrum in Figures 7, 8, 9, and 10, respectively.

In an asymmetrical natural progression, Table 6 compares the three CHMLI with a DLC circuit using ISPWM and M-W PWM techniques. For a desired twenty-five level output voltage, it was deduced that the new development in the M-W PWM scheme has resulted in an output with less total harmonic content.

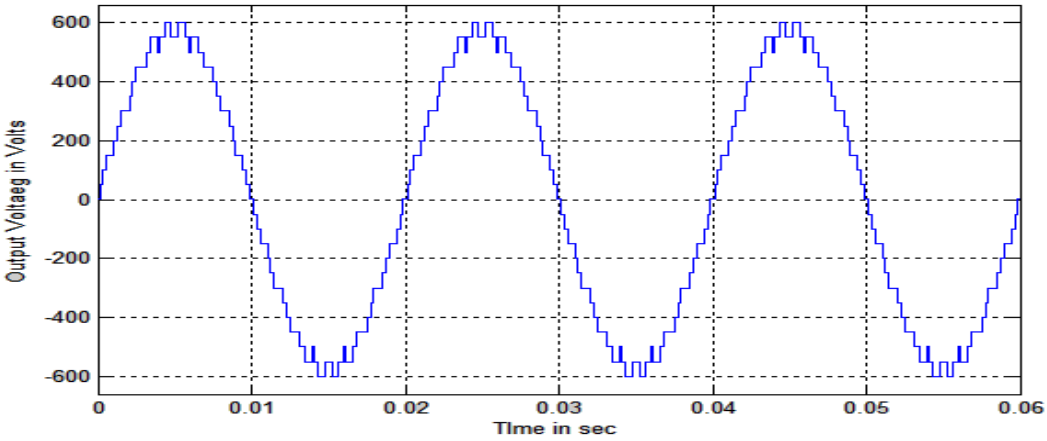


Figure 7 Output voltage for 25 level using ISPWM technique

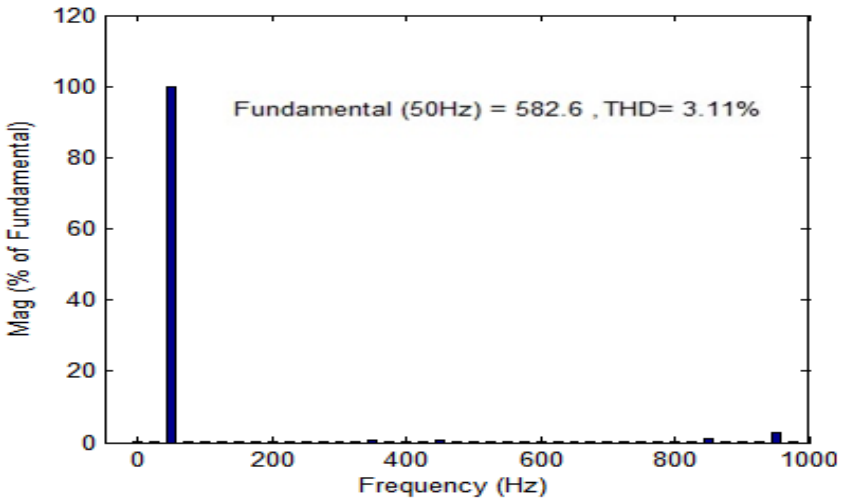


Figure 8 Output voltage for 25 level using ISPWM technique

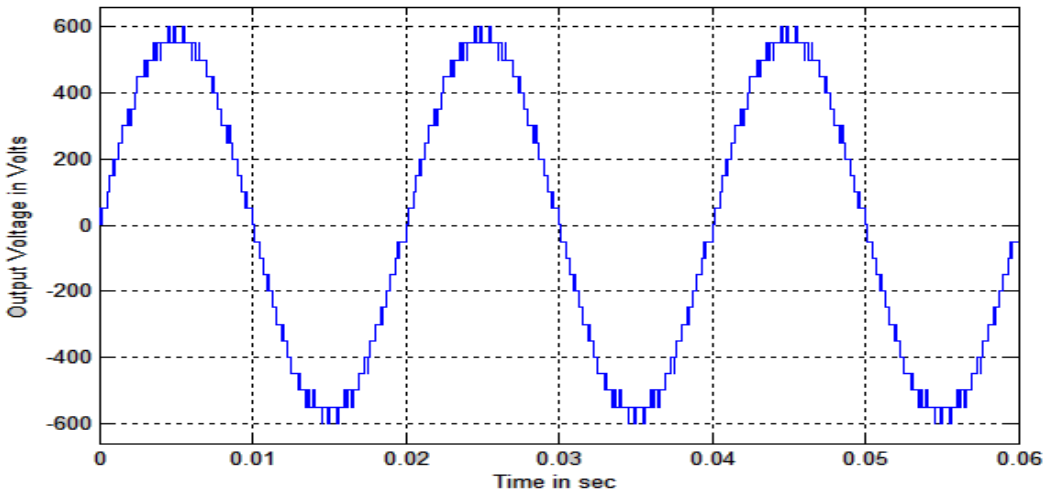


Figure 9 Output voltage for 25 level using M-W modulation technique

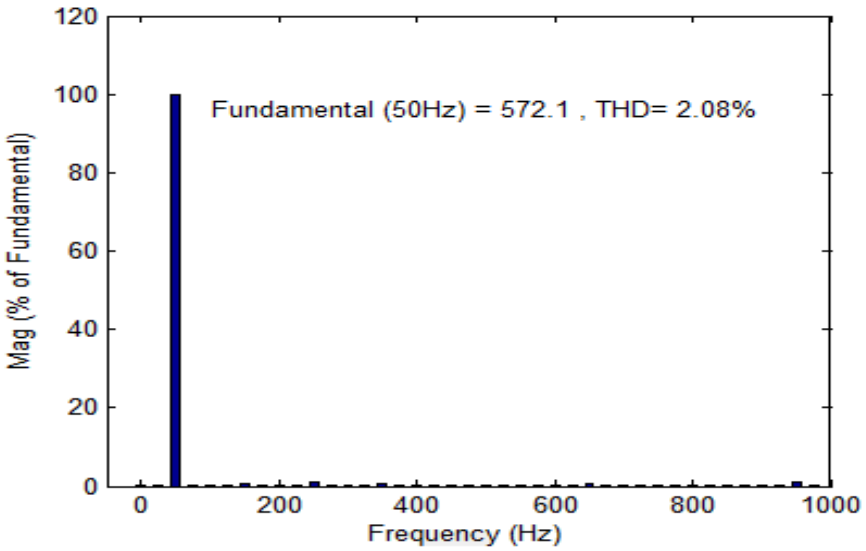


Figure 10 FFT analysis for 25 level using M-W modulation technique

Table 6 Comparison of ISPWM and M-W PWM in asymmetrical natural progression mode

Modulation Techniques	No. of DC sources	No. of Switches	No. of Levels	Inverter Output Voltage (V)	Total Harmonic Distortion (%)
ISPWM	4	14	25	582.6	3.11
M-W PWM	4	14	25	572.1	**2.08**

5. Conclusion

A high-frequency sine wave is employed to provide the pulses that activate the switches in a new H-bridge MLI (CHMLI+DLC) along with a new M-W PWM control strategy has been developed. In contrast to the traditional CHMLI, this requires 12 switches to produce the same output voltage, the new H bridge MLI only needs seven switches in the conduction path per voltage level. Additionally, at low switching frequencies, the control technology's merits can result in low harmonic distortion. Analysis of the outstanding simulation result in both symmetric and asymmetric configurations shows a notable decrease in THD in the inverter output voltage and an increase in the fundamental component. The advantages of the proposal have been demonstrated through the use of comparative results to illustrate the MCPWM techniques.

References

1. Akagi, H 2017, 'Multilevel converters: Fundamental circuits and systems', Proceedings of the IEEE, vol. 105, no. 11, pp. 2048-2065.
2. Aware, MV & Mane, JJ 2011, 'Multilevel grid connected inverter performance under different modulation strategies', International Conference & Utility Exhibition on Power and Energy Systems: Issues and Prospects for Asia (ICUE), pp. 1-8.
3. Bidyut, M, Saikat, M & Kartick, CJ 2018, 'Carrier based PWM techniques for multilevel inverters: A comprehensive performance study', Journal of Science Part A: Engineering and Innovation, vol. 5, no. 3, pp. 101-111.
4. Gowrishankar, J & Belwin, EJ 2018, 'Comparison of symmetrical and asymmetrical cascaded H bridge multilevel inverter using pulse width modulation', International Journal of Pure and Applied Mathematics, vol. 118, no. 17, pp. 891-901.
5. Gupta, KK, Ranjan, A, Bhatnagar, P, Sahu, LK & Jain, S 2016, 'Multilevel inverter topologies with reduced device count: a review', IEEE Transactions on Power Electronics, vol. 31, no. 1, pp. 135-151.
6. Hasan, NS, Rosmin, N, Osman, DAA & Musta, H 2017, 'Reviews on multilevel converter and modulation technique', Renewable and Sustainable Energy Reviews, vol. 80, pp. 163-174.
7. Irusapparajan, G, Periyaazhagar, D, Prabaharan, N & Rini, A 2019, 'Experimental verification of trinary DC source cascaded H bridge multilevel inverter using unipolar pulse width modulation', Automatika, vol. 60, no. 1, pp. 19-27.
8. Hasan, NS, Rosmin, N, Osman, DAA & Musta, H 2017, 'Reviews on multilevel converter and modulation technique', Renewable and Sustainable Energy Reviews, vol. 80, pp. 163-174.
9. Irusapparajan, G, Periyaazhagar, D, Prabaharan, N & Rini, A 2019, 'Experimental verification of trinary DC source cascaded H bridge multilevel inverter using unipolar pulse width modulation', Automatika, vol. 60, no. 1, pp. 19-27.
10. Ye, M, Chen, L, Kang, L, Li, S, Zhang, J & Wu, H 2019, 'Hybrid multi carrier PWM technique based on carrier reconstruction for cascaded H bridge inverter', IEEE Access, vol. 7, pp. 53152-53162.