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DESIGN OF LOW POWER VEDIC MULTIPLIER USING MGDI TECHNIQUE

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Abstract-Multiplication plays a vital role in the arithmetic operations. In the applications like Signal Processing the multiplication plays a major role in fast Fourier transform and convolutions etc. In this paper we designed the low power and Vedic Multiplier based on Urdhva Tiryakbhyam sutra. The Ripple Carry Adder (RCA) is used to design a Vedic Multiplier. In order to reduce the power consumption Modified Gate Diffusion Input (MGDI) technique is used. The architecture will be designed by using micro wind 2.6 software.

Keywords: RCA, MGDI technique, Vedic Multiplier

I.INTRODUCTION

In VLSI design, a multiplier refers to a digital circuit component used to perform multiplication operation. Multipliers are essential building blocks in digital signal processing, arithmetic operations, and various other computational tasks within integrated circuits. They can be implemented using different architectures such as array multipliers, Wallace trees, Booth multipliers, Vedic multipliers and others, each with its own trade-offs in terms of speed, area, and power consumption. There are a number of options available in choosing the basic circuit approach and topology for implementing various logic and arithmetic functions.

A Vedic multiplier is a type of digital multiplier inspired by ancient Indian mathematical techniques described in Vedic literature it is based on algorithms that exploit patterns symmetries in multiplication, aiming of efficiency and simplicity in electronic circuitry. Vedic multiplier deals with a total of 16 sutras or algorithms for predominantly logical operations. One of the most well-known sutras used in Vedic multiplication is the "Urdhva Tiryakbhyam" sutra.

II.EXISTING METHOD

A Vedic multiplier is a type of multiplier inspired by ancient Indian Vedic mathematics techniques. The existing method involves the design of Vedic multiplier using GDI technique. The results shows that the design of Vedic multiplier consumes more power. The multiplier uses Urdhva Tiryakbhyam sutra. The operation will be done in vertical and cross wise manner. The 2 X 2 Vedic multiplier is multiplied in three steps.

Step 1: The first LSB of the two binary numbers to be multiplied vertically and these numbers are too added with the previous carry, in this case the previous carry is zero. In the output bits the LSB bit will be taken as a result and the remaining bits are forwarded to the next step [6].

Step 2: In this step the two binary bits can be multiplied cross wise and the produced results will be added to the previously generated carry and again, in the output bits the LSB bit will be taken as the result and the remaining bits are forwarded to the next step[6].

Step 3: In this step the MSB bits to be multiplied vertically and the result of this is added to the previously generated carry and the output is taken as the result [6].

III.PROPOSED METHOD

A 4x4 Vedic Multiplier is a type of digital multiplier that is based on the Vedic mathematics system, which is a set of ancient Indian mathematical techniques that are used to solve complex mathematical problems. The Vedic Multiplier uses the Urdhva Tiryakbhyam sutra, which is a multiplication algorithm that is derived from the Vedic mathematical system. The Urdhva Tiryakbhyam sutra is a versatile algorithm that is used to perform multiplication of any two numbers. The algorithm uses a multiplicand and a multiplier, and the multiplication is performed by creating partial products, which are then added to produce the final result. Here, MGDI technique is used to design the 4*4 Vedic multiplier.

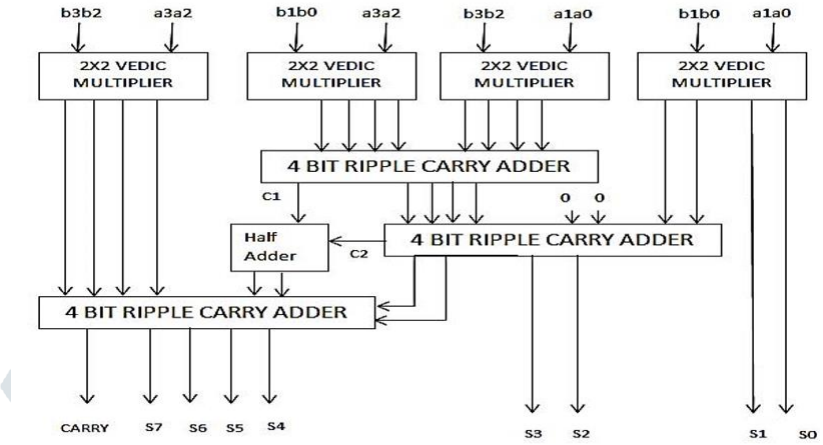

Fig1: Block diagram of 4*4 Vedic Multiplier

IV.RESULTS AND ANALYSIS

The below figure shows the implemented designs of full adder and 4*4 Vedic multiplier using GDI and MGDI technique.

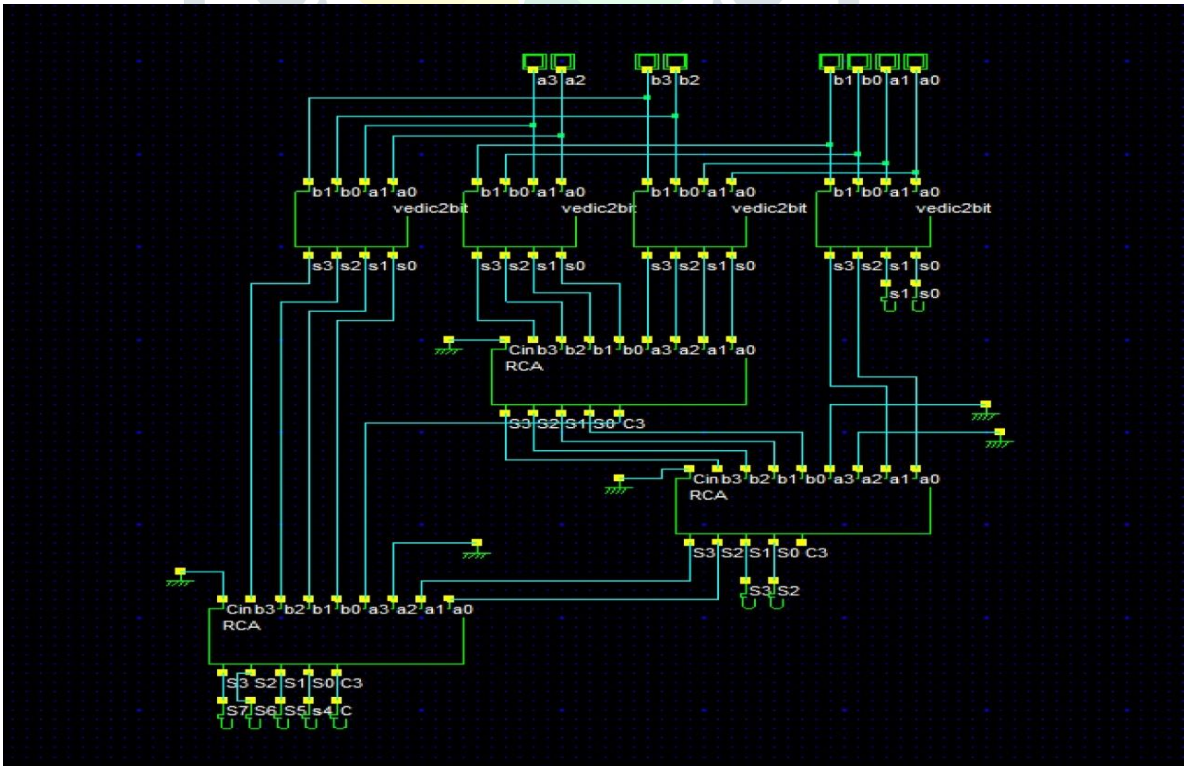

Fig2: 4*4 Vedic multiplier using GDI technique

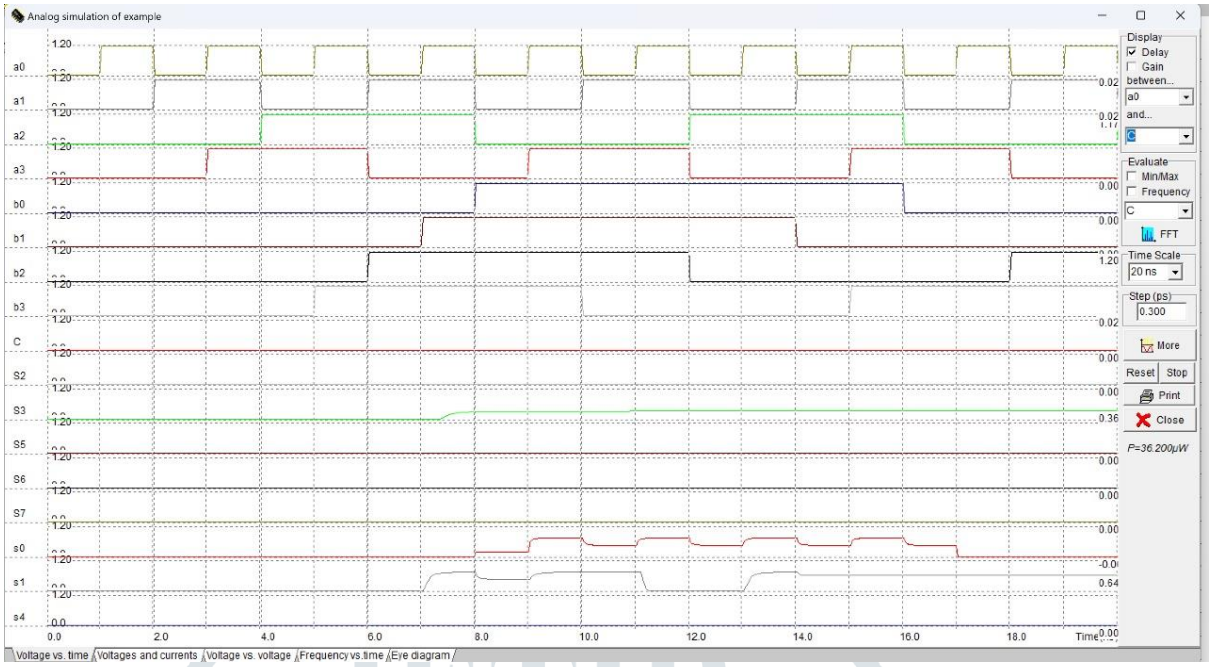

Fig3: GDI technique 4*4 Vedic multiplier waveform

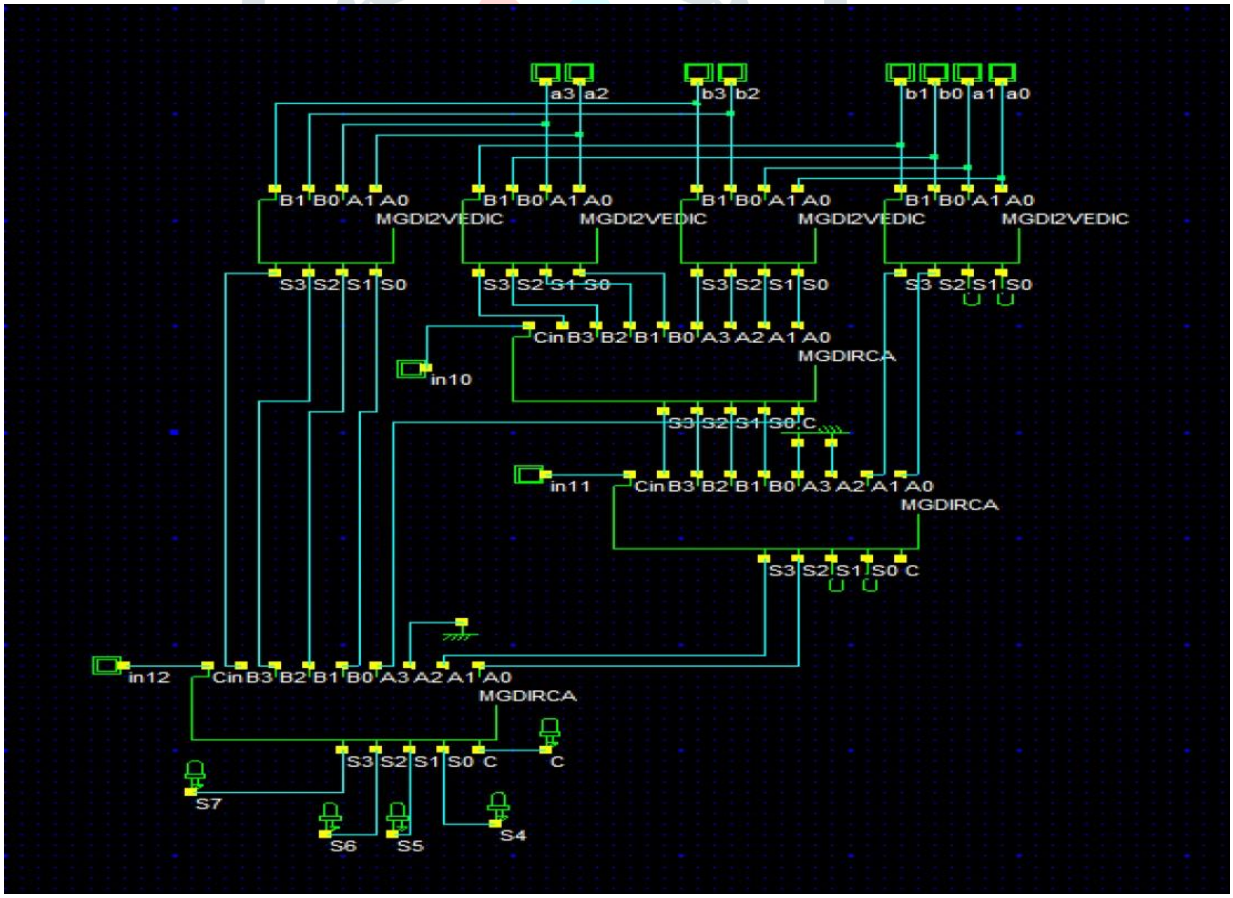

Fig4: 4*4 Vedic multiplier using MGDI technique

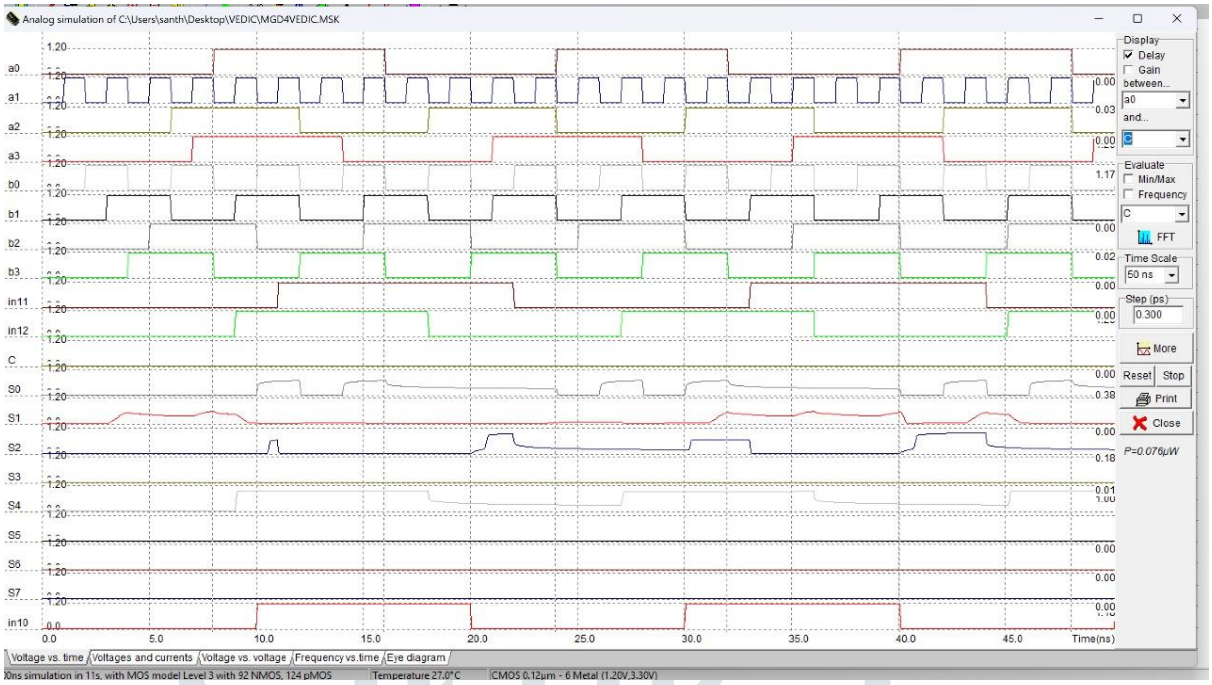

Fig5: waveform for 4*4 Vedic multiplier using MGDI technique

Table1: Comparison of power consumption by 4*4 Vedic multiplier using different logics

Logic Name	4*4 Vedic multiplier
GDI Technique	36.200µW
MGDI Technique	0.076µW

V.CONCLUSION

The project demonstrates that selection of appropriate logic is necessary to reduce the power consumption. The MGDI technique reduces the power consumption compared to GDI technique. Hence the simulation results shows that the MGDI technique reduces the power consumption.

VI.FUTURE SCOPE

Future research might examine other designing methods for designing Vedic multiplier. The effort can lead to low power Vedic multiplier design in future.

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