A Quadratic Boost Two-Stage Transformerless Inverter for Single Phase Photovoltaic Applications

Ch Sabitha
Assistant Professor
Department of Electrical
And Electronics Engineering,
Ramachandra College of
Engineering, India

J Suresh
Assistant Professor
Department of Electrical
And Electronics Engineering,
Ramachandra College of
Engineering, India

D Sai Prasanthi
Assistant Professor
Department of Electrical
And Electronics Engineering,
Ramachandra College of
Engineering, India

P Phani
Assistant Professor
Department of Electrical
And Electronics Engineering,
Ramachandra College of
Engineering, India

Abstract: The transformer-less inverter (TLI) is becoming more popular for use in photovoltaic (PV) systems due to its small size and excellent efficiency. The traditional PV inverter system's cumbersome and heavy transformer may be eliminated, allowing for a smaller TLI. The loss of isolation is the end consequence, as inverters link PV directly to the grid. Leakage current is caused by the direct connection, which causes the common mode voltage (CMV) to vary while the inverter is operating. In order to achieve a five-level output voltage, this article details a two-stage TLI setup. In order to give an inverter quadratic boost output for multilayer output voltage, the front end employs two inductors & two capacitors. Leakage current can be reduced with the use of a common ground configuration (CGC). To regulate the inverter, one uses level-shifted pulse width modulation, or LS-PWM. In addition, before choosing the power components, we examine the inverter's current and voltage stress for each switch. Both the MATLAB/Simulink environment and laboratory experiments are used to verify the TLI.

Keywords - Transformerless Inverter, Photovoltaic, Common Mode voltage, Leakage current, Common ground configuration, LS-PWM

I. INTRODUCTION

Currently, transformer-less inverters are becoming increasingly popular all over the world. Photovoltaic or solar energy is one of the greatest alternatives to traditional energy sources, and it is also readily available practically everywhere on Earth. It generates electricity with little to no noise, no moving components, and requires little to no fuel or maintenance. A transformer-less inverter is a necessary component for harnessing this renewable PV energy that is now accessible at no cost. Compared to the traditional PV inverter system, it offers a number of benefits, including a smaller footprint, less expensive, and more efficient operation. A transformer makes up the bulk of a typical PV inverter system, accounting for around 60% of its overall size and weight. It separates the PV cells from the electrical grid galvanically as well. A transformer-less inverter, on the other hand, bypasses the need for galvanic separation and establishes a direct connection between the PV and the grid. Leakage current is more likely to occur in a direct connection [10]. The common ground configuration (CGC) allows for the removal of leakage current [2], [4]. There is a plethora of material on TLI with CGC [6]-[8]. Additionally, [11]-[14] make advantage of AC and DC decoupling. In order to separate the PV side from the grid side during freewheeling time or zero level of operation, TLI arrangements can be used. operating the inverter system in such a way as to reduce the common mode voltage oscillation, a leading source of leakage current. Nonetheless, an additional power switch to the inverter is incorporated into both AC/DC decoupling systems in order to decrease the leakage current. Popular AC decoupling systems include PN-NPC, HRE, HBZVR D, and HERIC, which separate the PV from the grid by placing a bidirectional switch on the AC side between the power grid and inverter [13], [14]. In order to isolate the PV from the grid side of the inverter system, an additional active power switch is inserted in the PV and inverter front-end in a DC decoupling-based arrangement H10, H9, H6, and H5, as stated in [11], [12]. Existing inverters are made larger, lose more power, and cost more money when more switches are inserted into them. Additionally, these inverters can only produce a voltage within a narrow range of three levels while running in buck mode. Leakage current was not eliminated by all TLI systems with CGC characteristics [15], [16]. The buck mode of operation is implemented via the SCs-based topology that is covered in [bk1]. There is no change to the output; just the conversion from DC to AC occurs. It is rather easy to get the multilayer output voltage using various sources. Achieving multilayer output from a single source is made easier with the SC. Two times the input voltage is the

output voltage of the PV inverters described in [6]. A switched capacitor, charged in parallel with the DC source and discharged in series with the load and source, allows for these boosts. When each conduction cycle is charged and discharged sufficiently, the voltage in the SC is balanced. To balance the voltage on the capacitors, certain SC-based inverters need extra circuitry [17], [18]. In the design shown in [9], the output level is dependent on the quantity of switched capacitors. The voltage boosting that may be done with SCs is restricted to two or three times more than the input sources. Raising the value of the switched capacitor unit raises the output level. To get a greater output level, you need to use more switched capacitors. The voltage-boosting features' reliance on SCs makes them vulnerable to surges in charging current. Minimizing the charging current can be achieved by inserting a front-end tiny inductor into the conduction channel of the switched capacitor [7], [8]. With the above discussion in mind, a two-stage transformer-less inverter is developed for use in photovoltaic applications. To accomplish quadratic voltage gain, a front-end DC-DC converter is used, and the inverter receives additional input for the development of five-level outputs. By using a common ground, the inverter system's leakage current may be effectively eliminated. What the inverter is good for: Quadratic voltage gain can be achieved with the use of a front-end converter. 2) An output voltage with five levels is produced by the back-end inverter.

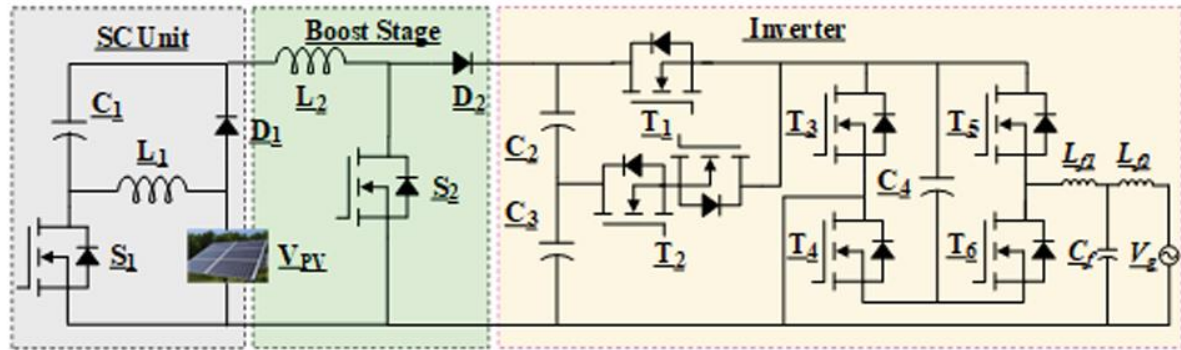2024 Third International Conference on Power, Control and Computing Technologies (ICPC2T)

Fig. 1. Two stage TLI configuration

Thirdly, using self-balanced SCs involves charging and discharging them correctly every cycle. 4) The voltage that blocks the power switches is less than or equal to the output of the front-end converter. 5) A CGC is useful for preventing current leakage.

II. CIRCUIT DESCRIPTION

A novel topology for two-stage transformer-less inverters (TLIs) is covered in this section for the PV application. Figure 1 shows the five-level output of this transformer-less inverter, which is made up of a DC-DC boost converter at the front end and a switched-capacitor multilevel inverter. It generates five different voltage levels using eight power MOSFETs (S_1, S_2, T_1, T_2, T_3, T_4, T_5, T_6), two diodes (D_1, D_2), two inductors (L_1, L_2), switching capacitors (SC) (C_1, C_4), and a DC link capacitor (C_2, C_3). The use of a DC-DC converter at the inverter system's front end allows for four times the boosting capability by providing the inverter with AC output. For the more compact PV source, it is a necessary characteristic. This converter is useful for integrating PV systems with lower output voltages into the grid. The PV source charges dual inductor sets (L_1 and L_2) as well as switching capacitor C_1. While discharging, the DC link capacitors C_2 and C_3 receive four times the voltage ($4V_{pv}$) from the PV source, the charged inductor (SC C_1), and a series connection. In addition, the inverter generates the AC output from the DC link voltage input. When the output voltage is negative, another SC C is discharged via the load; this one is charged to the same amount as the DC link voltage and employed in the inverter component. Switched capacitors can balance themselves, thus there's no need for a complicated circuit to balance the voltage.
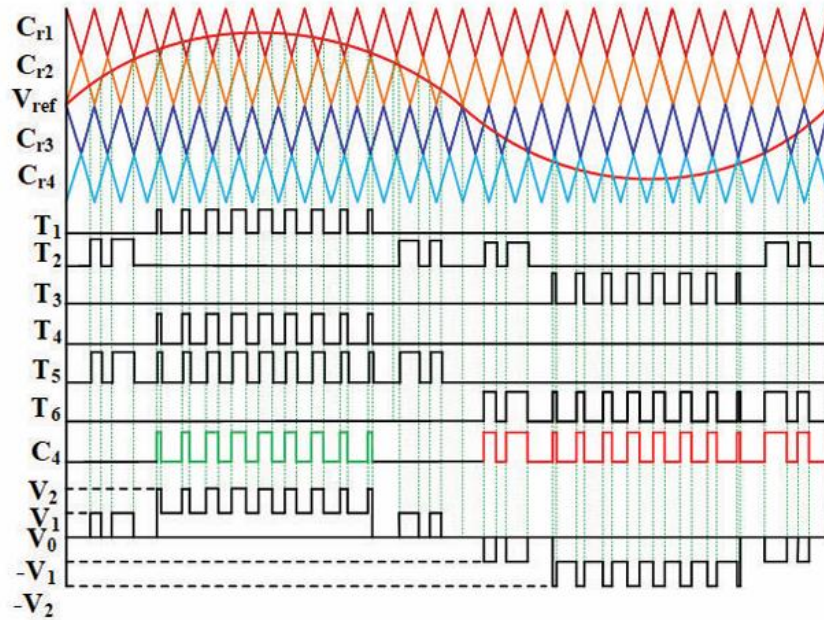
Fig. 2. LS-PWM control scheme

III. MODULATION SCHEME

PWM modulation is utilized to operate the DC-DC converter, and an output voltage of 20 kHz is obtained by switching the frequency.
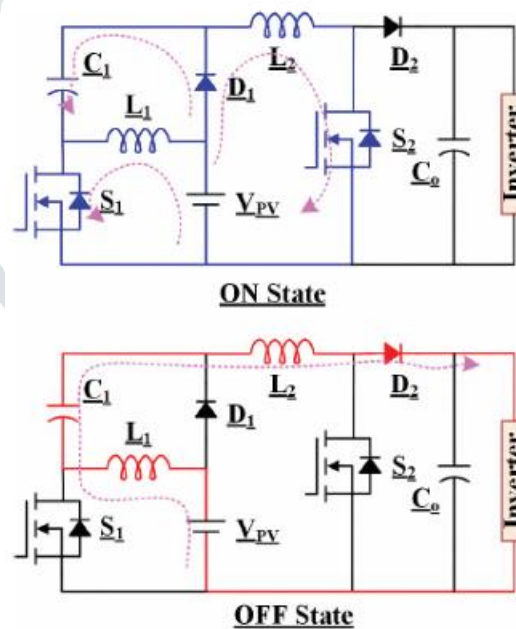

Fig. 3. DC-DC converter operation

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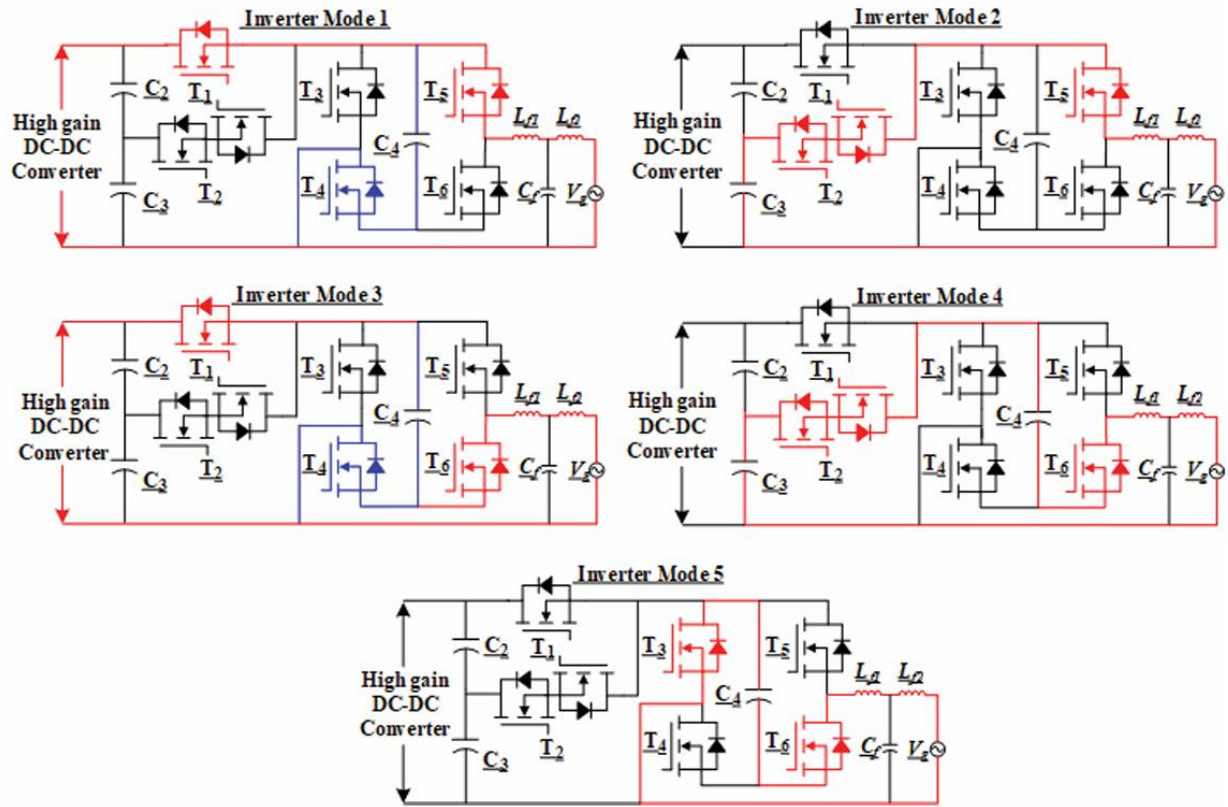
Fig. 4. Inverter working operation

On the other hand, the inverter's functioning is accomplished by supplying the appropriate gate pulse. The necessary gate pulse for inverter functioning is produced by level-shifted pulse width modulation, or LS PWM. To obtain the necessary gate pulse in LS-PWM, four carrier triangle waves with a switching frequency of 10 kHz are compared to a basic sinusoidal wave. Fig. 2 displays a switching pulse for every switch. Fig. 2 depicts the necessary switching pulse for this inverter. The necessary switching sequence must be followed in order for the inverter to function. For the generation of output level, inverter operation adheres to a particular switching sequence.

IV. WORKING OFINVERTER

Two phases are involved in two-stage TLI power transfer. The DC-DC inverter functions for four times gain in the first mode, and this output is used for five levels of output by the second inverter. The DC-DC converter has a high switching frequency and operates in two states. When switches both S1 and S2 are held in the ON position, the capacitor and inductor are charged. The output power for the inverter is then supplied by both the inductor and capacitor discharging. As seen in Fig. 3, both of the switches remain in the off position. The output voltage of the DC-DC converter can be written as

$$V_{output} = 2\frac{V_{PV}}{1-D} \qquad (1)$$

where D stands for duty ratio; this duty ratio is maintained at 50% to obtain $V_{output} = 4V_{PV}$. Five modes of operation can also be used to explain the five-level inverter.

In Mode 1, as illustrated in Fig. 4, $V_o = 4V_{pv}$, the output voltage level is attained by maintaining the ON states of switches T_1 and T_5. By doing this, the inverter output terminal is directly connected to the DC link voltage. That switched capacitor C4 is connected across the voltage of the DC link and charged to the total of the DC link capacitor (C_2 and C_3) at the same time that switch T4 turns ON. The resultant voltage level is attained in Mode 2, $V_o = 2V_{pv}$, by Switches T_2 and T_5 provide the output voltage level in Mode 2, $V_o = 2V_{pv}$. This voltage output level is powered by the DC connection capacitor C_3. By maintaining switches T_4, T_6, in the ON state, zero voltage output level is attained in Mode 3, $V_o = 0$ V. Switches T_4 & T_6 offer a path for the load's current flow in this condition. Concurrently, switch T_1 is activated to link the voltage of the DC link capacitors in parallel to the SC C_4. Mode 4, $V_o = -2V_{pv}$, is the output voltage level that can be reached by maintaining the ON states of switches T_2 and T_6. The output terminal has a 2 V_{pv} output voltage since the DC link's capacitors C_3 & SC C_4 are linked in series having opposite polarity. At this output voltage level, the SC C_4 discharges. By switching on switches T_3 & T_6, the output voltage level in Mode 5, $V_o = -4V_{pv}$, is reached.

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TABLE I
COMPONENTS PARAMETER FOR BOOST MODEOFOPERATION

Components	Parameter
Switch	NTHL020N120SC1
Gate driver	Skyper 32
Controller	TMS320F28379D
Switching frequency	10 kHz
Output power	1kW
Input voltage	100 V
Output voltage	328 V
Output current	6.3 A
SCs	2200Mf
L1, L2	10mH
Filter capacitor	40 Mf
Filter Inductor	0.02 mH

Only SC C_4 keeps the output voltage for the output terminal constant at that voltage level. It is evident from the various modes of operation that just two switches are needed to create output voltage for each conduction level. To charge the SC C_4, one additional switch is required.

V. COMPONENTS SELECTION AND LOSS CALCULATION

Power components are arranged inverters in a certain way, for example, to produce multilayer output voltage. These power components are used to generate the multilayer outputs, therefore choosing the right power components is important to achieving high-quality output voltage. The inverter design can be made more cost-effective by making the right choice.

(1) DC link capacitors, (2) Power switch board, (3) Skyper board (4) TMS320F28379D , (5) 15 Volt Power supply for gate driver, (6) Break out board, (7) Switched capacitor, (8) Resistor, (9) Filter component (L_f, C_f), (10) Current sensor, (11) Oscilloscope
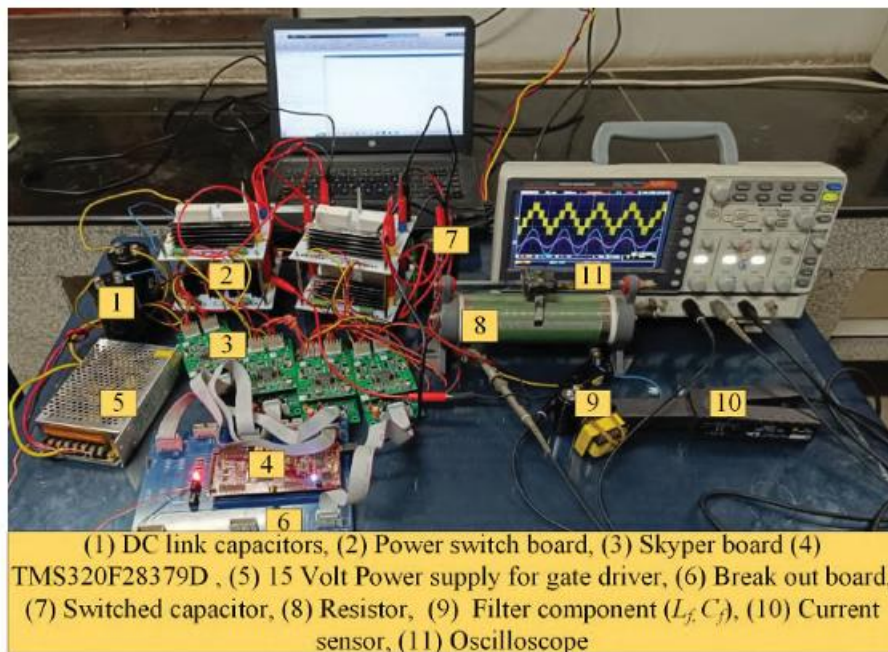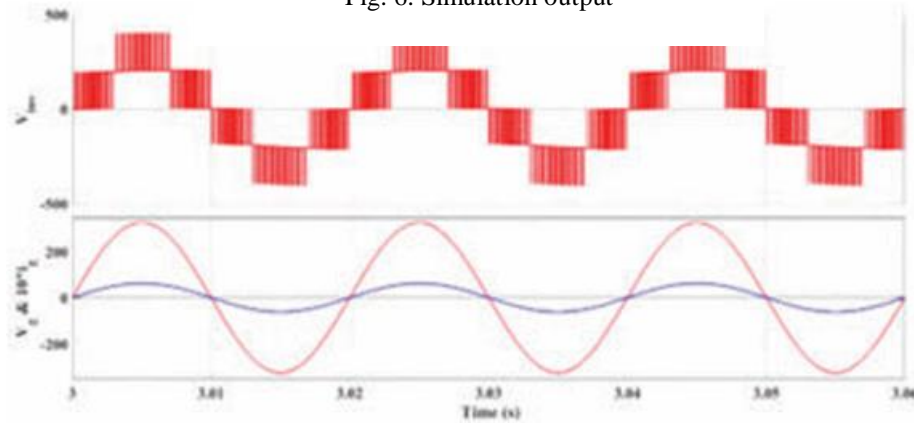
Fig. 5. Experimental Setup

A. Capacitor selection

A switched capacitor in a SC-based TLI maintains the output power. For the output terminal to preserve power quality, a larger capacitance value is advised.The formula is used to determine the value of the capacitor.

$$C_i = \frac{P_o}{2\omega_o V_{PV} \Delta V_{PV}} \qquad (2)$$

where, i =1,2,3,4 ω_o is the angular grid frequency.

Fig. 6. Simulation output

B. Selection of inductor

The inductor value can be found by using the equation

$$L_1 = L_2 = \frac{V_{PV}D}{\Delta i_{PV}f_s} \qquad (3)$$

where, f_s is the switching frequency.

C. Switch loss

The switching losses for power switches are caused by the ON AND OFF state frequency during every operation cycle. Switching losses may be greater at higher frequencies than at lower ones. On the other hand, conduction losses rely on the conducting components' equivalent resistance. Consequently, the whole switch loss can be written as

$$P_{sw} = \frac{f_s}{6} i_{rms} V_{rms}(E_{on} + E_{off}) + i_{o,rms}^2 r_{eq} \qquad (4)$$

VI. RESULTS DISCUSSION

As shown in Fig. 5, an experiment is conducted in the laboratory and MATLAB/Simulink environment to verify the provided two-stage TLI. Tabel I displays the parameters of the parts utilized in the simulation and experiment. As shown in Figs. 6 and 7, the experiment uses 400 DC, which is produced from a high gain DC–DC converter, as input to the inverter system to provide a five-level voltage output of 325 V. The waveforms for grid voltage and current are also shown in this figure.
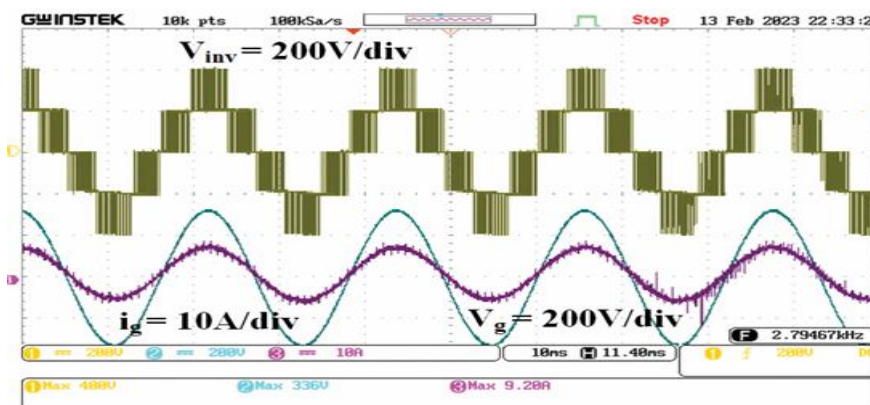

Fig. 7. Output voltage and current of inverter

Because a switched capacitor unit keeps the power output of the inverter constant for the output with a negative voltage level, the experiment is run for a 1 kW load system. After analyzing the voltage of these switched capacitors, it was found that V_{C1}, V_{C2}, and V_{C3} could supply the output voltage at a negative level. The voltage waveforms of the switched capacitor and DC link capacitor are displayed in Fig. 8(a). Higher current spikes across capacitor units are observed in certain switched capacitor-based multilevel inverters. Spikes in high current reduce the SCs unit's life cycle. Similarly, Fig. 8(e)–(f) shows the voltage stress throughout switches.

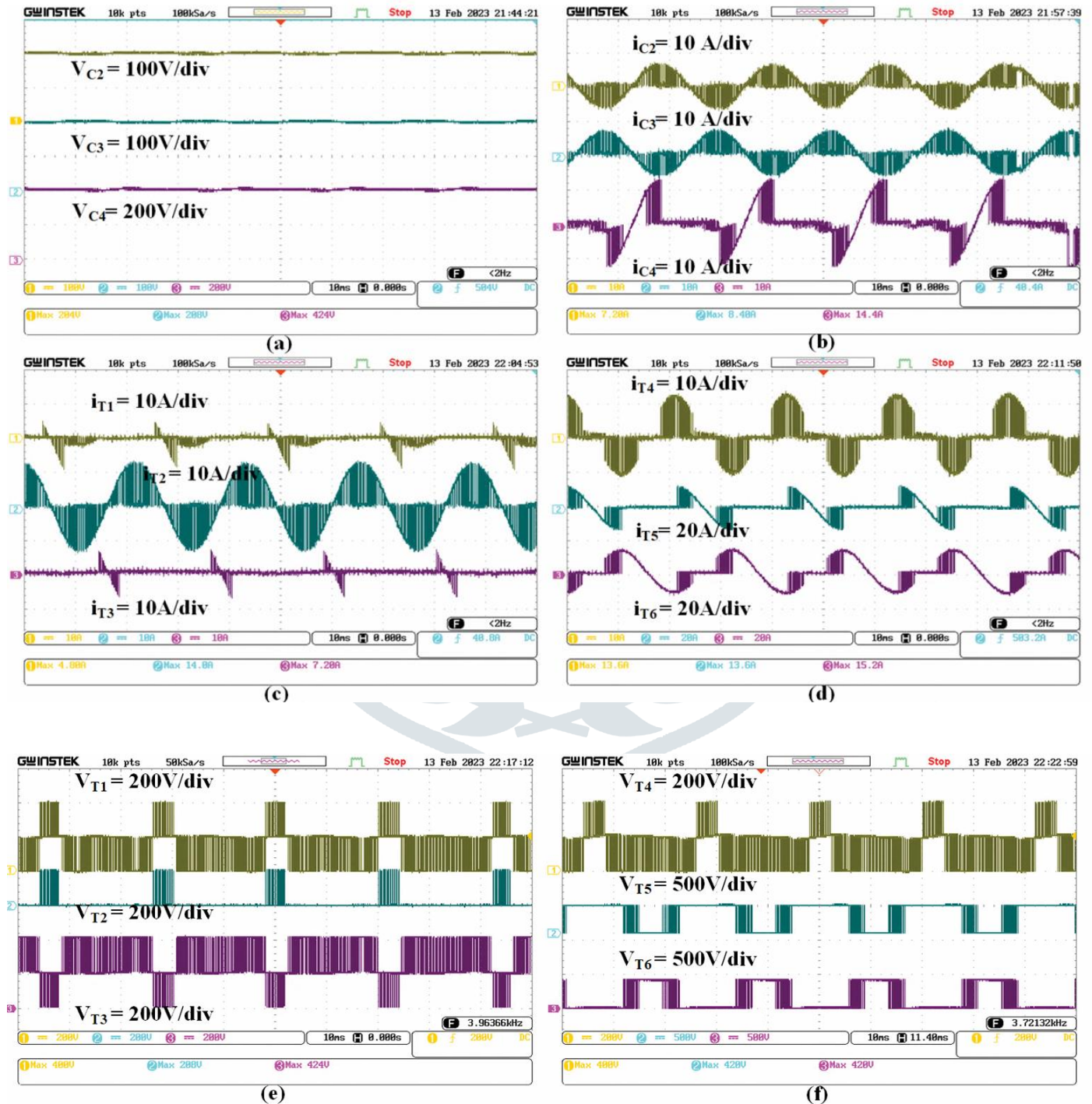**2024 Third International Conference on Power, Control and Computing Technologies (ICPC2T)**

Fig. 8. Stress across the different power components

VII. COMPARASION WITH EXISTING ARE OF LITERATURE

By contrasting this inverter with the current body of literary works, its benefits become apparent. Table II presents the results of a comparison examination between the number of power components & attributes, including TSV, CGC, LC, Gain, power, and efficiency. According to this table, architecture [5] utilizes the fewest devices/power devices to achieve multilayer output voltage, whereas [1] uses the greatest amount of components. In order to generate output levels that are comparable, the suggested topology

and [2] employ the exact same component count. The suggested topology makes use of higher power diodes, switches, and capacitors. It also uses [2], [3] in inverter operation. The suggested topology has a higher TSV in relation to the input voltage source than the topologies [4] and [5], which have TSVs of $6V_{DC}$ and $12V_{DC}$, respectively. The TSV of the inverter system is increased through the quadratic voltage enhancing feature. In terms of output voltage, the TSV drops four times. All but [1] of the inverters that have been discussed have CGC.

TABLE II

COMPRESSION PROPOSED TLI WITH EXITING TWO-STAGE FIVE LEVEL TLI

[Ref]	C_{switch}	C_{diode}	$C_{inductor}$	$C_{capacitor}$	TSV	CGC	LC	Gain	Power η
[3]	7	2	3	4	-	Yes	0	2	3kW @ 98%
[4]	8	4	1	2	6VDC	Yes	17.4mA	2	500W @ 97.24%
[2]	7	5	3	2	-	Yes	LC	1	1.5kW @ 97.36%
[1]	8	4	2	4	-	No	70mA	2	3kW @ 97.4%
[5]	7	3	1	2	12VDC	Yes	-	2	1kW @ 96.8%
[P]	9	2	2	4	16VDC	Yes	0	4	1Kw @ 97.1%

[1] has a 70mA leakage current. There's also a tiny quantity of LC in [4]. TLI's efficiency ranges from 96% to 98%, while the suggested inverter's efficiency is 97.2%.

VIII. CONCLUSION

This research proposes a two-stage TLI that includes a front-end DC-DC converter and SC working together to provide a quadratic boosting feature. The quadratic boost is achieved via the front-end converter's high switching frequency operation. By employing a low inverter section switching frequency, losses from this converter are minimized. LS-PWM generates the correct switching sequence for charging and discharging throughout each operational cycle, enabling SC to have a self-balanced characteristic. By contrasting the inverter with the body of current literary art, its benefits can be discovered. A common ground arrangement is provided in order to eliminate leakage currents. When designing an inverter, a thorough analysis of the stress caused by voltage and current is done. Among the benefits of the inverter which make it a strong contender for a photovoltaic PV application are its quadratic boost, straightforward inverter control system, minimal leakage current, and reduced stress across the power components.

REFERENCES

[1] J.-S. Kim, J.-M. Kwon and B.-H. Kwon, "High-Efficiency Two-Stage Three-Level Grid-Connected Photovoltaic Inverter," in IEEE Transac tions on Industrial Electronics, vol. 65, no. 3, pp. 2368-2377, March 2018, doi: 10.1109/TIE.2017.2740835.
[2] L. Zhang, F. Jiang, D. Xu, K. Sun, Y. Hao and T. Zhang, "Two stage transformerless dual-buck PV grid-connected inverters with high efficiency," in Chinese Journal of Electrical Engineering, vol. 4, no. 2, pp. 36-42, June 2018, doi: 10.23919/CJEE.2018.8409348.
[3] Y. Chen, M. Chen and D. Xu, "A 3-kW Two-Stage Transformerless PV Inverter With Resonant DC Link and ZVS-PWM Operation," in IEEE Transactions on Industry Applications, vol. 57, no. 2, pp. 1495-1506, March-April 2021, doi: 10.1109/TIA.2020.3043218.
[4] S. K. Kuncham, K. Annamalai and N. Subrahmanyam, "A Two-Stage T Type Hybrid Five-Level Transformerless Inverter for PV Applications," in IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 9510 9521, Sept. 2020, doi: 10.1109/TPEL.2020.2973340.
[5] N. V. Kurdkandi, M. Ghavipanjeh Marangalu, T. Hemmati, S. H. Hosseini, O. Husev and A. Khsokhbar-sadigh, "Single-Phase Two Stage Transformerless Grid-Connected Inverter For Photovoltaic Appli cations," 2021 12th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), Tabriz, Iran, 2021, pp. 1-5, doi: 10.1109/PED STC52094.2021.9405959.
[6] S. S. Neti, V. Singh, S. Pattnaik and V. Anand, "Common-Ground Single-Stage Transformerless Inverter using Switched-Capacitor for Sin gle Phase PV Application," 2023 IEEE IAS Global Conference on Re newable Energy and Hydrogen Technologies (GlobConHT), Male, Mal dives, 2023, pp. 1-7, doi: 10.1109/GlobConHT56829.2023.10087729.
[7] Singh Neti, S, Singh, V, Pattnaik, S, Anand, V. Single-phase five-level common-ground transformerless inverter using switched capacitors for photovoltaic application. Int J Circ Theor Appl. 2023; 51(10): 4626 4645. doi:10.1002/cta.3671.
[8] Singh Neti, S, Singh, V. A common ground switched capacitor based single-phase five-level transformerless inverter for photo voltaic application. Int J Circ Theor Appl. 2023; 51(6): 2854-2874. doi:10.1002/cta.3552.
[9] Neti, S.S., Anand, V. Singh, V. Single-Phase Generalized Switched Capacitor Multilevel Inverter Using Reduced Number of Power Semi conductor Components with Voltage Boosting Ability. Arab J Sci Eng 47, 2613–2627 (2022). https://doi.org/10.1007/s13369-021-05701-9

[10] H. Patel and V. Agarwal, "A Single-Stage Single-Phase Transformer Less Doubly Grounded Grid-Connected PV Interface," in IEEE Trans actions on Energy Conversion, vol. 24, no. 1, pp. 93-101, March 2009, doi: 10.1109/TEC.2008.2006551.

[11] Y. Y. Syasegov et al., "HERIC-Clamped and PN-NPC Inverters With Five-Level Output Voltage and Reduced Grid-Interfaced Filter Size," IEEE Open J. Power Electron., vol. 4, pp. 306–318, 2023.

[12] S. Jain and V. Sonti, "A Highly Efficient and Reliable Inverter Con f iguration Based Cascaded Multilevel Inverter for PV Systems," IEEE Trans. Ind. Electron., vol. 64, no. 4, pp. 2865–2875, 2017.

[13] M. F. Kibria, A. Elsanabary, K. S. Tey, M. Mubin, and S. Mekhilef, "A Comparative Review on Single Phase Transformerless Inverter Topolo gies for Grid-Connected Photovoltaic Systems," Energies, vol. 16, no. 3, 2023.

[14] P. S. Gotekar, S. P. Muley, D. P. Kothari, and B. S. Umre, "Comparison of full bridge bipolar, H5, H6 and HERIC inverter for single phase photovoltaic systems- a review," in 2015 Annual IEEE India Conference (INDICON), 2015, pp. 1–6.

[15] Y. P. Siwakoti, T. Long, R. Barzegarkhoo and F. Blaabjerg, "A Dual Mode 5-Level Inverter with Wide Input Voltage Range," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 3609-3615, doi: 10.1109/ECCE.2019.8912556.

[16] Valderrama GE, Guzman GV, Pool-Maz´un EI, Martinez-Rodriguez PR, Lopez-Sanchez MJ, Zu˜niga JMS. A Single-Phase Asymmetrical T-Type Five-Level Transformerless PV Inverter. IEEE Journal of Emerging and Selected Topics in Power Electronics 2018; 6(1): 140-150.

[17] Dhara S, Hota A, Jain S, Agarwal V. A transformerless 1-phase, 5 level half-bridge PV inverter configuration based on switched- capacitor technique. IEEE Transactions on Industry Applications 2021; 57(2): 1619–1628.

[18] Xu S, Zhang J, Hu X, Jiang Y. A novel hybrid five-level voltage-source converter based on T-type topology for high-efficiency applications. IEEE Transactions on Industry Applications 2017; 53(5): 4730–4743.

[19] Grigoletto FB. Five-Level Transformerless Inverter for Single-Phase Solar Photovoltaic Applications. IEEE Journal of Emerging and Selected Topics in Power Electronics 2020; 8(4): 3411-3422.