

Analysis of Failure Encountered by IC Substrate and Plastic Package

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Abstract—This paper presents the review on the work done on failure analysis mainly with respect to temperature and humidity. The pressure failure mode include package delamination ,solder abnormality and moisture ingress. After studying their impact,source prevented measures and improvements suggested have been studied.

Keywords—, *plastic packaging, delamination, solder abnormality' moisture ingress, failure analysis technology, IC substrate*

I. Introduction

The semiconductor engineering process is poised by different separate companies. Generally, these companies are special concentrating on one fact of fabrication: assemble, test, PCBA and etc. Therefore it takes up even long time in transfer and storage steps. For instant, a building block from company A would have been stored for more than one year before soldering on board at company B. During this period, the most sensitive issue encountered in practice is environment (temperature, humidity) which could be replicated by “Moisture Sensitivity Level” test. Most of the time, this problem will occur in the real-world application at customer site [1]. The failure linked to MSL appears to overtake the ratio of ESD failure, and these two kinds have occupied the failed modes of whole cycle of device's life. This paper is to clarify some mainly achievement of FA by crisp two year's FA data and reports in their lab. The hitches are all accomplished and verified through modern FA

technologies. X-ray ,scanning acoustic microscope (SAM), final test (FT) equipment are classified to non-destructive tools when cross section/polish destructs the

samples to suspected area. Then, Optical Microscope (OM) and Scanning Electron Microscope (SEM) with Energy Dispersive Spectroscopy (EDS) are taken privileged at final check. All the irregular parts are selected as plastic encapsulation and substrate or lead-frame which are more typical and popular packages and structures. The failure images of delamination, solder abnormality (joint melt, bridge, SMD short/open) are demonstrated .But still it just shoot a glance of failure appearance and provides a introductory study of root cause . Hope for those who do not have enough attention to these problems, remind and formed would promote their quality and cheapness[2].

II. Failure mode

A. Type one : Delamination

As a chief fact in the arena, delamination is considered the most common and sensitive problem for affecting the activation energy of the different materials. And this could be tempted by variable temperatures(thermal cycling or thermal shock), extreme high temperature storage (for electronics products:150℃) which could damage the structure of package , for the purpose that each material has its own coefficient of expansion when temperature change ,the interface flanked by the different two materials is at a dis-match status , and the two materials separated and then a new gap at this interface produced ,always “open signal” could be detected using a parameter tester.

B. Type two: Solder Abnormality

When the solder materials meet a high temperature above 235°C (for Pb free) the solder would melt, restructure and flow around along with the gaps. Finally, the links in package are “short” or “open”.

C. Type three: Temperature, Humidity and bias failure

Suppose the model is in an atmosphere of suitable temperature and humidity, the moisture have entered into the interlayer or materials in package. When this example under bias, which means some of the PADS on die own a potential voltage to other circuits, the moisture would expand along the potential path and cause electric problems.

III. Case study

All discontent samples were established by a common failure analysis flow, still denoting to former practices, specific process were taken and proved to be helpful. For the cases in this paper, firstly, FT is pragmatic to define which parameter was abnormal, such as open/short signal, a high/low leakage, and this could be shortened by IV tracer even multi-meter sometimes; X-ray was used to check if there was solder abnormality or crack in the package; SAM was performed to find the location of potential delamination.

After the suspected area was located, the destructive ways which determine cross-section and polishing (physical FA process) came to expose the bomb spots. These fail spots were taken pictures by using OM and SEM.

A. Case one : Delamination

When the miscarried samples was proved to exist delamination that damage the parameters, they usually displays:

- molding compound and lead-frame separated

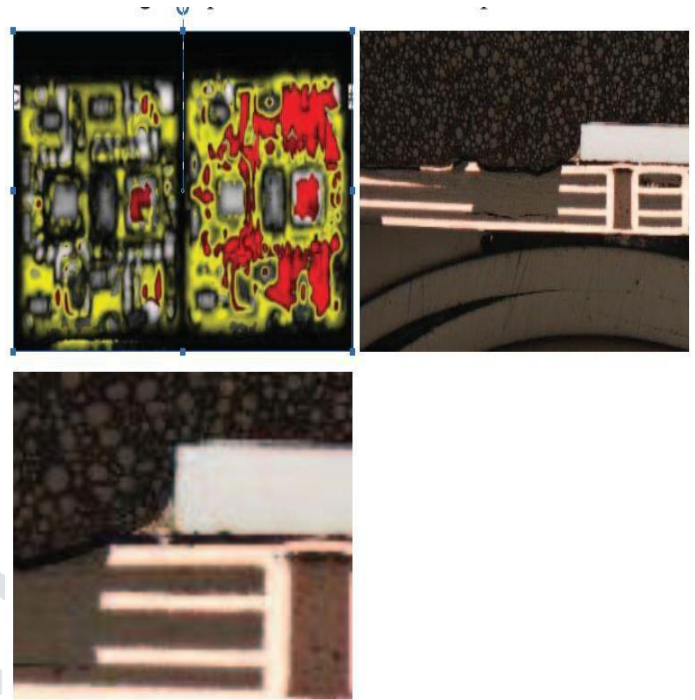


Fig.1. Displaying SAM found delamination and side cross-section confirmed molding compound and lead-frame separated, unstable curve during IV test[3].

- Bonding stitch broken

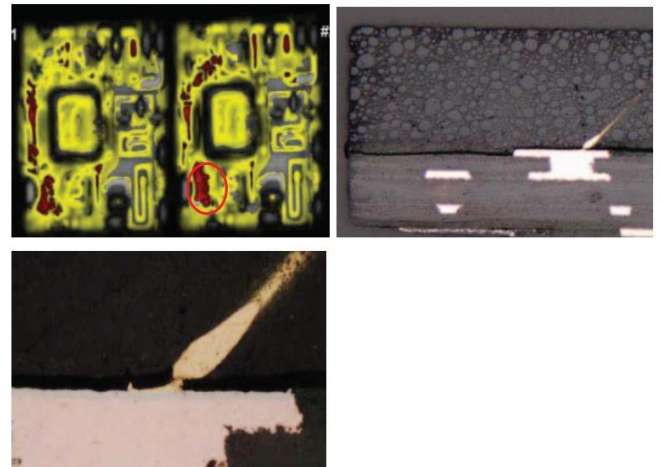


Fig.2. SAM found delamination and side cross-section set bonding stitch broken, open signal probing for this connection[4].

B. Case two : Solder Abnormality

When the miscarried samples was proved to have solder abnormality that damage the parameters, they usually displays:

- solder reflow cause “SMD open/short”

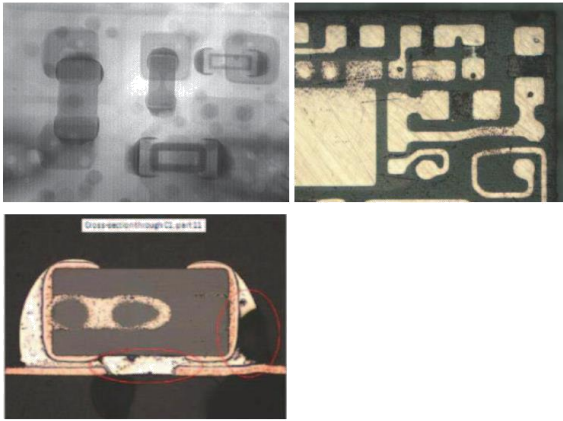


Fig.3. Displaying X-ray found solder deviation on one SMD and behind polish and side cross section set SMD two terminal “solder short”, very high current to GND for FT result

- solder reflow cause “lead short”

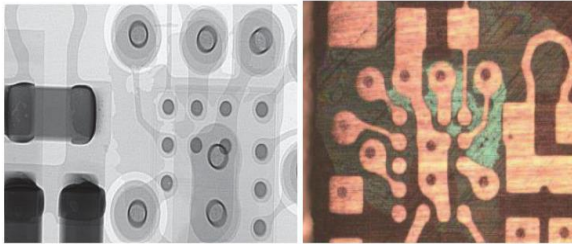


Fig.4. Showing X-ray found solder abnormality on one SMD [5].

- solder reflow cause “solder ball melt and short”

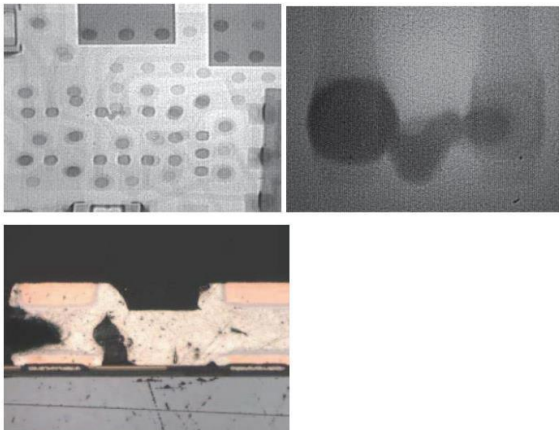


Fig.5. Displaying x-ray found solder ball melt and lateral cross section confirmed two balls “solder short”, short curve during IV curve[8].

C. Case three :temperature ,humidity and bias fail

When the failed samples were proved to have this failure, they usually shows:

- die surface moisture ingress

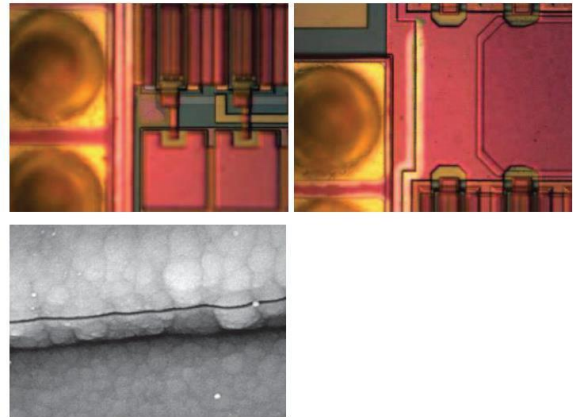


Fig.6. Displaying OM found ingress moisture on edge of die surface and SEM found passivation crack proof, a marginal leakage on this pad during FT[7].

- die surface passivation crack

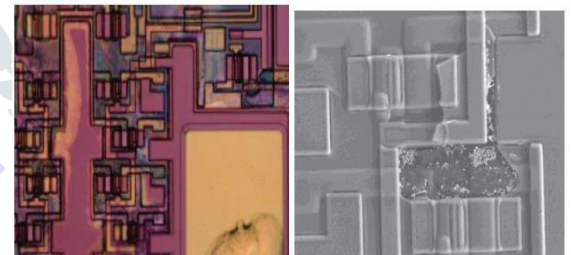


Fig.7. Displaying OM found moisture ingress on edge of die and SEM bring into being passivation crack evidence, various parameters fail during FT[6].

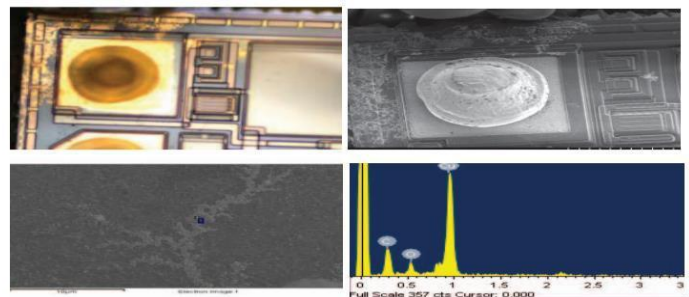


Fig.8. Displaying OM found discolor and relocation on edge of die surface and SEM(EDX) set Cu migration on surface , high leakage on this PAD during FT[1].

IV. Conclusion

Summarizing these cases and some corresponding conclusions were made on these three evidences:

- Ratio of temperature ,humidity failure
- FA technology application
- case analysis and initial root cause

A. Ratio of temperature ,humidity failure

Two years' cases of their lab are brief from the stage of process monitor ,reliability test and customer return, the ratio of temperature and humidity bomb is shown below

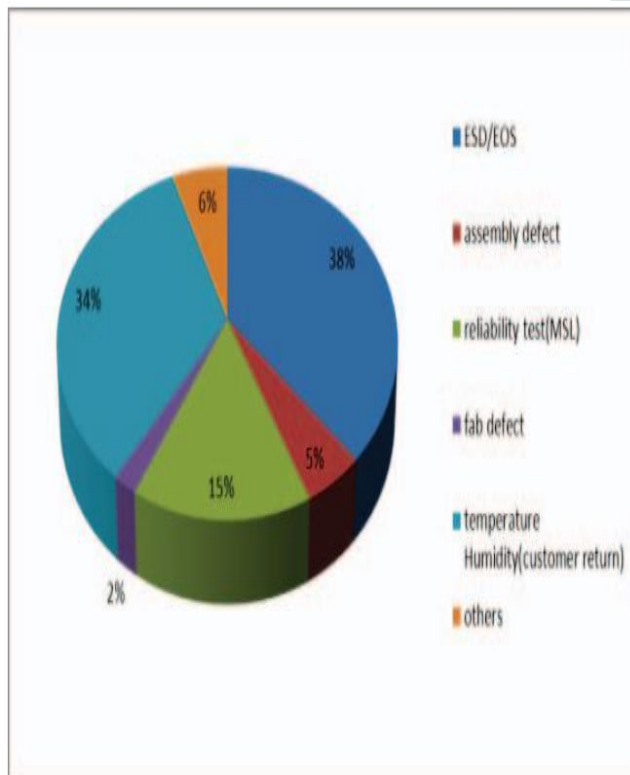


Fig.9. Displaying each failure mode ratio in our company [1].

The temperature and humidity related issues are still our top test

B. FA technology application

TABLE I

Fail mode	Non destructive			Destructive	
	FT	X-ray	SAT	Cross section	De-capsulation
Delam	Ohmic or IV curve	X	Color map	Side Polisher	X
Solder abnormal	Ohmic or IV curve	Gray value map	Color map	Side, top,back polisher	X
Moisture ingress	Ohmic or IV curve	X	Color map	X	Exposing die surface

Fail mode	Inspection	
	OM	SEM
delamination	Black gap, crack at interface	X
Solder abnormal	Solder melt/flow/bridge	X
Moisture ingress	Discolor on die	Crack in /on the die

C. Case analysis and initial root cause

Functional test against temperature ,humidity :The products with substrate and SMD package possesses the solder material , and more sensitivity on temperature ,humidity. When open/short signal was spotted under FT, firstly these issues should be revealed.

Delamination and open bonding :always when along the delamination border(Fig.1&Fig.2), there should be affection end(whatever ball or stitch),the separated layers must have effect the connection between closeness and its leads(frame or pad),so this connection could be broken by the section.

The relative of delamination and solder reflow: for the substrate/SMD samples with solder on(Fig.3~5) ,after delamination happened , there came a sudden high temperature(like solder on board process:235℃ for Pb free)

the solder material melt down and re-soldered shape beside the delamination gap, so the lands of substrate would be solder –

linked which could even induce a heavy short, and lack of solder would break the original connection which make the circuit

vulnerable. Always one fail mode was not only occur on one failed sample, they combine and happen subsequently, one failure may occur next another[1].

The relative of Moisture and electric damage :for electric damage samples after exposing to environment ,moisture maybe one of the root causes(Fig.6~8) .Humidity have invaded into at the package/die, when the bias applied, this potential voltage would accelerate this ingress. Sooner ,the relative circus was leak aged, with time goes ,this marvels would become serious and activates ESD/EOS damage which could cover the true cause. Moisture induced failure that is additional observed by using a thermal discharging equipment to match the result.

Advices: facing to these circumstances, a proper time of sweltering would be a better solution to drive out the potential moisture whenever the resulting cases exist: a long period storage, the transfer from each process or company, de-solder or re-solder from PCB, return from customer, and etc. Or pay more attention to the loading environment at each process.

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