

Θ_i -SELECTION MODULE IMPLEMENTATION USING ADAPTIVE CORDIC FOR FFT ARCHITECTURES

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Abstract—This electronic document is a “live” template and already defines The overview of this paper is to design a micro rotation selection block for TW based FFT. This design is mainly based on Adaptive CORDIC algorithm. CORDIC stands for COordinate Rotation Digital Computer. Two ways to implement the CORDIC algorithm are 1. Vector mode and 2. Rotation mode. The main difference between Vector and rotation are, vector mode is used to compute an angles at given point where as Rotation mode is used to compute the sine and cosine terms at given point. This paper mainly deals with vector method by using micro rotation for complex multiplications in FFT architectures. Θ_i -selection (Θ_i -sel) block for CORDIC based Twiddle Factor (TW) architecture is a computation approach which does an angle selection. CORDIC algorithm is easy to implement trigonometric, hyperbolic and exponential functions based on micro rotation for VLSI Signal processing. The simulation results are examined using Xilinx ISE 14.5 Tool.

Keywords—Fast Fourier Transform (FFT), Adaptive CORDIC Algorithm, Θ_i -selection (Θ_i -sel).

I. INTRODUCTION

In digital signal processing the Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) are playing an important role. The fast computation method of Discrete Fourier Transform (DFT) algorithm is Fast Fourier Transform (FFT).

In 1965 [1], Cooley and Tukey was first introduced the FFT signal flow graph. So that, FFT became most utilized circuits in many of signal processing and communication applications such as CDMA [5], OFDM [6], WiMAX [2], MIMO [4], WLAN [7], and 3GPP-LTE [3]. In addition to this FFT requires a computational technique in other applications like the image processing application of Fourier-Domain Optical Coherence Tomography (FD-OCT) [9], Synthetic Aperture Radar (SAR) [10], and the multimedia application of Digital Video Broadcasting-Terrestrial or Digital Video Broadcasting-Handheld (DVB-T/DVB-H) [8].

FFT architectures are of two types. They are Fixed-point and Floating-point architecture. The problem with fixed point architecture is Fixed-point Arithmetic Error (FAE) [11]. In systems fixed point or floating point FFT implementations are used for high speed with low resource cost or High Precision with wide data range.

In Twiddle Factor (TF) implementation, there are two categories. Namely, Look-Up Table (LUT) [14]-[17] and Direct computation based on COordinate Rotation Digital Computer (CORDIC) algorithm [12],[13],[18]. Where the LUT 's uses a floating point multiplication and it stores the trigonometric constants where as the CORDIC is used to make a direct computation.

The advantages of LUT based design is high precision, low latency, and reasonable cost. But the problem with LUT based technique suites for only a limited number of FFT- point than a large number of FFT-points. Here by increasing the number of FFT-points the number of stored elements in LUT also increases. Therefore, there is a memory requirement problem. This problem can be overcome by many other techniques such as binary tree decomposition algorithm [21], memory access optimization [22], memory minimization method [19], and Read-After-Write latency optimization [20]. In these techniques also there is a trade-off between memory reduction, performance of accuracy, and the throughput rate.

For large-point FFT systems and Application Specific Integrated Chip (ASIC) implementation, a direct computation method is selected i.e., CORDIC. CORDIC algorithm provides a memory free solution for Twiddle Factor (TF). But the main disadvantage of CORDIC algorithm is high latency because of more number of iterations. To overcome this disadvantage we can move on with Adaptive CORDIC (ACor) method and it was introduced by Y. H. Hu et al. in 1993 [23]. The improvements in the method was introduced by Hong Thu Nguyen et al. in 2015 [24]. The main idea of the ACor method is to reduce the number of iterations and giving the equivalent or better accuracy performance. By reducing the number of iterations, the ACor method gives a low-resources, low-latency, and high-precision.

II. BASIC CORDIC TECHNIQUES

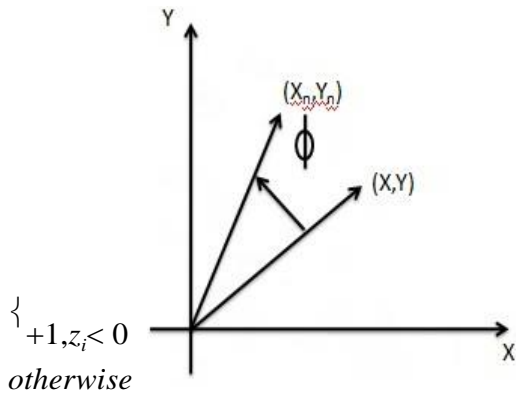
Lets us consider, the two vectors $[X, Y]$ of the same magnitude. And the second vector is obtained by rotating the first vector with an angle of (θ) .

Now we can calculate $V_n = [X_n, Y_n]$ based on the input vector and the rotational angle (θ) . The required equations are given below:

$$X_n = X_0 \cos(\theta) - Y_0 \sin(\theta)$$

$$Y_n = Y_0 \cos(\theta) + X_0 \sin(\theta)$$

(1) Where θ is a rotation angle.



which indicates the direction of next rotation is used to reduce the angular error. The difference equation is based on logic as

$$Z_{i+1} = Z_i - d_i \cdot \tan(\phi_i) \tag{6}$$

Where Z_i ($i = 0, 1, \dots, N-1$). Z_i indicates the remaining rotation before performing the rotation by ϕ_i . And d_i is the direction of angle of rotation, which indicates the direction of rotation is

$$d_i = \begin{cases} -1, & \text{if} \\ \end{cases}$$

(7)

Fig. 1: Rotation of vector [X,Y] by ϕ degrees.

To concatenate angles ϕ , ($i=0,1,2, \dots, N-1$) and to Now the equation (5), can be represented as below: $X_{i+1} = \cos(\phi_i) (X_i - d_i \cdot Y_i \cdot 2^{-i})$

evaluate the angle $\phi = \sum_{i=1}^n \theta_{-i}$. The input and output to the $Y_{i+1} = \cos(\phi_i) (Y_i + d_i \cdot X_i \cdot 2^{-i})$

$Z_{i+1} = Z_i - d_i \cdot 2^{-i}$ (8)
rotation by ϕ_i with $[X_i, Y_i]$ and $[X_{i+1}, Y_{i+1}]$.

$$\begin{aligned} X_{i+1} &= X_i \cos(\phi_i) - Y_i \sin(\phi_i) \\ Y_{i+1} &= Y_i \cos(\phi_i) + X_i \sin(\phi_i) \end{aligned} \tag{2}$$

In the above equation, common term $\cos(\phi_i)$, and the equations can be rewritten as,

$$X_{i+1} = \cos(\phi_i) (X_i - Y_i \sin(\phi_i) / \cos(\phi_i)) \quad Y_{i+1} = \cos(\phi_i) (Y_i + X_i \sin(\phi_i) / \cos(\phi_i)) \tag{3}$$

B. Gain Compensation

To concatenate several rotations, it requires lots of multiplications because equation (5) contains $\cos(\phi_i)$ term. To solve this problem we have to consider that

$$\phi_i = \arctan(2^{-i}), \quad i \in \{0, 1, 2, \dots\}$$

And

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We know that, $\sin/\cos = \tan$, so we can place \tan in the above equation as given below:

$$\begin{aligned} X_{i+1} &= \cos(\phi_i) (X_i - Y_i \tan(\phi_i)) \\ Y_{i+1} &= \cos(\phi_i) (Y_i + X_i \tan(\phi_i)) \end{aligned} \tag{4}$$

Where $\tan(\phi_i) = \pm 2^{-i}, (i=0,1,2, \dots, N-1)$.

Under this condition, the above equation becomes $\cos(\phi_i) = \cos(\arctan(2^{-i})) =$

because, we know that

$$\cos(x) = \pm \frac{1}{\sqrt{1 + \tan^2 x}} = \frac{1}{\sqrt{1 + 2^{-2i}}}$$

1

$$X_{i+1} = \cos(\theta_i) (X_i - Y_i \cdot 2^{-i})$$

$$Y_{i+1} = \cos(\theta_i) (Y_i + X_i \cdot 2^{-i})$$

(5) Now, to divide equation (8) by $\cos(\theta_i) =$

which gives, $1 + 2^{-2i}$

$$X_{i+1} \cdot a_i = X_i - d_i \cdot Y_i \cdot 2^{-i} \cdot Y_{i+1}$$

$$a_i = Y_i + d_i \cdot X_i \cdot 2^{-i}$$

Where $a_i = 1 + 2^{-2i}$. At the right side the computation is performed as shift-and-addition parts. So the amplified gain a_i is obtained x_{i+1} and y_{i+1} .

The gain is compensated by multiplying a constant A_i on both sides. Let $A_{i+1} = a_i A_i$. The recursive equations are obtained as

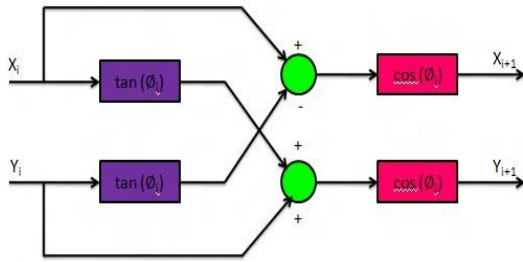


Fig. 2: Organizing computations of the transform. For some specific angle θ_i , multiplication by $\tan(\theta_i)$ can be replaced by an arithmetic shift and some sign multiplication.

A. Determining Rotation Directions

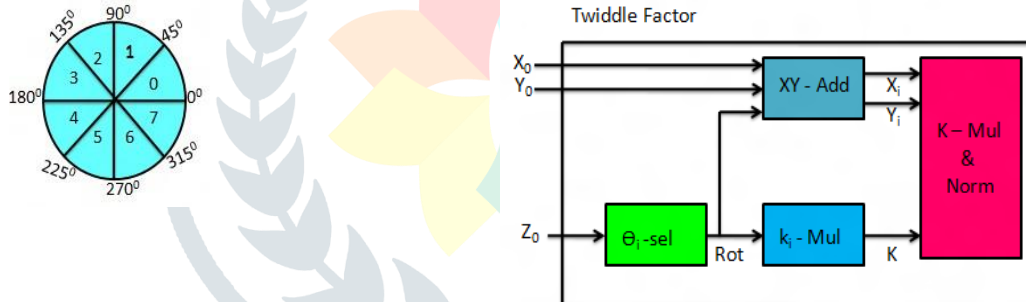
Define For the composite rotation of an angle θ is uniquely defined by the elementary rotation direction is sequence $(d_0, d_1, \dots, d_{N-1})$.

An angle accumulator is used to determine the sequence. The accumulator accumulates the elementary rotation angles, $X_{i+1} \cdot A_{i+1} = X_i A_i - d_i \cdot Y_i A_i \cdot 2^{-i}$ $Y_{i+1} \cdot A_{i+1} = Y_i A_i + d_i \cdot X_i A_i \cdot 2^{-i}$

By equating, the above steps in N iterations. The Gain can be calculated by using the equation given below.

$$A_N = \prod_{i=0}^{N-1} \sqrt{1 + 2^{-2i}}$$

In this method, the scale factors are considered for computations during iterations. So that, the process is complicated and occupies more memory. The whole process will be stopped, when the Z value is larger than the threshold value.



segment	correction	segment	correction
0	$\sin\theta_0$ $\cos\theta_0$	4	$\sin\theta_4 = -\sin\theta_0$ $\cos\theta_4 = -\cos\theta_0$
1	$\sin\theta_1 = \cos\theta_0$ $\cos\theta_1 = \sin\theta_0$	5	$\sin\theta_5 = -\cos\theta_0$ $\cos\theta_5 = -\sin\theta_0$
2	$\sin\theta_2 = \cos\theta_0$ $\cos\theta_2 = -\sin\theta_0$	6	$\sin\theta_6 = -\cos\theta_0$ $\cos\theta_6 = \sin\theta_0$
3	$\sin\theta_3 = \sin\theta_0$ $\cos\theta_3 = -\cos\theta_0$	7	$\sin\theta_7 = -\sin\theta_0$ $\cos\theta_7 = \cos\theta_0$

Fig. 3: 8-segment normalized angles for the ACor method.

The input angle has range of [00 to 450] for the applied ACor algorithm is noted. If the range is extended then it should be normalized. From the figure // explains about the 8-segment trigonometric circle and by using simple trigonometric transformation the change of angle from other segment to zeroth-segment. Table I. The first 16 iteration values of $\tan(\phi)$, and ϕ .

i	$\tan(\phi) = 2^{-i}$	$\phi = \arctan(2^{-i})$
0	1	45.000000000
1	1/2	26.565051177
2	1/4	14.036243468
3	1/8	7.125016349
4	1/16	3.576334375
5	1/32	1.789910608
6	1/64	0.895173710
7	1/128	0.447614171
8	1/256	0.223810500
9	1/512	0.111905677
10	1/1024	0.0559552892
11	1/2048	0.027976453
12	1/4096	0.013988227
13	1/8192	0.006994114
14	1/16384	0.003497057
15	1/32768	0.001748528

III. FFT TWIDDLE FACTOR ARCHITECTURE

The total processing time is reduced by reducing the total number of iterations so that the values in the Look-Up-Table and the accuracy performance will be less. By limiting the number of iterations, the trade-off between the accuracy and timing resources. Fig. 4: Twiddle Factor Architecture overview.

The above figure consists of 4 important modules that is Θ_i – selection (Θ sel), X-Y iteration addition (XY-Add), micro-length factor k_i iteration multiplication (k_i -Mul), and length-factor k multiplication and output normalization (K - Mul and Norm).

The process starts with Θ_i – sel module, which receives Z_0 as new input value. The micro rotation series is selected by the Θ_i – sel module and XY – Add and k_i – Mul are used to transmit the Rot values. The XY – Add and k_i – Mul modules receives a single value at each clock operation and then the iterative computation process X_i – Y_i and k_i respectively. The XY - Add modules also requires the initial values X_0 and Y_0 as shown in the figure. In the next clock operation Θ_i – sel module as used to transmit the Rot value. By using the two modules the final values of X_i – Y_i and the length factor K is obtained.

Table II. 8-Segment information for data recovery

Segment	Angle Norm	X-Y swap		reversed	
		Input	Output	X	Y
0	z_0	No	No	No	No
1	$\pi/2-z_0$	Yes	No	Yes	No
2	$z_0-\pi/2$	No	Yes	Yes	No
3	$\pi-z_0$	Yes	Yes	Yes	Yes
4	$z_0-\pi$	No	No	Yes	Yes
5	$3\pi/2-z_0$	Yes	No	No	Yes
6	$z_0-3\pi/2$	No	Yes	No	No
7	$2\pi-z_0$	Yes	Yes	No	No

As the ACor range is [0-45], other than the ranges values must be normalized as shown in table 2. Z_0 is used to modify the input values X_0 and Y_0 . If necessary the input and output values can be swapped and sine can be reversed.

A. Θ_i -Sel module Block

The Θ_i – sel modules are the Z-Normalized, Arithmetic Logic Unit (ALU), Absolute Value Modifier (ABS), Set rotation (SetRot), Θ_i look-up table (Θ_i -LUT), and the input angle Z_0 can be normalized by using the controller. The results of ALU can be positive to by Add/sub the current Z_i with the Θ_i value.

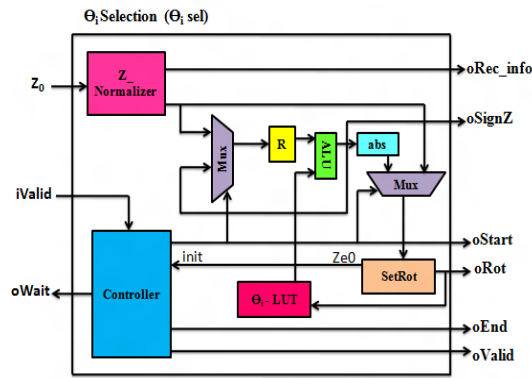


Fig. 5. Block diagram for Θ_i -Sel module.

If necessary the input angle of z_0 is normalized by Z_Normalizer to the zeroth –segment from the table-II. The normalized angle is the NormZ signal and the oRec_info signal will carry recovery information.

The next z_i value is evaluated by adding/subtracting the current value z_i at the ALU and the register with Θ_i -LUT forms appropriate Θ_i value. By using abs module the ALU output can be changed to positive value and at the outside oSignZ signal is transferred as signed outside.

IV. RESULTS

The simulation is carried out in Xilinx ISIM Tool and the synthesis is performed in Xilinx ISE 14.5 Tool for Spartan3E FPGA Family with Device XC3S500E, Package of FG320 and Speed Grade of -5. The design utilizes 81 slices out of 4656 slices, 0 LUTs out of 9312 LUTs and has a combinational path delay of 12.047ns as shown in Figure 6. The corresponding RTL and Technology Schematics are shown in figures 7 and 8 respectively. The simulation result is shown in figure 9, where the input given is 3F49, for which as per the design, the output obtained is 3F49.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	81	63288	0%
Number of fully used LUT-FF pairs	0	81	0%
Number of bonded IOBs	75	498	15%
Number of BUFG, BUFGCTRL, BUFGPCEs	1	16	6%

Fig.6. Device Utilization Summary Θ_i -Sel module.

RTL and Technology Schematics as Separate Figures (7&8).

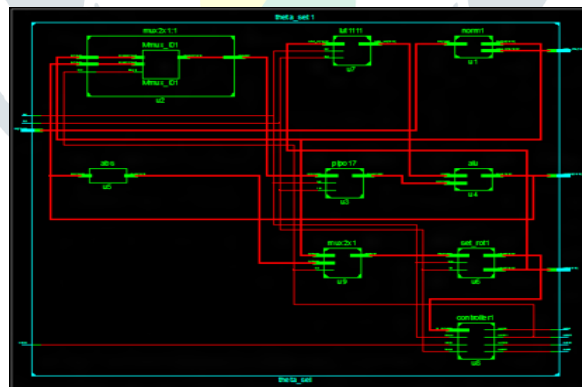


Fig. 7. RTL Schematic for Θ_i -Sel module.

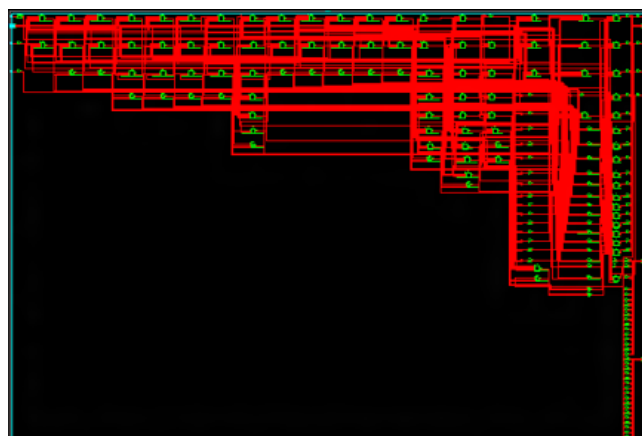
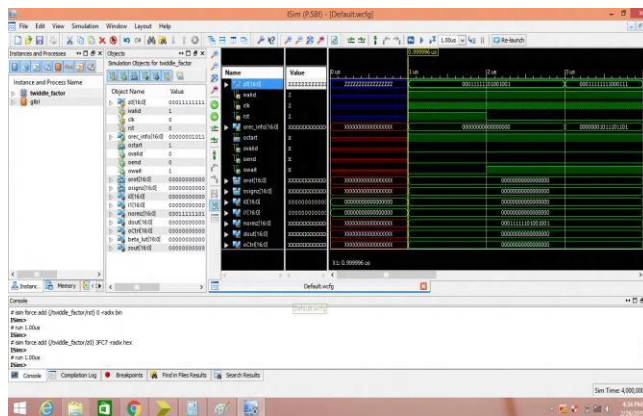


Fig. 8. Technology Schematic for Θ_i -Sel module.

Fig. 9. Simulation Results for Θ -Sel module.

V. CONCLUSION

The design of theta I sel block was implemented in this paper. Adaptive CORDIC (ACor) algorithm is a decision making algorithm so that, it reduces the number of iterations which in turns reduces the latency compare to the conventional CORDIC algorithm.

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