Modeling and Analysis of reduced Switch Multi level Inverter with Different Pulse Width Modulation Techniques

Akhilesh Gandhi
Dept. of Electrical Engineering SVIT, Vasad
Gujarat

Prof. Rakesh Gajjar
Dept. of Electrical Engineering SVIT, Vasad
Gujarat

***Abstract*— Now days Power electronic inverters are becoming trendy for various Industrial drives, UPS, HVDC transmission system & Induction heating. Bipolar inverter Are less efficient, costly, and high switching losses. To overcome these demerits, Multilevel Inverters are used. The Multi-level inverter output voltage response having a smaller number of harmonics compared to output voltage of the unadventurous bi-polar inverter. As Voltage level increases, number of power semiconductor switches also increases. It further increases cost, size and complexity in control. To obtain higher level of voltage with number of switches reduce, new multi-level inverter topology with reduced number of power semi-conductor switches is obtainable. The Multilevel Inverter proposed here uses a smaller number of switches compared to conventional topologies. Hence provides lower switching losses and economically advantageous unit than conventional cascaded H-bridge inverter. The topology suggested here is simulated using level shift and phase shift carrier pulse width modulation technique.**

Keywords—Multi-level inverter, Fundamental switching, Power-electronic switches

I. INTRODUCTION

In the cutting-edge time, enterprises and home buyers are requesting electric supply with greater dependability and power quality. Basically, two-level inverters are not ready to give pure power according to the buyers' necessities. Along these lines, multilevel inverters are getting to be increasingly main-stream as their strength to create voltage with fewer harmonic. MLI majorly used in sustainable power sources, dynamic channel, static compensator so on. Major advantage of these in the ventures makes it to be selected as a develop invention [1]. Previously, two level VSI were classifiably utilized producing just two levels in output voltage. These inverters are worked at high repetition to decrease the wave impurities in out-put voltage wave- form yet need of electronic switches and extended exchanging misfortunes are the important disservice of these inverters. In multilevel inverter high voltage can be acquired with the assistance of low voltage rating power gadgets. There are three sorts of ordinary multilevel inverter topologies: Neutral point clamped, flying capacitor and fell H-connect multilevel inverter [2]. From the three above MLI topologies, fell H-connect is main because of its straight forwardness in charge, particular structure and no need of additional capacitor and diode. Fell H-connect MLI can be divided in two classes: symmetrical and asymmetrical configuration. In symmetrical topology all unit will have same estimation of dc voltage sources. In lopsided topology distinctive unit will have diverse estimation of dc voltage sources, parallel or trinary relying upon necessity. By utilizing diverse voltage sources and expanding the extent of dc voltage sources, increasingly level can be created in yield voltage. Consequently, hitter kilter multilevel inverters produce higher number of levels in yield voltage utilizing fewer power electronic gadgets when contrasted with the symmetrical multilevel inverter.

In multilevel inverter the essential guideline is to use low voltage switches for getting high output voltage by partitioning the supply voltage among the power electronic switches. As of late, numerous topologies were introduced and can be isolated in numerous gatherings. To start with, in which the output voltage is not exactly the total of the greatness of the info dc voltage sources. Second, in which yield voltage greatness is equivalent to the aggregate of size of different info voltage sources as symmetrical and awry topology. Third [3]-[4], in these structure sizes of yield voltage is more prominent than the entirety of extent of different information voltage sources. This is finished by utilizing an additional capacitor which by charging and releasing builds the estimation of info dc voltage sources. Be that as it may, utilization of complex control procedure for controlling the charging and releasing of capacitor, is a major test. Utilization of additional control electronic switches, dc voltage sources and complex control strategy are the different key components for selecting the specific topology.

In [5], a lopsided topology is displayed which utilizes one voltage sources and two switches as fundamental unit. For producing increasingly level in yield voltage, one more dc voltage source and a switch is associated with the essential unit. Numerous units, with various dc voltage sources extent can be associated in arrangement to accomplish progressively level. Be that as it may, utilization of substantial number of unidirectional and bidirectional switches makes MLI cumbersome one. The multilevel inverter proposed in [6], utilizes a blend of single bidirectional switch with one dc voltage source and two capacitors as a fundamental unit. This fundamental unit

produces positive level as it were. By falling the fundamental unit higher of level in yield voltage can be produced. By utilizing a full H-connect inverter cell, negative level is likewise gotten. However, utilization of bidirectional switch builds the expense of the inverter. In [7], symmetrical and deviated topology for MLI is proposed. Be that as it may, this topology required countless just as bidirectional switches for producing the required level in yield voltage. The multilevel inverter proposed in [8], utilizes dc voltage sources with same size and unidirectional switches. Yet, a substantial number of intensity electronic switches and dc voltage sources are required for producing progressively level in yield voltage. Here, another multilevel inverter topology for single stage 5 – level and 7-level are proposed utilizing two dc voltage sources and six power electronic switches. The proposed MLI topology is contrasted with a few MLI topologies with explore its predominance. At last, the execution of the proposed topology is affirmed by reproduction in MATLAB condition for proposed inverter. The proposed topology can likewise be utilized for three stage frameworks.

II. ASYMMETRIC COURSE STAGGERED INVERTER(ACMLI)

The Hilter kilter topologies have two unique sorts named ACMLI and Deviated Crossover AHMLI. The primary distinction of AHMLI as for the ACMLI is the exchanging gadgets. H-Scaffold cells are shaped utilizing same semi-conductors in ACMLI, for example, transistor family. Then again, in AHMLI topology, cells are shaped with various semiconductors, for example, transistor family. On the off chance that the amount of DC sources in any topsy-turvy topologies organized as the twice of past one, the topology is named paired structure; on the off chance that it is multiple times more noteworthy as per past, the topology known as trinary structure. The figuring of yield voltage level is given in eq.1 for double structure and in eq.2 for trinary structure. "N" is the yield voltage level and "n" is the cell number in eq.1 and eq.2, where the "k" parameter is a whole number [10].

$$N_{binary} = 2^{n+1} - 1 \qquad V_{dc} = V / 2^{k-1}, k = 1, 2, \ldots, n \qquad (1)$$

$$N_{trinary} = 3^{n} \qquad V_{dc} = V / 3^{k-1}, k = 1, 2, \ldots, n \qquad (2)$$

II. MODULATION TECHNIQUES

In MCPWM, (m-l) transporters are utilized to contrast and the adjustment motion in an m-level inverter [1]. There are six triangular bearer signals for 7 level AC-MLI inverter in the MCPWM regulation. The periods of triangular bearer signals are changed and these signs are put vertically in PD- PWM, Case PWM and APOD-PWM. The tri-angular waves are contrasted and one sinusoidal flag at various adequacy. Another MC-PWM strategy is known as PS-PWM. Transporter signals are set evenly in various stages. PSPWM has likewise n-1 transporters and stage contrast of each stage is determined with 180/n for n-level yield.

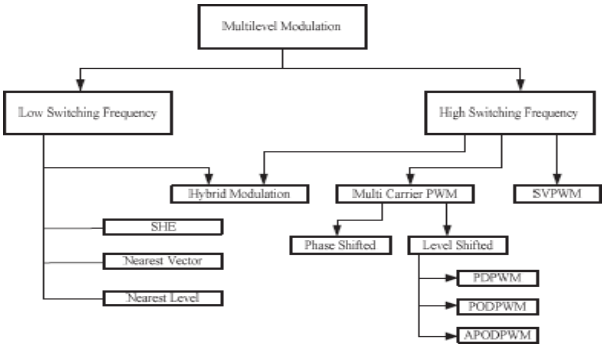

Fig.1 classification of modulation techniques

III. SIMULATION

1. SIMULATION OF CHB-MLI TOPOLOGY USING LEVEL SHIFT METHOD:

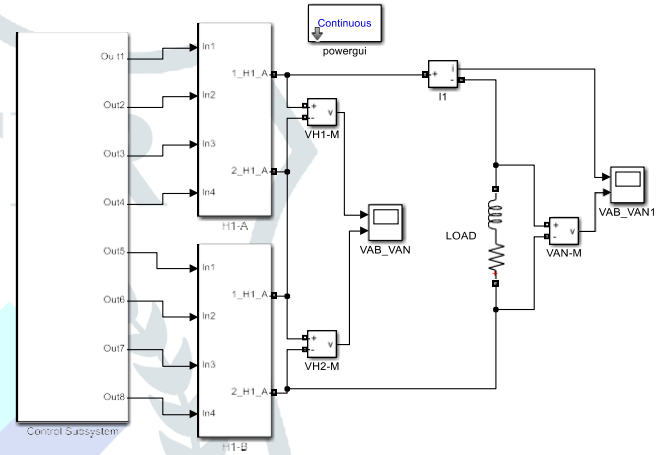

Fig.2 Simulink model of CHB-MLI topology

2. SIMULATION OF CHB-MLI TOPOLOGY USING PHASE SHIFT METHOD

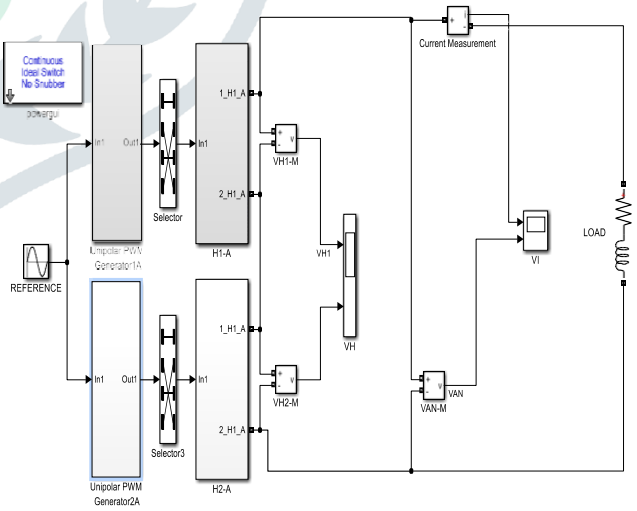

Fig.3Simulink model of CHB-MLI topology

3. SIMULATION OF PROPOSED TOPOLOGY(5-Level):

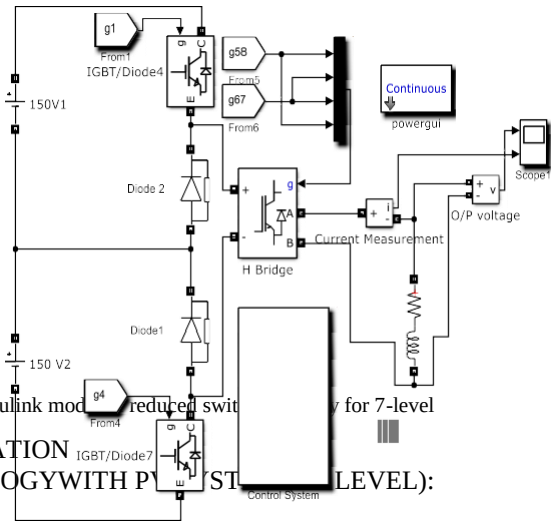

Fig.6 Simulink mod reduced swit for 7-level

6. SIMULATION IGBT/Diode7 OF REDUCED SWITCH TOPOLOGYWITH P ST LEVEL):

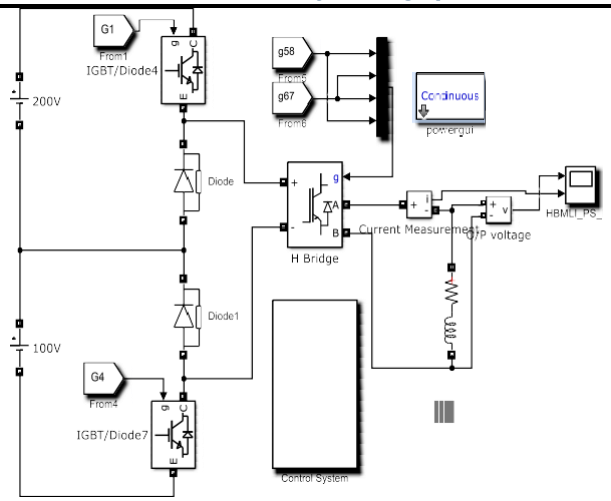

Fig.4 Simulink model of proposed topology(5-level)

4. SIMULATION OF REDUCED SWITCH TOPOLOGY WITH PV SYSTEM (5 – LEVEL):

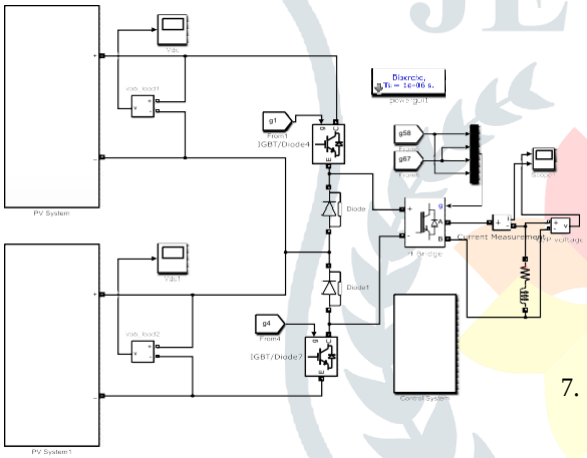

Fig.5 Simulink model of proposed topology with PV system(5-level)

5. SIMULATION OF PROPOSED TOPOLOGY(7-LEVEL):

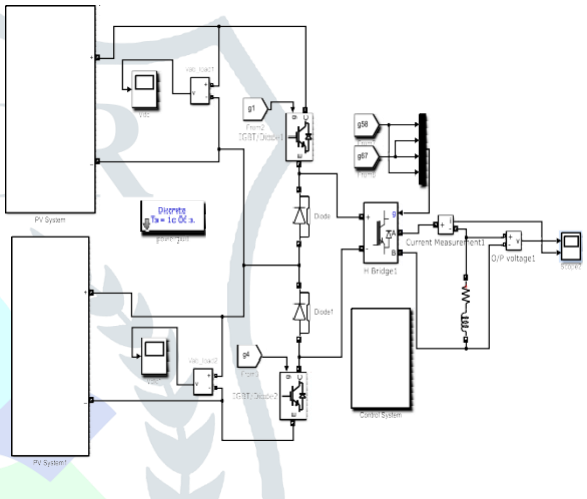

Fig.7 Simulink model of proposed topology with PV system (7 level)

7. SIMULATION OF LEVEL SHIFT METHOD FOR PROPOSED TOPOLOGY:

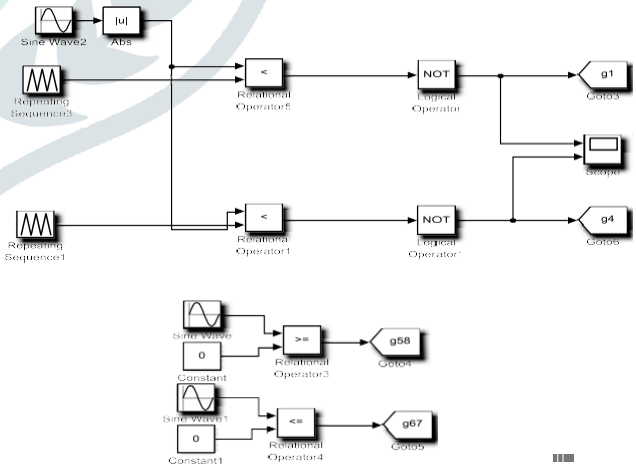

Fig.8 Simulink model of level shift method for proposed topology

8. SIMULATION OF PROPOSED TOPOLOGY WITH PHASE SHIFT METHOD:

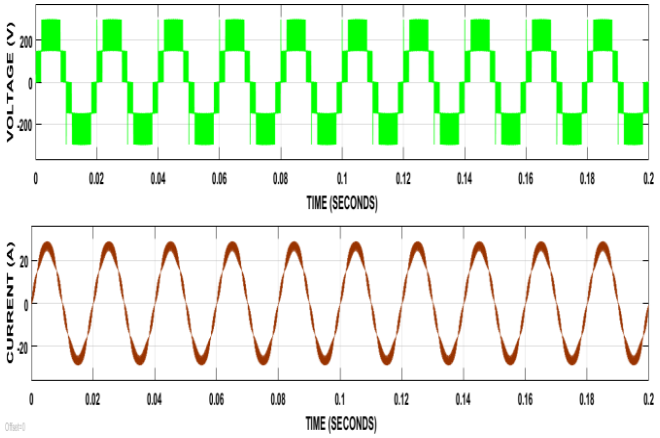

Fig.9 Simulink model of phase shift method for proposed topology

9. SWITCHING TABLE OF PROPOSED TOPOLOGY (5-LEVEL):

Table.1 switching pattern for proposed topology (5-level)

V_{OUTS}	S_1	S_4	S_5 & S_8	S_6 & S_7
2V	1	1	1	0
V	1	0	1	0
0	0	0	1	0
-V	1	0	0	1
-2V	1	1	0	1

10. SWITCHING TABLE OF PROPOSED TOPOLOGY (7-LEVEL):

Table.2 switching pattern for proposed topology (7-level)

V_{OUTS}	S_1	S_4	S_5 & S_8	S_6 & S_7
3V	1	1	1	0
2V	1	0	1	0
V	0	1	1	0
0	0	0	1	0
-V	0	1	0	1
-2V	1	0	0	1
-3V	1	1	1	0

IV. RESULTS

11. OUTPUT WAVEFORM OF PROPOSED TOPOLOGY USING LEVEL SHIFT METHOD:

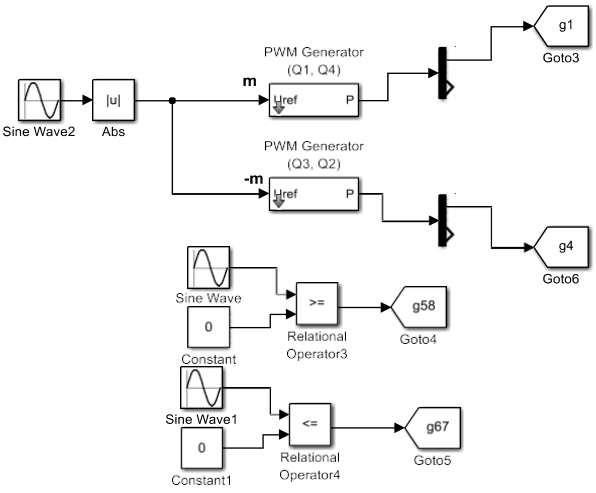

Fig.10 output waveform of proposed topology using level shift method (5-level)

12. OUTPUT WAVEFORM OF PROPOSED TOPOLOGY USING PHASE SHIFT METHOD:

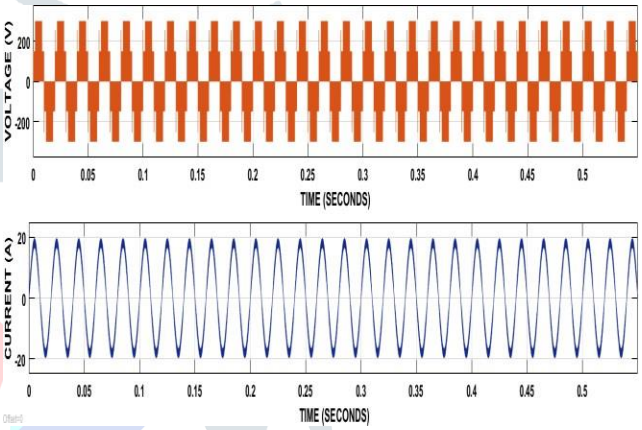

Fig.11 output waveform of proposed topology using phase shift method (5-level)

13. OUTPUT RESPONSE OF PROPOSED TOPOLOGY WITH PV SYSTEM (PS- METHOD):

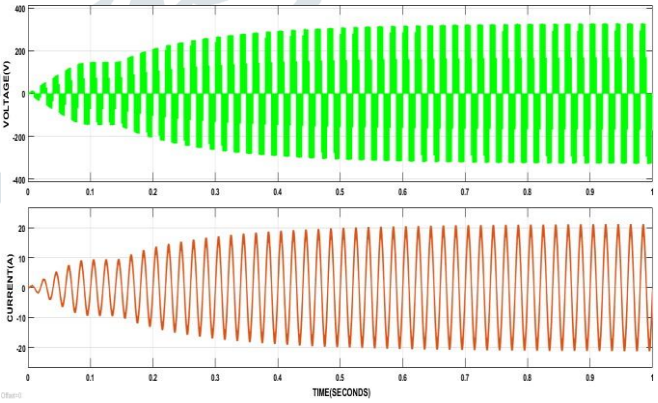

Fig.12 output waveform of proposed topology with PV-system using phase shift method (5-level)

14. OUTPUT WAVEFORM OF PROPOSEDTOPOLOGY WITH PV SYSTEM USING LEVEL SHIFT METHOD (7-

LEVEL):

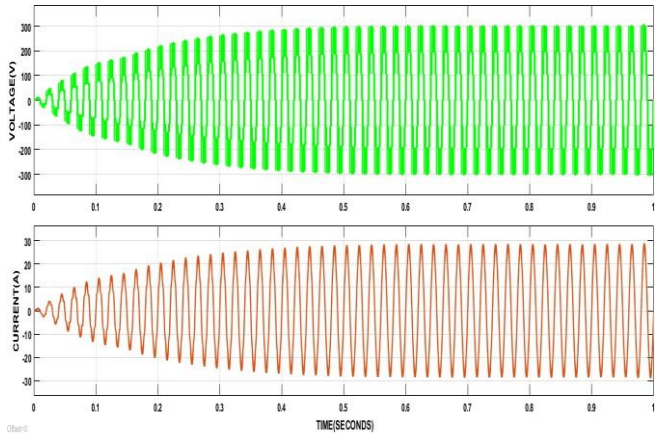

Fig.13 output waveform of reduced switch with PV- system using level shift method (7-level)

15. OUTPUT WAVEFORM OF PROPOSED TOPOLOGY WITH PV SYSTEM USING PHASE SHIFT METHOD (7-LEVEL):

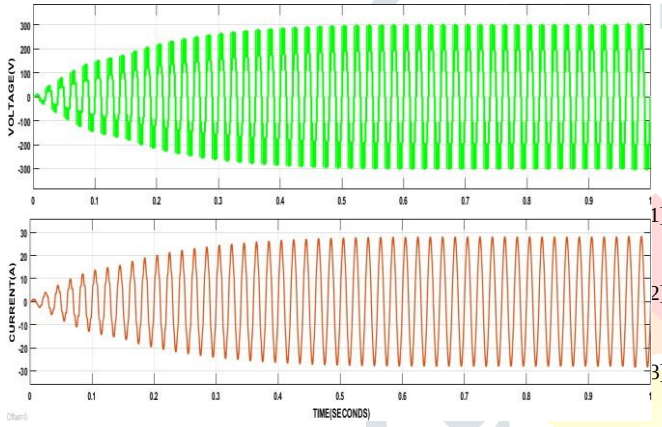

Fig.14 output waveform of reduced switch with PV-system using phase shift method (7-level)

A. COMPARISION OF 5-LEVEL TOPOLOGIES:

Table.3 comparison of PS and LS method (5-level)

TOPOLOGY	NO. OF SWITCH	NO. OF SOURCE	THD (O/P CURRENT)	OUTPUT VOLTAGE GAIN	NO. OF COMPONENTS (CAPACITOR & DIODE)
DCMLI	8	1	21.73	0.5	10
CHB-MLI	8	2	15.03	1	0
HBMLI	6	2	8.40	1	2

TOPOLOGY	NO. OF SWITCH	NO. OF SOURCE	THD (O/P CURRENT)	OUTPUT VOLTAGE GAIN	NO. OF COMPONENTS (CAPACITOR & DIODE)
DCMLI	8	1	20.34	0.5	10
CHB-MLI	8	2	2.57	1	0
HBMLI	6	2	7.29	1	2

B. COMPARISION OF 7-LEVEL TOPOLOGIES

Table.4 comparison of PS and LS method (7-level)

TOPOLOGY	NO. OF SWITCH	NO. OF SOURCE	THD (O/P CURRENT) %	OUTPUT VOLTAGE GAIN	NO. OF COMPONENTS (CAPACITOR & DIODE)
CHB-MLI	8	3	6.67	2	0
HBMLI	6	2	2.78	2	2
HBMLI-PV	6	2	3.67	2	2

TOPOLOGY	NO. OF SWITCH	NO. OF SOURCE	THD (O/P CURRENT) %	OUTPUT VOLTAGE GAIN	NO. OF COMPONENTS (CAPACITOR & DIODE)
CHB-MLI	8	3	1.06	2	0
HBMLI	6	2	1.44	2	2
HBMLI-PV	6	2	2.65	2	2

VI. CONCLUSION

In this paper, simulation of a reduced multilevel inverter topologyfor 5-level & 7-level is done. from this simulation it is very clear that THD of output waveform is very less in phase shift method compare to level shift method. 7-level reduced topology have also less switches compare to conventional topology.

REFERENCES

[1] Kouro, S., Malinowski, M., Gopakumar, K., et al.: 'Recent advances and industrial applications of multilevel converters', IEEE Trans.Ind.Electron, 57, (8), pp. 2553–2580, 2010.

[2] Jose Rodriguez, J S Lai, and F. Z. Peng, "Multilevel Inverters: ASurvey of Topologies, Controls, and Applications", IEEE Trans. OnIndustrial Electronics, vol. 49, no. 4, pp. 724-738, August2002.

[3] Y. Hinago and H. Koizumi, "A Switched-Capacitor Inverter UsingSeries/Parallel Conversion With Inductive Load," in IEEETransactions on Industrial Electronics, vol. 59, no. 2, pp. 878- 887,Feb. 2012.

[4] E. Babaei and S. S. Gowgani, "Hybrid Multilevel Inverter UsingSwitched Capacitor Units," in IEEE Transactions on IndustrialElectronics, vol. 61, no. 9, pp. 4614-4621, Sept. 2014.

[5] E. Babaei, "A Cascade Multilevel Converter Topology With ReducedNumber of Switches," in IEEE Transactions on Power Electronics, vol.23, no. 6, pp. 2657-2664, Nov. 2008.

[6] G.Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter and M. I.Gimenez, "A New Simplified Multilevel Inverter Topology forDC–AC Conversion," in IEEE Transactions on PowerElectronics, vol. 21, no. 5, pp. 1311-1319, Sept. 2006.

[7] M. Farhadi Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters,"IEEE Trans. Power Electron., vol. 28, no. 2, pp. 625–636, Feb. 2013.

[8] E. Najafi and A. H. M. Yatim, "Design and Implementation of a New Multilevel Inverter Topology," in IEEE Transactions on IndustrialElectronics, vol. 59, no. 11, pp. 4148-4154, Nov. 2011.