FAULT DETECTION IN COMBINATORIAL CIRCUITS USING ATPG

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Abstract*— The recent VLSI circuits development necessitate device miniaturization as well as intricate manufacturing for their fabrication. This however has led to greater process variation and higher probability of the defects and consequently has worsened yield. To improve the functionality of IC by removing the defects, there are various proposed ideas which reduces difficulty in identifying faults. Many ATPG algorithms were employed in olden days to improve IC functionality. To get better accuracy, we proposed an algorithm called pseudo random bit sequence(PRBS). Unlike existing methods, this technique does not use any diagnostic test generation, circuit modification or mitre-based approach. This is useful in analysing the performance level in terms of area, power and delay.

***Keywords*— fault detection, ATPG tools, PRBS, diagnostic test set, faulty location, test set generation.**

I. INTRODUCTION

The diagnosis problem has surfaced as being not only more difficult but also more important since the reason for low yield needs to be ascertained. at the net-list level and necessary corrections be made in the manufacturing process so as to enhance the yield. Diagnosis is also needed to enable the use of partially defective chips on the basis of the location of the defects. the various methods for faulty site locations that are employed during yield ramp up such as the traditional physical failure analysis and volume diagnosis depends on logical level processing called fault diagnosis. for effective fault detection ATPG tools provide test with high fault coverage and identify redundant faults in circuit-under test to a large extent, even though the underlying problem is known to be computationally hard. Generally the ATPG tools aim to minimize the size of the test set and maximize fault coverage.

The further sections includes the earlier research works in fault detection is discussed to know their efficiency and betterment attained in diagnosing and the proposed work will provide outcomes more than the previous ones. In brief, our proposed system includes that, the test vectors are randomized using random testing of vectors. Input vector is generated and stored in buffer. Test vectors from LUT are given to benchmark circuit where comparator functions to locate the defects in the integrated circuits.

II. LITERATURE SURVEY

A.TEST SET COMPACTION ALGORITHMS

The Idea was about presenting a new algorithm, essential fault reduction, for producing compact test sets for combinational circuits under the single stuck at fault model, and new heuristic for evaluating the base single stuck at fault test set size. These algorithms together with the dynamic compaction algorithm were combined into a advanced automatic test pattern generation system for combinational circuits, called Min Test . Min Test provided better lower limits and produced smaller test sets than the previous outcomes for the ISCAS85 and full output forms of the ISCAS89 benchmark circuits. The Essential Fault Reduction algorithm was employed to overcome the defects of EFP algorithm along with dynamic compaction called Min test was effective than the previous one. It found better lower bounds for generating test sets and reduce the test vectors.

B.AUTOMATIC DEFECT DIAGNOSIS

Logic defect diagnosis was to find the defect spots in a digital IC that fails testing. It was one of the basic advances during the process of manufacturing yield improvement. Automatic defect diagnosis techniques for circuits with single defect have been enhanced significantly. In any case, the technologies for multiple defect diagnosis are still inadequate. In this paper, they proposed a effective heuristic for diagnosing a full-sacle design with multiple defects. Concepts called curable vectors and curable outputs were incorporated. By combining these two measures as a grading criterion, each signal's possibility of being one of the defect spots was computed with a high accuracy.

C.BIST

. Logic BIST implements most ATE functions on chip so that the test cost can be reduced through less test time, less tester memory requirement, or a cheaper tester. Logic BIST applies a large number of test patterns so that more defects, either modelled or un-modelled, can be detected.

D.MATRIX CODES

Matrix codes were introduced. Due to the need, a technique is introduced to secure memories against multiple bit upsets and to enhance manufacturing yield. The proposed strategy, called a Matrix code, joins Hamming, Parity codes to guarantee the change of unwavering quality and yield of the memory contributes the nearness of high deformities and numerous bit-upsets. The technique was assessed utilizing flaw infusion tests. The outcomes were contrasted with understood procedures, for example, Reed– Muller and hamming codes. The proposed system performed superior to anything the Hamming codes and accomplishes that amount execution with Reed– Muller codes with extremely increased ideal usage, for example, 25% decrease in territory and power utilization. It additionally accomplished unwavering quality increment by over half sometimes. The matrix codes combined the Hamming and parity codes to improve reliability and yield of memory chips even in the presence of high defects and multiple bit upsets. It was employed for reducing memory size. It was applicable for high performance and low power applications. It corrected up to 3 errors.

E.GENETIC ALGORITHMS

In this paper an on-line multiple faults recognition approach was first of all proposed. For effectiveness, optimal designs of participation capacities were required. Consequently, the proposed approach was enhanced utilizing Particle Swarm Optimization (PSO) strategy. The contributions of the proposed approaches were residuals represented to the numerical evaluation of Analytical Redundancy Relations.. These residuals were produced because of the utilization of bond graph modeling. The consequences of the fuzzy recognition modules were shown as a hued causal graph. An examination between the outcomes got by utilizing PSO and those given by the utilization of Genetic Algorithms (GA) was finally made. The trials centered around a recreation of the three-tank pressure driven framework, a benchmark in the conclusion area.

F.HAMMING CODE

In 2015, due to radiation effects, errors caused in electronics devices have emerged as key reliability concerns. Blunders happen in VLSI circuits which are sent in atomic power plants because of radiation, temperature changes and so on. Reliability is a major concern in advanced electronic circuits. Defects caused for instance by radiation turns out to be more typical as technology scales. To guarantee that those mistakes don't influence the circuit usefulness a number of mitigation methods can be utilized. Among them, Error Correction Codes (ECC) were regularly used to secure recollections and registers in electronic circuits. Hamming code was one of such forward defect revising code which has numerous applications. In this paper the algorithm for hamming code is discussed about and its implementation of it in Verilog is done to get the outcomes. Hamming code is an improvement over parity check method. Here a code is implemented in Verilog in which 7-bit of data information is transmitted with 4-excess bits and it tells about single error correction and double error Detection (SECDED). To discover the estimation of these excess bits ,a code is composed in Verilog which will be simulated in Quartus 9 programming. To improve system reliability, it needs automatic error detection and correction circuit, at opening level single parity bits were used for the detection of error in the information, then multiple bits were used.

III. PROPOSED WORK

Automatic test pattern generation is the process of generating input patterns to test a circuit, These programs usually operate with a fault generator program, which creates the collapsed fault list. In many ATPG algorithms, we employed one is PSEUDO RANDOM BIT SEQUENCE ALGORITHM.

Many ATPG algorithms were employed in olden days to improve IC functionality. to get better accuracy, an algorithm called pseudo random bit sequence(PRBS) was proposed. unlike existing methods, this technique does not use any diagnostic test generation, circuit modification or miter-based approach. this is useful in analysing the performance level in terms of area, power and delay. Automatic test pattern generation is the process of generating input patterns to test a circuit, These programs usually operate with a fault generator program, which creates the collapsed fault list. In many ATPG algorithms, we employed one is PSEUDO RANDOM BIT SEQUENCE ALGORITHM. The disadvantages of the existing system such as Set of vector generation is not static for entire testing ,Testing produces faults under certain risk factors, It forms irregular pattern., High power consumption**.** Correction of errors detected is less.

A. *BLOCK DIAGRAM*

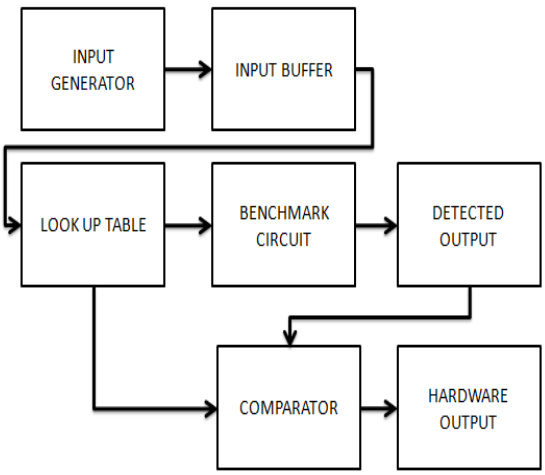

Figure 1.Block Diagram

B. *SCHEMATIC CIRCUIT*

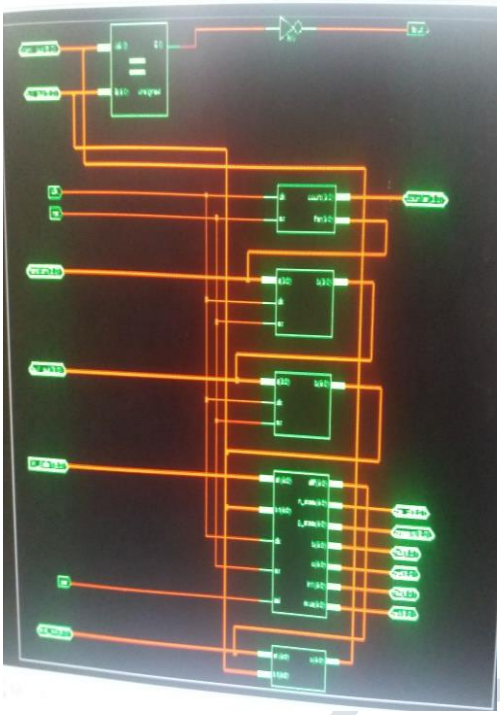

Figure 2. Schematic diagram

C. *MODULES DESCRIPTION*

INPUT GENERATOR

Input patterns are generated by automatic test pattern generator(ATPG). According to number of inputs, the input patterns are generated. Functional ATPG generate complete set of tests for circuit input-output combinations.

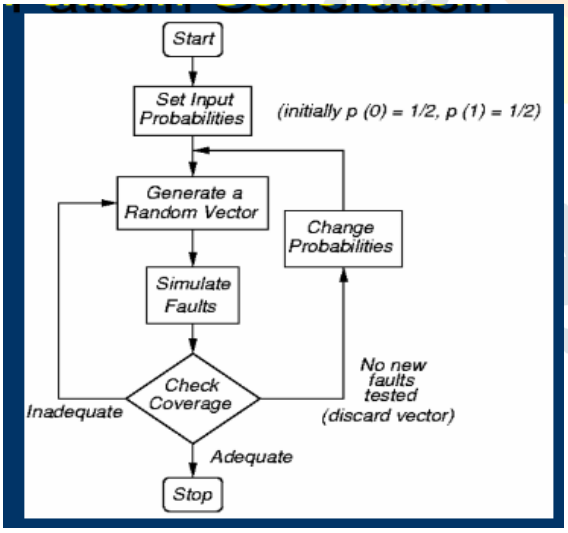

Figure 3.ATPG Process

INPUT BUFFER

The input patterns generated are usually stored in buffer (memory block). Linear feedback shift register is generally used for this purpose. To generate a binary sequence in random fashion, there is a need for storing large input combination so 4 bit LFSR is used.

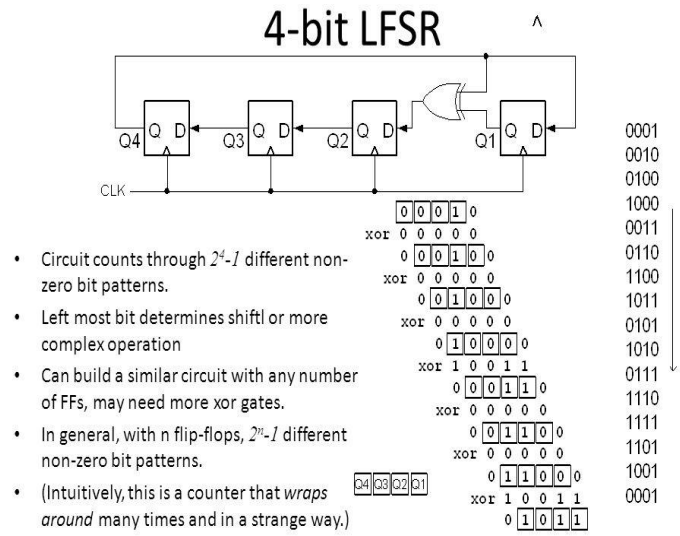

Figure 4.LFSR

LOOK-UP TABLE (LUT)

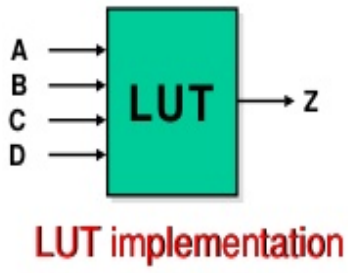

Figure 5. LUT

Look-up table with N inputs can be used to implement any combinational functions of N inputs. Look-up table is an array type and programmed with truth table. Address of this array is input functions and value is output patterns. Here multiplexing is done to choose a test vectors, therefore 4:1 mux is used.

BENCHMARK CIRCUIT

The ISCAS'85 benchmarks were collected and published to help in comparing automatic test generation (ATPG) tools. These are often used in combinational form, with all internal flops made into pseudo-primary inputs and outputs.

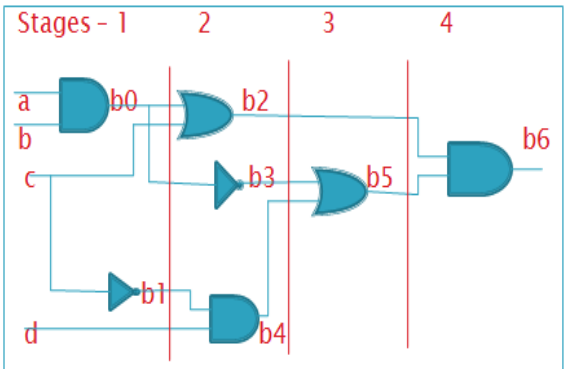

Figure 6.Benchmark Circuit

COMPARATOR

Comparator is generally used for comparing the values and based on the requirement, output gets displayed. Here, 2 bit comparator is used.

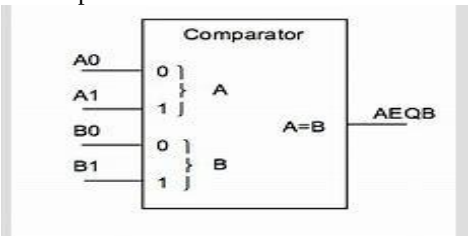

Figure 7. Comparator

Thereby, the fault bits are activated based on the comparator outputs on the FPGA kit.

D. *ALGORITHM*

Under ATPG, technically many algorithms are employed in the view of improving the performance of IC in one way or the other in an efficient manner. So, in order to improve the performance by accurate fault detection, lessening time, area and power consumption.

The proposed idea is about implementing PRBS algorithm for generating patterns in a binary sequence. The algorithm has following steps:

Step 1: Start the program.
Step 2: Get the inputs and generate the test vectors randomly.
Step 3: Inputs are stored in buffer**.**
Step 4: LUT is updated with generated test vectors**.**
Step 5: Benchmark circuit is selected and 4-bit inputs are given.
Step 6: The output detector detects the outputs of LUT.
Step 7: The desired output from LUT is compared with the LUT output.
Step 8: The faulty location is displayed corresponding to the comparator output.
Step 9: When they are equal
Output = 0 (LED will not blink)
When they are not equal
Output = 1(LED will blink)
Step 10: Stop the program.

It is described in a flow diagram

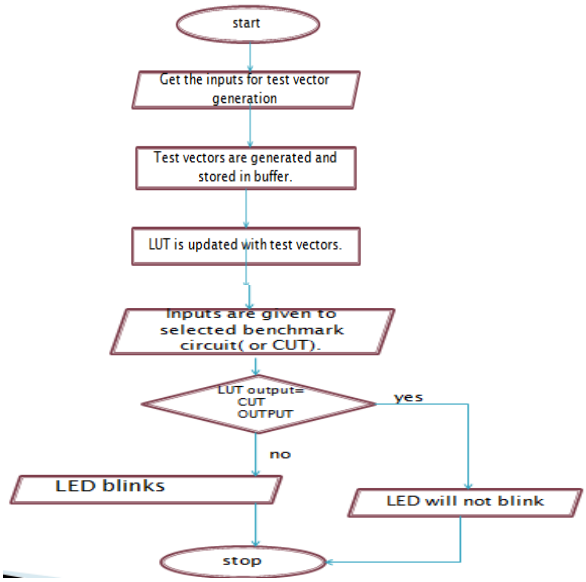

Figure 8.Proposed Flow Diagram

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IV. SPECIFICATION

SOFTWARE

A. *MODEL SIM*

Model sim altera 6.3_g_p1 version is used for simulation purpose in Xilinx ISE design environment. **ModelSim** is a multi-language HDL simulation environment by Mentor Graphics, for simulation of hardware description languages such as VHDL, Verilog and SystemC and includes a built-in C debugger. ModelSim can be used independently, or in conjunction with Intel Quartus Prime, Xilinx ISE or Xilinx Vivado

The main purposes of modelsim are

Logical verification,
behavioral verification and
post-place and route.

B. **Xilinx ISE**

Xilinx ISE (**I**ntegrated **S**ynthesis **E**nvironment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. Xilinx ISE is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors. The Xilinx ISE is primarily used for circuit synthesis and design, while ISIM or the ModelSim logic simulator is used for system-level testing **Xilinx ISE** (**I**ntegrated **S**ynthesis **E**nvironment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

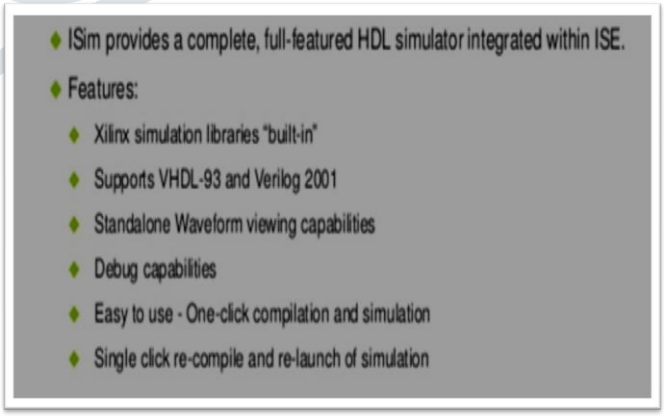
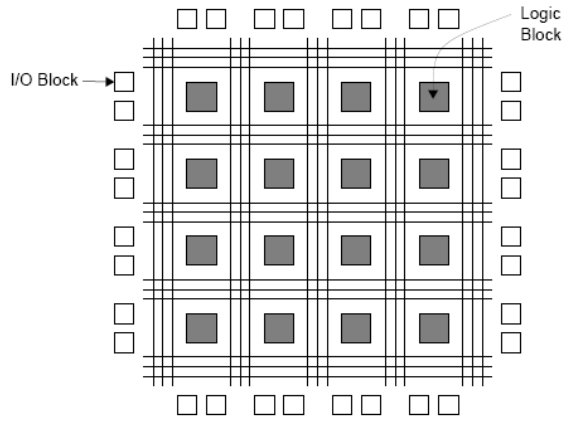


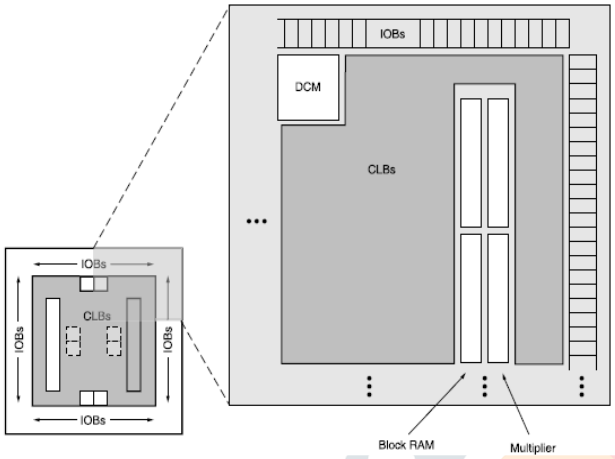
Figure 9. Xilinx ISE

HARDWARE

FPGA INTERNAL STRUCTURE



SPARTAN 3E ARCHITECTURE



Features:

- Very low cost, high-performance logic solution for high-volume, consumer-oriented applications.
- Proven advanced 90-nanometer process technology
- Multi-voltage, multi-standard Select IO interface pins
- Up to 376 I/O pins or 156 differential signal pairs
- LVCMOS, LVTTL, HSTL, and SSTL single-ended.

F. *CODING FORMAT*

VHDL is used to describe the model of a digital hardware. This model gives the external view and one or more internal views.

- ➢ Internal View: Gives the functionality of the structure.
- ➢ External view: Gives the interface of the device.

VHDL provides 5 different primary constructs called design units. They are:

- Entity declaration
- Architecture body
- Configuration declaration
- Package declaration
- Package body.

V. RESULTS

A. SIMULATION

when input is 1101001

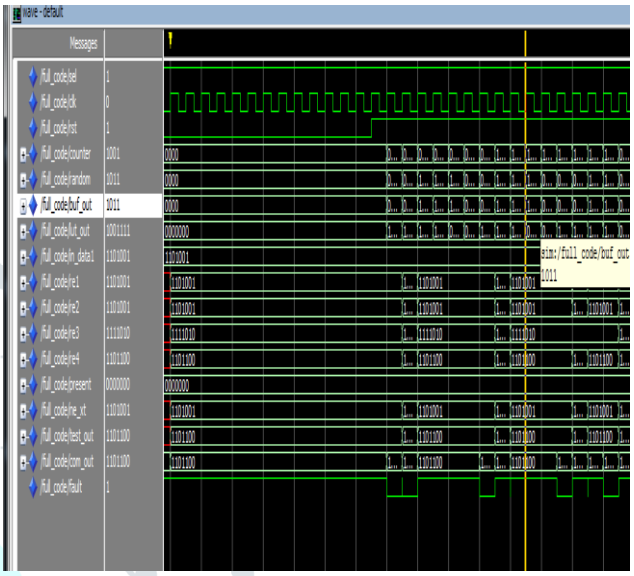


Figure 10.Output

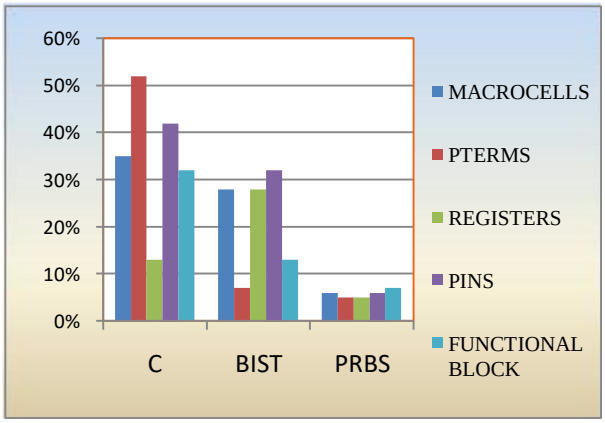
Comparison table

Comparison done between existing and proposed system

TECHN-IQUES	*MACRO CELL USE-D*	*P - TERM USED*	*REGISTER USED*	*PINS USED*	*FUNCT-IONAL BLOCK USED*
CHECK SUM	*35 %*	*52%*	*13%*	*42%*	*32%*
BIST	*28 %*	*7%*	*28%*	*32%*	*13%*
ATPG (PRBS)	*6%*	*5%*	*5%*	*6%*	*4%*

Table 1.Final Comparison properties

Comparison chart



. Figure 11.Final Comparison result

B. *HARDWARE RESULTS*

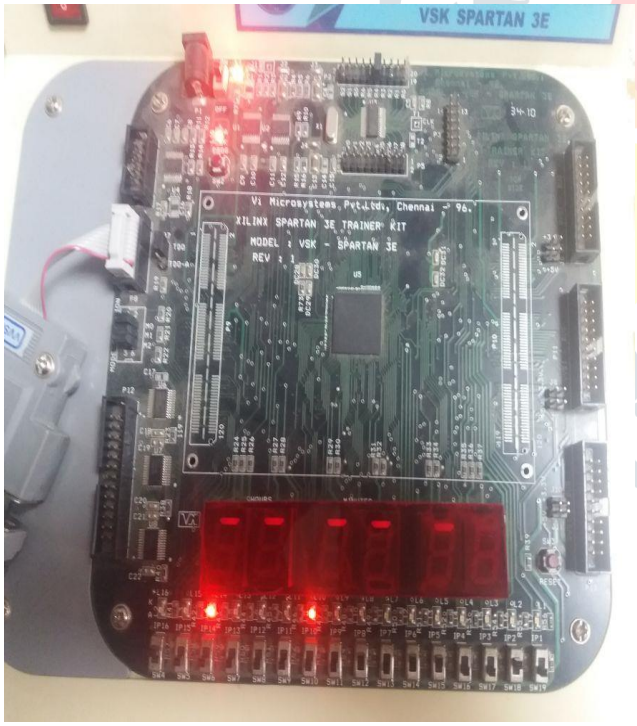


Figure 12.FPGA Output

VI. CONCLUSION

The diagnosis problem has surfaced as being not only more difficult but also more important since the reason for low yield needs to be ascertained. . for effective fault detection ATPG tools provide test with high fault coverage and identify redundant faults in circuit-under test to a large extent, even though the underlying problem is known to be computationally hard. generally the ATPG tools aim to minimize the size of the test set and maximize fault coverage. The various techniques are discussed and their efficiency is observed with their simulation results obtained on experiments. The proposed algorithm reduces the time and improves the accuracy than previous algorithms. This work implies that a simple ATPG based procedure is capable of producing random test patterns to reduce the time consumption, power consumption and delay. In general, ATPG method can be applied to all IC circuits to distinguish and locate the defects clearly. Thus the performance of the IC will be increased by reducing the power used for the input and outputs and fault location operations while reducing the area it consumes. This algorithm is experimented on the benchmark circuit and the observed output is tabulated their overall efficiency.

VII. FUTURE SCOPE

Fault coverage can be increased further and faults can also be corrected effectively under low power consumption and *delay.* Faults may be recovered while designing to simplify the complexity of locating the faults.

V. REFERENCES

[1] Ilker Hamzaoglu and Janak H. Patel “Test Set Compaction Algorithms for Combinational Circuits”IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, AUGUST 2000.

[2] Andreas Veneris, Robert Chang Magdy S. Abadir Mandana Amiri “Fault Equivalence and Diagnostic Test Generation using ATPG” ISCAS 2004.

[3] Yung-Chieh Lin, Feng Lu and Kwang-Ting Chen” Multiple-Fault Diagnosis Based On Adaptive Diagnostic Test Pattern Generation” IEEE TRANSACTIONSONCOMPUTER-AIDED DESIGN OF INTEGRATEDCIRCUITS ANDSYSTEMS, MAY 2007.

[4] Y. Zhang and V. D. Agrawal, “A diagnostic test generation system,” in Proc. ITC, Nov. 2010, pp. 1–

[5] Costas Argyrides, Dhiraj K. Pradhan and Taskin Kocak ” Matrix Codes for Reliable and Cost Efficient Memory Chips” IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION(VLSI) SYSTEMS, March 2011.

[6] Sunita M and Kanchana Bhaaskaran V "MATRIX CODE BASED MULTIPLE ERROR CORRECTION TECHNIQUE FOR N-BIT MEMORY DATA " International Journal of VLSI design & Communication Systems (VLSICS) , February 2013 .

[7] K.P. Sridhar, B. Vignesh, S. Saravanan, M. Lavanya and V. Vaithiyanathan "Design and Implementation of Neural Network Based circuits for VLSI testing" World Applied Sciences Journal 29 (Data Mining and Soft Computing Techniques): 113-117, 2014 ISSN 1818-4952 .

[8] Wei-Ting Kary Chien, Randy Kang* , Howking Sii, Ming Li "Predict VLSI Circuit Reliability Risks Using Neural Network" Universal Journal of Engineering Science 2(5): 116-123, 2014 .

[9] Mrs. K. Kalaivani1 , Dr. A. Sivagami "ERROR DETECTION AND CORRECTION USING HAMMING CODE IN VLSI DESIGN UNDER NUCLEAR ENVIRONMENT" International Journal For

Technological Research In Engineering, June-2015 .

[10] Manjari Pradhan and Bhargab B. Bhattacharya "COMEDI: Combinatorial Election of Diagnostic Vectors From Detection Test Sets for Logic Circuits"'IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, 2017.

[11] Imtiez Fliss and Moncef Tagina "Exploiting Particle Swarm Optimization in Multiple Faults Fuzzy Detection"JOURNAL OF COMPUTING, VOLUME 4, ISSUE 2, FEBRUARY 2012, ISSN 2151-9617 .

[12] Shi-Yu Huang "On Improving the Accuracy Of Multiple Defect Diagnosis".

[13] Yong Chang Kim Vishwani D. Agrawal Kewal K. Saluja "Multiple Faults: Modeling, Simulation and Test "7th ASPDAC and 15th Int'l Conf. on VLSI Design January 2002.