Study and Theoritical Investigations ofCMOS RF Power Amplifiers

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***Abstract*—Today's communication system has many of advanced features which gives faster rate of information trans-reception. The simplest high frequency transmitter has different blocks like sensor, modulator, LNA, oscillator, RF power amplifier and an antenna. Among these, the most hungry device is the RF Power Amplifier(PA)and its efficiency dominates the overall efficiency of the transmitter.One of the most challenging issues in the design of CMOS radio frequency(RF) transmitter is linearity requirement. Due to their large RF envelope fluctuation, modulation schemes such as QAM etc are more sensitive to the power amplifier nonlinearities,which is the major contributor of non linear distortion in a RF transmitter. An obvious solution is to operate the power amplifier in the linear region where the average output power is much smaller than the amplifier's saturation power. Use of CMOS technology will have the ability to shrink in size with low cost and better design results. PA can be designed on CMOS 130nm, 90nm, 45nm Technology with the advanced design system(ADS)tool with graphical results. This study paper helps us to design an efficient RF power amplifier(PA),to get an optimum output power.**

Index terms—Design, CMOS technology, output power, linearity, performance analysis, linearization techniques,power added efficiency(PAE).

INTRODUCTION

Thesuccess of the wireless telecommunication system in the commercial markets relies on the advancements in the technologies related to the low power, low cost and small size of RFICs. Thanks to the continuous scaling of CMOS transistor channel length, standard CMOS technologies are now used in the high frequency applications. As a result, it is now feasible to integrate analog circuits and digital circuits on a single die. A variety of architectures are used for RF CMOS transmitter implementation[2][3]. Each of them is well suited for a certain standard. The architecture for a particular standard has certain compatibility issues with another standard, especially where high performance is required. However, the flexibility of transmitter architectures is highly desired for multistandard operations. Highly integrated direct conversion architecture becomes popular due to the fact that this architecture can remove bulky and expensive off-chip component and simplify the overall RF system. Fig.1 shows the block diagram of a simple RF transmitter that includes: sensor, LNA, VCO, power amplifier, oscillator and an antenna.

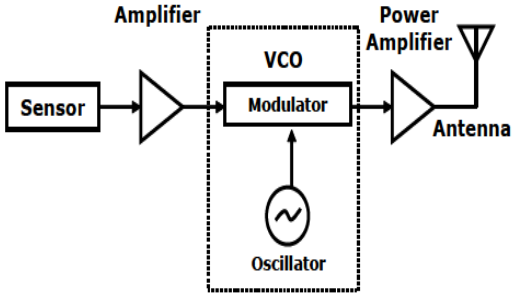


Figure 1:Block diagram of a RF transmitter

Researchers have been focusing on designing more efficient power amplification techniques. It has been shown that the power efficiency of traditional amplificationtechniques could be improved at a cost of linearity degradation,which may not be tolerable by the standards' requirements. The current state of the art is the design of a moderately linear PA with the additional implementation of a linearization technique [7]. To maximize power efficiency, the amplifier should operate as close to saturation as possible, with the linearization system maximizing the spectral efficiency in this near-saturated region.On one hand, the PA is most power consuming; for example, in a cellular phone, the battery life is largely determined by the power efficiency of the PA[1]. On the other hand, it is desirable to have the ability to transmit data at the highest possible rate for a given channel bandwidth, i.e., to have high spectral efficiency.

The first CMOS RF power amplifier which delivered the hundreds of MW power reported in 1997, implemented on the single ended configuration with 0.8 μm CMOS Technology, the power amplifier was able to give 62% drain efficiency of (824~ 849) MHz using the supply voltage of 2.5V. The first GHz range differential power amplifier was reported in 1998, implemented using 0.35 μm CMOS Technology. In 2001, 130 nm CMOS technology came into notice[4]. Today's Scientist working on 14 nm CMOS technology, in few years scale will down to 10 nm, which is very tiny. There is considerable industrial interest in producing RF PAs with good linearity and power efficiency. These two contradictory requirements can be achieved by using external circuitry to linearize an efficient amplifier. PAs must be linear to minimize interference and spectral re-growth. However, PAs generally have nonlinear behavior and are basically the main sources of distortion and nonlinearities in the RF transmitter[5].

This paper reports the classification of RF PAs in section II. The following section III presents the different characteristics of RF PAs. The various linearization techniques is discussed in section IV. Importance and challenges of CMOS technology used in RF PAs is presented in section V. In section VI, VII the applications and design procedures of RF Pas are discussed respectively. The related works on RF CMOS PAs are reported in section VIII. The conclusion and references of PAs are specified in section IX and X respectively.

II.CLASSIFICATION OF RF PAs

Figure 2 shows the various classification of PAs. There are two modes of the power amplifier used for two different operations. They are i. Current Source PAs and ii. Switch Mode PAs.

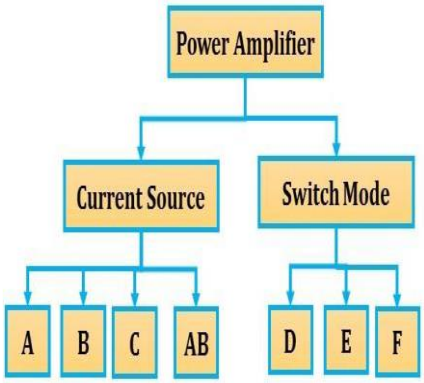


Figure 2: Classification of RF Power Amplifiers

i. Current Source PAs

The classes A, B, C, and AB are considered as a constant current source PAs. The drawback of power dissipation is more in these amplifiers.A class-A power amplifier, in principle, works as a small-signal amplifier. It is probably the only "true" linear amplifier, since it amplifies over the entire input cycle such that the output is an exact scaled replica of the input without clipping. This "true" linearity is obtained at the expense of wasting power. To improve efficiency without sacrificing too much linearity, the concept of "reduced conduction angle" was proposed. The idea is to bias the active devices with low quiescent current and let the input RF signal to turn on active devices for part of the cycle. As the conduction angle shrinks, the amplifier is biased from class AB, to class-B and eventually class-C. Regardless of conduction angle, the active devices are used as current sources. Therefore, they are referred often as "Trans conductance" PAs.

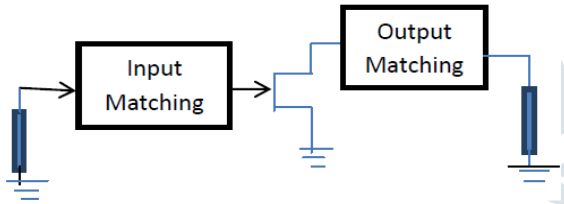


Figure 3 : Basic topology of RF Power Amplifier.

ii.Switch mode PAs

The switch mode power amplifier includes class D, E, F. These types of PAs rely on the operation in triode region for optimal efficiency and output power.Figure 5 shows the basic circuit diagram of class E PA. In these amplifiers, the output device is driven by a large square wave signal. For signals that have mainly phase and frequency modulation, such as QPSK,GMSK, the envelope is constant. The key idea behind the switch-mode PA technology is to operate the transistor in the saturation region depending on amplifier class is switched on and off, waveform shows isolated signals of either voltage or current.

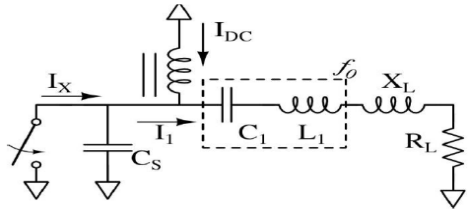


Figure 5:Basic class E Power Amplifier Circuit

When switch is open, only voltage is present over the transistor while when switch is close, only current flows through it. Therefore, there is no any overlapping of current and voltage waveform, so the dissipation of power will be as low as possible. But some of the overlapping portion will give dissipation. The less power dissipation will give better efficiency. Theoretically the 100% efficiency is possible with the design equations[1].

iii.Hybrid Class PAs

The hybrid class of power amplifiers has their advantages and disadvantages respectively of the combination of two different classes. To overcome these limitations and further improvements will be done with several classes like a class BD power amplifier, class EF power amplifier are the particular classes of the interest. To design this PA the use of Class EF will give special attention to get better performance with low voltage supply. This operating class also have the advantage of getting high bandwidth with frequency range is from 1.5 to 3 GHz.

Table 1 compares the performance of the different classes of operations in terms of output power, gain, efficiency, and linearity. It shows that the efficiency of the linear amplifiers decreases from class A to class C. However, the high linearity of the class A PA trends to the high nonlinearity of the class C PA when moving from class A to class C. In the case of switching-mode PAs, class D and E PAs have very high efficiencies, but they are strongly nonlinear. The class F PA also has very high efficiency and is highly nonlinear.

TYPES OF PA	PARAMETERS			
	Output power	Gain	Efficiency	Linearity
ClassA	Very High	Very high	Low	Very high
ClassB	Medium	Medium	High	Medium
ClassC	Low	Low	Very high	Low
Class AB	High	High	Medium	High
ClassD	Medium	Medium	Very high	Low
ClassE	Medium	Medium	Very high	Low
ClassF	High	High	High	Low

Table 1: Performance comparison for different class of operation of PAs

III. CHARACTERISTICS OF RF POWER AMPLIFIER

Radio frequency (RF) power amplifiers are an essential part regarding the base station and also in the communication networking devices energy consumption and power dissipation. There is also the environmental impact of the PA, as the power consumption affects the environmental impact to get a reduction of the radio access network. The main goals for the further improvement in the PA are as follows:

1. High linearity to satisfy higher-order modulation scheme.
2. Greater average output power levels
3. Broader operating bandwidth
4. Low consumption of radio network energy reduces the environmental impact.

The performances matrices like gain, output power, ruggedness, linearity, efficiency, sizes, and noise can be measure different for different type of applications, in these applications most commonly used matrices for measurements are efficiency and the linearity.. The S-Parameter analysis will give the gain, reflection coefficient for input and output side as well as the reverse isolation will give results with graphically as well as theoretically.

i. Efficiency

It is the most important measurable parameter for the power amplifier, will measure how well a device converts one energy source to another [9]. In the power amplifier, the efficiency can be calculated in the form of drain efficiency and the power added efficiency[6]. Equations (1) and (2) show the definition of efficiency in the form of drain efficiency and the power added efficiency.

$$Drain\ efficiency(\eta_D) = Pout/Psupply \ldots\ldots \quad (1)$$

$$Power\ Added\ Efficiency\ (\eta_{PAE}) = (Pout - P_{IN})/P_{SUPPLY} \ldots \quad (2)$$

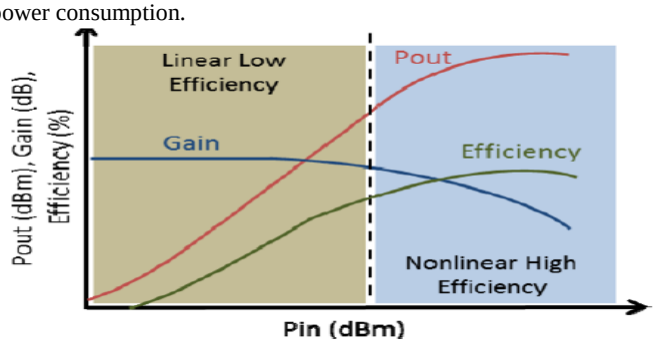
ii. S-Parameters analysis

It is one of the important measurable performance aspects with the measurement of the S-Parameters. To design of the power amplifier, one should have to consider a large signal S-Parameters and to be aware of the nonlinear effects. The S-Parameter includes quantities like S11, S22, S12 and S21, which means that input return loss, output return loss, reverse isolation and the power gain respectively. Graphically one can measure the S-Parameters, which will be easy to measure the circuit performance and also avoid the complexity of equation calculations [8]. The smith chart will also be useful to calculate the matching conditions of source to load impedance to transfer maximum power at the output.

iii.Power consumption/Power control circuitry.

In a typical transmitter, the PA consumes the most amount of power from the supply/battery. For portable devices, it is essential that this parameter must be kept as minimum as possible. This can be achieved with smaller transistors and smaller bias currents.One of the many power saving schemes is the use of power control circuitry. When the mobile system is near a base-station, a decision logic at the output of the PA senses that high output power levels are not required and the control circuitry controls the amount of bias/supply to reduce the power levels. The operation is performed when the base-station is at a distance away from the mobile system. The battery life is thus improved, but at the expense of extra circuitry. Another power saving scheme is the use of power switching, wherein a switch transistor is used to turn off the power supply going into the core amplifier, thus reducing the power consumption.

PARAMETERS	TYPES OF LINEARIZATION TEHNIQUES		
	Feedback	Feedforward	Analog/Digital Predistortion
Frequency Bandwidth	Narrow	Wide	Ultra/Medium
Linearity	Good	Ultra	Medium/Ultra
Complexity	Medium	High	Medium/Medium
Power Efficiency	High	Low	High/High
Adaptation	Intrinsically adaptive	Intrinsically non-adaptive	Intrinsically non-adaptive



IV. LINEARIZATION OF RF PA

The nonlinear behavior of the RF front-end, especiallyRF transmitters, significantly degrade the overall performance of wireless systems. An amplifier operating in this nonlinear range generates IM distortion that interferes with neighboring channels. Therefore, there should be compensation for the nonlinearities and distortions of the RF transmitter. An efficient PA design reduces the cost of power consumption and increases the battery life of wireless mobile transmitters. However, the increase in efficiency is usually accompanied by linearity deterioration, which requires a trade-off between efficiency and linearity [14]. The output power, gain and efficiency variations for a typical PA as functions of the input power are shown in below Figure 4. As can be observed from this figure, there are two major operational regions for the amplifier. In the first region, the amplifier has a linear gain, but the efficiency is low. In the second region, the amplifier has high efficiency, but the gain is nonlinear. Linearity deterioration is caused by the distortions introduced to the signal by the compression of the PA in the saturation region. As a result, the linearity/nonlinearity of the PA depends on the input signal power.

Fig 4:Output power, gain and efficiency versus input power in RF PAs

Linearization is a systematic approach to reduce an amplifier's distortion and is inevitable for enhancing the linearity of an amplifier to the high input power drive levels and achieving linearity requirements when operating the device over its entire power range. Linearization allows a PA to generate more power and operate with higher efficiency for a given level of distortion[6]. There are different methods for linearizing an RF amplifier. The three major linearization techniques are feedback, feedforward, and predistortion [15]. Table 2 given below compares the performance of feedback, feed-forward, and predistortion linearization techniques, in terms of frequency bandwidth, linearity, complexity, power efficiency, and adaptation. Table 2 explains the performance comparison of various linearization methods.

Table 2: Performance Comparison of Different Linearization Methods

V. CMOS TECHNOLOGY

As mass-consumer products require a low manufacturing cost, CMOS technologies have been preferred as semiconductor material, as it has been possible to integrate more and more functionality along with a constant increase of performance. Without the scaling of both transistors and the cost of manufacturing of CMOS transistors, high-technology innovations like portable computers and mobile phones would probably not have been realized[11],[13]. Considering the scaling trend of MOS device we foresee almost a reduction of two of the gate oxide thickness and a reduction of four of the gate length for the thin oxide devices in the next ten years, leading to potentially extreme f_T[10],[12]. Due to the very thin oxide andthe low supply voltages, it is more likely to use the thick oxide (I/O) devices or a combination of both devices in PA design. The expected trend for the thick oxide devices is not as extreme as for the thin oxide devices, as they are expected to have an oxide thickness of 2.6nm in ten years, comparable toexisting thick oxide devices today.

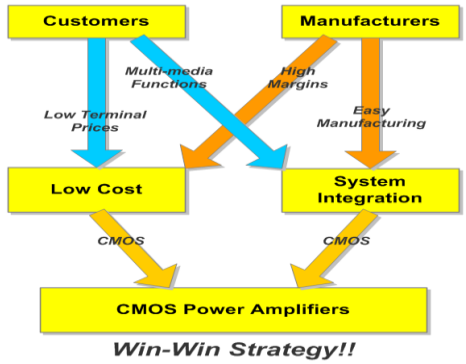


Figure 5: Benefits of CMOS PAs in Cellular Markets

VI. APPLICATIONS OF PA

Each real PA targets a specific wireless application among many wireless systems and standards. The key specificationsdetermining the PA design approach are the RF signal PAR and bandwidth, and the requirements for power control.

i. PAs for AMPS, GSM and GPRS

Advanced mobile phone system(AMPS) uses old-fashioned frequency modulation, whereas GSM and general packet radios service (GPRS) employ Gaussian minimum shift keying (GMSK). Most present 824-849MHz AMPS PAs are designed as dual-mode CDMA/AMPS solutions implemented with gallium arsenide(GaAs), gallium indium phosphide(GaInP) or Gallium Nitride(GaN)transistors. These circuits support CDMA in optimized preferred mode as current PAs and are used for AMPS in legacy mode as switching PAs. The typical GSM/GPRS PAs are quad-band multichip modules(MCMs) containing two circuits, each containing two circuits, each covering adjacent bands: 824-849/880-915MHz and 1710-1785/1850-1910MHz. At nominal 3.4V battery voltage and 25˚C, these amplifiers deliver 35dBm power in the digital cellular communication system(DCS)/personal communication services (PCS)bands with average PAE(over different products) better than 55 and 52%, respectively.

ii. PAs for EDGE

Enhanced data for GSM evolution(EDGE), a GSM upgrade, uses the same 200kHz channelization but introduces 8 phase shift key(8PSK) modulation for a 3X increase in raw data rate. This comes at the expense of 3.2dB signal PAR, which dictates a different approach to the PA design. To meet the spectral mask and EVM requirements, it is customary to use class AB current/linear PAs operated 2.5-3dB compression.Typically, an EDGE with 3.5V supply providing 29dBm power in the U.S Cellular/EGSM bands and 28dBm power in the DCS/PCS bands has only 25%PAE. Because of moderate PAR and narrow signal bandwidth, EDGE is an excellent system candidate for polar PA application.

iii. PAs for CDMA and WCDMA

CDMA and WCDMA use MHz signal bandwidths and a coding scheme generating RF signals with high PAR. The most successful CDMA PA approach to date is class AB with efficiency enhancements, but other techniques are also considered. A common method used in CDMA PAs to mitigate the efficiency problem due to large power control is quiescent operation adaptation. Another method is the power supply adaptation according to the envelope tracking technique. Finally, the CDMA efficiency problem has motivate a serious reconsideration of the classical Doherty and Chireix concepts. Design considerations and board-level implementations of three-stage WCDMA (1920-1980MHz) Doherty amplifiers using 10V GaAs FET can be used. Similarly, a Chireix out-phasing PA WCDMA 2110-2170MHz downlink uses a pair of saturated class B amplifiers implemented with two 0.25µm amplifiers implemented with two 0.25µm p.channel high electron mobility transistors(pHEMTs), which are bare-die bonded on a printed circuit board(PCB).

iv. PAs for IEEE 802.11a/b/g

The typical performance of commercial IEEE 802.11 PAs operates from a 3.3 V power supply. The 6.5-8 dB difference between the 1 dB compression point *p* IdB and the orthogonal frequency division multiplexing (OFDM) signal power *P*OFDM(max) is consistent with the large PAR of 64-QAM OFDM. Despite using identical signaling, the 802.11a PA efficiency is approximately 2X smaller than that of the 802.l1g PA. This is a consequence of operation at much higher frequencies. The 802.11g parts support IEEE 802.11b CCK signaling with *lower* PAR. In CCK mode, the PAs can be operated with less back-off and much improved PAE. Typically, an *802.1* 1*big* PA with 26.5 dBm P_{1dB} delivers approximately 23dBm CCK power with 30% PAE. Table 3 shows how popular wireless systems compare in terms of these specifications.

	PAR (dB)	Signal Bandwidth (MHz)	Power Control (dB)
AMPS,GSM,GPRS,EDGE	Low (≈0,≈0.2)	Smal l(≤0.2)	Moderate (≤30)
CDMA,CDMA 2000,WCDMA	Moderate (3-5)	Large (1.23,3.84)	Very large (70-80)
IEEE 802.11a,IEEE 802.11g	Large (>7)	Very large (≈17)	N/A

Table 3:PAR, Bandwidth, and Power Control Specifications

VII.DESIGN PROCEDURE OF RF PAs

In the design of a PA with given specifications, a systematic approach can be helpful.

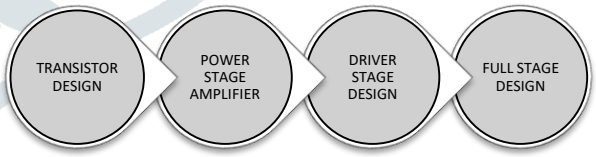


Figure 6 : General Design Procedure of PAs.

The first step of the procedure is to evaluate the transistor in light of the available semiconductor solutions and then to check the transistor characteristics from the perspective of the loadline, the determination of size, and finally the characteristics of a given size. The next step is to design a power stage in which both load-pull and source-pull analyses are repeated until the design optimization for output power, efficiency, and sometimes even linearity are complete. The final step is to evaluate the spectrum performance of the power stage. The same procedure can be applied to the driver stage. By securing the designed power stage and the driver stage, a complete PA that focuses on the output matching, inter-stage matching, and input matching can be designed. Since the performance should be optimized, even though each block is already characterized well, all design parameters should be readdressed from the perspective of the full stage design. Since all specifications are in trade-off relations,

designers are required to spend considerable time optimizing and repeating the same procedure until all the specifications have sufficient margins.

VIII. RELATED WORKS

i. Chaoyi Huang et al., proposed a 80W high gain and broadband Doherty PA for 4/5G Wireless communication systems[16]. In this paper, the 2-carrier 40MHz long-term evolution (LTE) signals were used.Elimination of complex interaction of varying 2nd harmonic impedances caused by active load modulation was carried out. A peak output power of 49.1-49.5dBm was achieved , with a drain efficiency of 50.2%-55.1% at 8dB output back-off. Experimental results showed that adjacent channel leakage ratio(ACLR) was -30dBc at average output power of 3.45GHz. It employed wolfspeed's CGHV27030S GaN HEMT to validate the design method.

ii. Frederick H.Raab introduced a 650W high efficiency amplifier for 704MHz [17]. It employed five GaN-FET class-F RF power amplifiers with a low-loss Gysel splitter and combiner.If one PA fails, the other four continue operating as if nothing had happened.The high isolation of the power combiner allows the failed PA to be swapped while the others are operating. Efficiency is maintained over a wide range of amplitudes through supply modulation(Envelope Elimination Restoration). Efficiency of 79% was achieved for power outputs from 380 to 650 W , and an efficiency of 70% for all outputs above 90W is obtained. The drive power was only 12W.

iii. Branko Bukvic et al., proposed a simple design of a Class-J amplifier with predetermined efficiency [18]. High-gain of 1.5GHz GaN HEMT PA was designed and fabricated.Measured drain efficiency of the PA at 1 and 2 dB compression points are 55.2% and 70% respectively.The maximum drain efficiency is higher than 85% at the saturated output power of 40dBm. Measure d(small signal) S-parameters, output power, gain, and drain efficiency of the PA compare extremely well with full-wave and circuit- based cosimulations.

iv.Xuan Anh Nghiem et al., proposed a 100W GaN HEMT SPA-D with 57% fractional bandwidth for DVB-T applications [19].The high power SPA-D demonstrator exhibits measured drain efficiency of 45%–67.5% at 8 − *10 dB*power back-off (BO) and 54%–79% at peak power of ≥ 100 Wover 460 MHz–830 MHz(∼ *57% FB).* At 710 MHz, ameasured power added efficiency (PAE) of 70 % and 62.5 % areachieved at 50.5 dBm output power and 8 dB BO, respectively.

v.Jessica Chani-Cahuana et. al., introduced a new technique to identify the parameters of a digital predistorter based on iterative learning control (ILC) [20]. A complete derivation of an ILC scheme suitable for the linearization of PA which includes convergence conditions and the derivation of two learning algorithms is presented. The proposed ILC scheme and parameter identification technique are demonstrated experimentally and compared with the indirect learning architecture (ILA) and direct learning architecture (DLA). The experimental results shows that, even for the most difficult cases, the proposed ILC scheme can successfully linearize the PA.

vi.Ritabrata Bhattacharya et al., demonstrated a highly area-efficient , dual-band (2/5 GHz), fully integrated PA designed for WLAN and WiMAX applications using in 180nm technology [21]. By varying a switchable inductor to achieve dual-band operation in the interstage matching network and low-Q on-chip input and output matching networks. The proposed PA, occupies a core area of only 0.9 mm^2 and does not used any off-chip components.A maximum P_{sat} of 17.8/16.3 dBm, a maximum PAE of 26/15% , at 2/5GHz resulted in the post-layout simulation.

vii.Sunbo Shim et al., introduced a CMOS RF programmable-gain driver amplifier (RF PGDA)for wireless transmitters [22]. In order to enhance the dynamic range and to save power consumption, especially at low gain region, digital-step differential attenuators is preceded with programmable-gain amplifier. The RF PGDA fabricated in a 130nm CMOS technology with a 1.2V supply voltage achieved a dynamic range of 49dB with a step error of less than 0.5dB and highly-linearized output satisfying the WCDMA/LTE specifications. The experimental results exhibited a maximum output power of 6.6dBm satisfying 3GPP ACLR specification, power consumption of 18mW at an output power of -42.36dBm for WCDMA and applicable performances for even LTE with a bandwidth of 20MHz.

viii. Kiitchiro Takenaka, et al, [23]proposed the novel broadband Doherty Power amplifier designed for multiband handset applications.This proposed DPA is demonstrated experimentally with InGaP-HBT.A PAE of 45.3% and an E-UTRA ACLR of -36.1 dBc at an average output power of 27.5 dBm are measured.At 800MHz under LTE 10MHz,QPSK, 12 RB operation, and the effiency improvement from Class AB operation achieved 12%. Then proposed DPA maintained more than 41.2% efficiency with an E-UTRA ACLR of below -35.5dBc from 700MHz to 950MHz, corresponding to 30% fractional bandwidth.

ix. Ankur Gupta et al., reported drain-extended MOS device design guidelines for the RF PA applications[24]. A complete RF PA circuit in a 28-nm CMOS technology node with matching and biasing network was used as a test vehicle to validate the RF performance improvement by a systematic device design. By simultaneous improvement of device-circuit performance, 45% improvement in the circuit RF power gain, 25% improvement in the PAE at 1-GHz frequency,0.16W/mm power density and 5x improvement in the electrostatic discharge robustness were reported experimentally.

x. Chaoyi Huang et alpresented theoretical background of a Class-J mode Doherty power amplifier(PA).A GaN DPA is designed and fabricated to validate the method over a frequency band of 3.3-3.7GHz.Under a 10% duty-cycle pulse excitation, experimental results show the DPA delivers 48-48.8 dBm output power with a drain efficiency of 58%-71%.At 8 dB OBO, a measured DE of 44%-55% is achieved with a gain of 11.8-13.5dB.When driven by a 2-carrier 40-MHz long-term evolution signal with a PAPR of 8dB, the DPA exhibits an ACLR of -30dBc at an average power of 40.7dBm at 3.45GHz.

xi. Rocco Giofre et al proposed a design method to minimize the phase distortion (AM/PM) in GaN PAs without worsening efficiency, amplitude distortion and gain [26]. When tested with modulated signals, at 32 dBm of average output power and without any digital predistortion, the DPA shows a spectral regrowth of around 36 dBc and a PAE of 40%, whereas the class AB PA achieves 40 dBc and 30%, respectively.

IX.CONCULSION

This paper explained the characteristics, classifications of RF power amplifiers. The various applications of RF PAs were discussed. The importance of CMOS technology in RF PAs were studied. The performance parameters of RF PAs were tabulated. Related works on CMOS RF PAs carried by various authors also were discussed.

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