16-BIT ADC USING SECTIONAL COUNTER TECHNIQUE

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Abstract: Different ADC techniques are briefly introduced here. The simultaneous converter has least conversion time but becomes unwieldy for more than a few bits of digital conversion. The simple counter method has a very long conversion time (2n clock pulses for n-bit conversion). The continuous converter is very fast once it is locked with the signal but cannot be multiplexed.

Here, we present 16-bit ADC using sectional counter technique. This technique is used for reducing the total conversion time of a simple counter by dividing into sections. Here we use programmable gain amplifier (op-amp IC741) whose gain is selected by digitally controlled analog switching multiplexer IC CD4052.

Using the sectional counter our aim is to reduce conversion time. In simple counter method; pulses required for one conversion are given by 2^n (for 8 bit conversion, 2^8 = 256 and for 16 bit conversion 2^{16} = 65,536 pulses). In sectional counter technique, number of pulses required for one conversion is given by Number of sections * 2^n (for 8 bit conversion of 2 sections of 4 bits each $2*2^4$ = 32 clock pulses and for 16 bit ADC of 4 sections of 4 bits each $4*2^4$ = 64 clock pulses).

***Index Terms* – ADC, Conversion time, Sectional Counter, Bit.**

I. INTRODUCTION

This technique used to convert analog signal into digital signal. We have several techniques to convert analog signal to digital signal i.e. simultaneous conversion technique, Simple Counter Technique, Continuous analog to digital conversion, Successive Approximation Technique and Sectional Counter Technique. In addition there are integration methods.

The simultaneous method of A/D conversion is based on how many comparators are there in the circuit. As the number of bits in digital number increases, the number of comparators increases rapidly (2^n-1), and the problem becomes unmanageable. The simple counter technique is good method for digitizing to a high resolution. This method is simpler than simultaneous method, but the conversion time required is longer than simultaneous method. The average conversion time is 2^{n-1} counts. Continuous A/D conversion is used for speeding up the conversion of signal to eliminate need for resetting the counter each time a conversion is made. If multiplexing is required, the successive approximation convertor is most useful. In this method one conversion cycle requires one cycle of the clock.

A high resolution A/D converter using only one comparator could be constructed if a variable reference voltage were available. The reference voltage could then be applied to the comparator, and when it became equal to the input analog voltage, the conversion would be complete. We use Sectional Counter Technique for reducing total conversion time of a simple counter converter is to divide the counter into sections. An amplifier with a several gain choices is provided in the DAQ (Data Acquisition) Systems to boost low level signal to optimum level. The Programmable gain amplifiers (PGA) enable the selection of the gain through program. Amplifiers built with discrete components are also used in the DAQ systems. Such systems use a register on-board to set the gain of the amplifier.

II. RESEARCH METHODOLOGY

To construct sectional counter, we use five important circuits,

1. Comparator circuit
2. Sample and Hold circuit
3. 4-bit DAC circuit using R-2R ladder
4. 4-bit DAC simple counter
5. Variable gain amplifier

- Function of Comparator:

The Comparator has two input terminals and one output terminal. The two input terminals are Analog Input Voltage terminal V_a and Reference Voltage Input terminal V_{ref} The Digital output terminal is V_0. Comparator compares the two input voltages and produces Digital output of 0 or 1.
First assume that V_a is less than the reference voltage ($V_a<V_{ref}$), As the non inverting input of comparator is less than the inverting input, output will be low $V_0 = 0$ and at negative supply voltage, $-V_{cc}$ resulting in a negative saturation of the output. If we now increase the input voltage V_a, so that its value is greater than the reference voltage V_{ref} on inverting input ($V_a>V_{ref}$), the output voltage rapidly switches high ($V_0 = 1$) towards the positive supply voltage, $+V_{cc}$ resulting in a positive saturation of output. Basically op-amp comparator produces a positive or negative voltage output by comparing its input voltage against reference voltage.

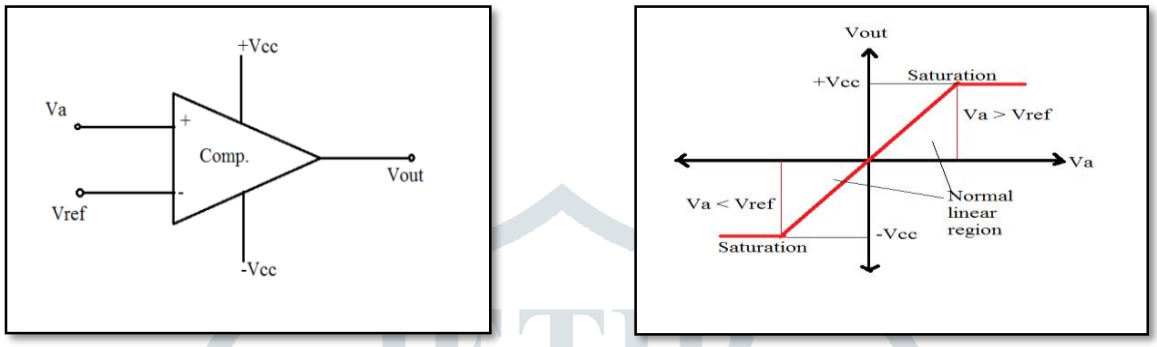

Fig.1: Comparator

- Function of Sample and Hold circuit:

A sample and hold circuit is used to sample an input signal and holds on to its last sampled value until the input is sampled again. Circuit is shown in Fig.2(a)**.** The n-channel E-MOSFET works as a switch in this circuit. Input analog voltage is applied to the drain of E-MOSFET and control voltage is applied to the gate. Capacitor is used to store the charge. When V_c is positive, E-MOSFET turns ON so capacitor C charges. Input voltage appears across capacitor and output will appear at voltage follower A_2**.** Output waveform of the circuit is shown in Fig: 2(b) **[5]**. When V_c is low the E-MOSFET is off. The capacitor cannot discharge due to high input impedance, it holds the voltage. T_s is sampling time and T_h is hold period.

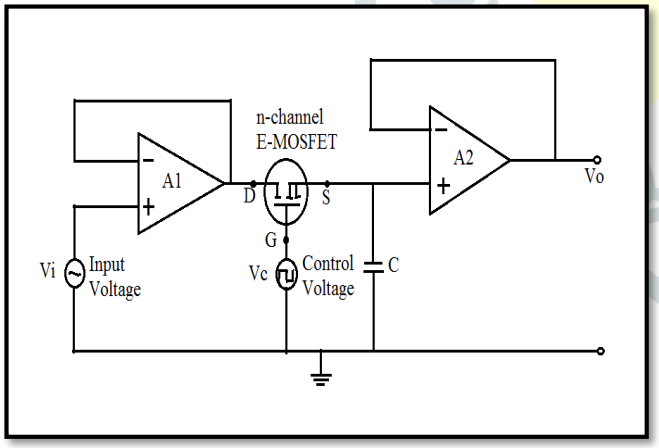

Fig. 2(a)

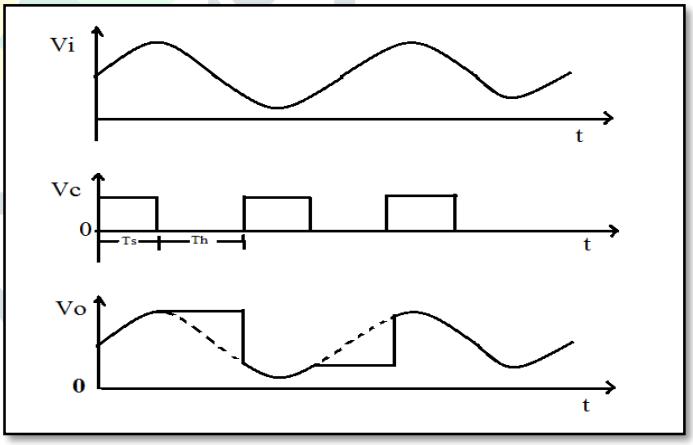

Fig.2(b)

Fig.2: (a) Sample and Hold Circuit (b) Input/ Output Waveform of the circuit

- Operation of simple counter ADC using DAC in the feedback path:

The output of S/H circuit is applied at the Analog Voltage Input terminal V_a of a Comparator. The other input terminal V_{ref} is applied the analog output of the DAC using R-2R binary ladder connected in feedback path as shown in Fig.3(b). The operation of the simple binary counter is as follows, first the counter is reset to all 0s. When Converted signal appears on the START line, the gate opens and clock pulses are allowed to pass through it to the input of the counter. Now output of this counter is connected to a standard Binary ladder (R-2R network) to form a simple DAC converter as shown in Fig.3. We get the familiar staircase waveform at the output of DAC. This waveform is applied at the reference input terminal V_{ref} of the comparator. Another input terminal of Comparator V_a is applied output of S/H circuit. When these both voltages are equal then the gate is closed. The counter will stop and conversion is complete. The digital number stored in the counter is the desired converted digital output.

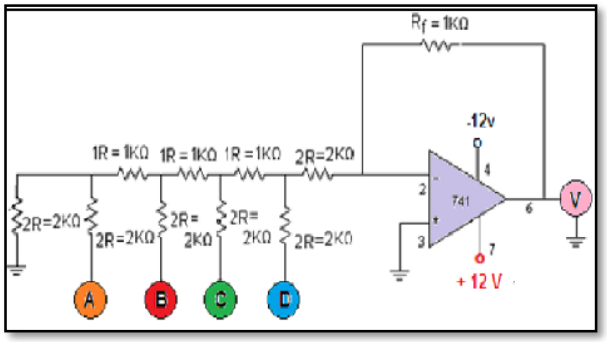

Fig. 3(a)

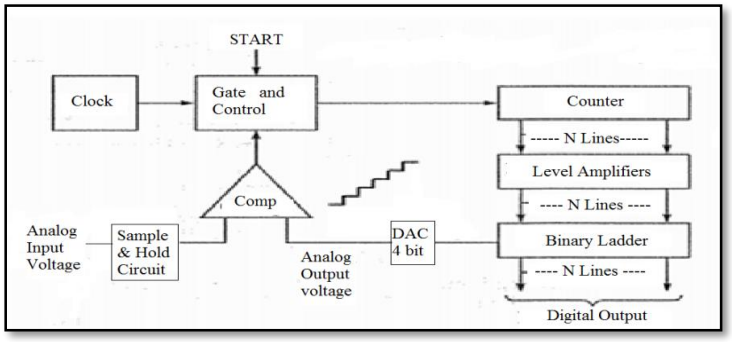

Fig. 3(b)

Fig.3: (a) 4 bit DAC using R-2R ladder**[4]** (b) 4 bit DAC simple counter, one comparator and 4 bit DAC in feedback path

- Operation of 16 bit ADC using Sectional counter technique:

Here we have designed 16 bit ADC using 4 sections of 4 bits each. The block diagram is given in Fig 4. A variable gain amplifier block is inserted between DAC output and V_{ref} input to the comparator. A two-pole four-way switch using digitally controlled 8 channel analog switching IC CD 4052, a IC 555 Astable Clock and a Counter using IC 4029 is fabricated and this circuit is used to switch the 4 sections and produce the 16 bit digital converted output.
This switching of gains of amplifier and switching of sections and output bits is done by a two - pole four - way switch as shown in the block diagram fig. 4.

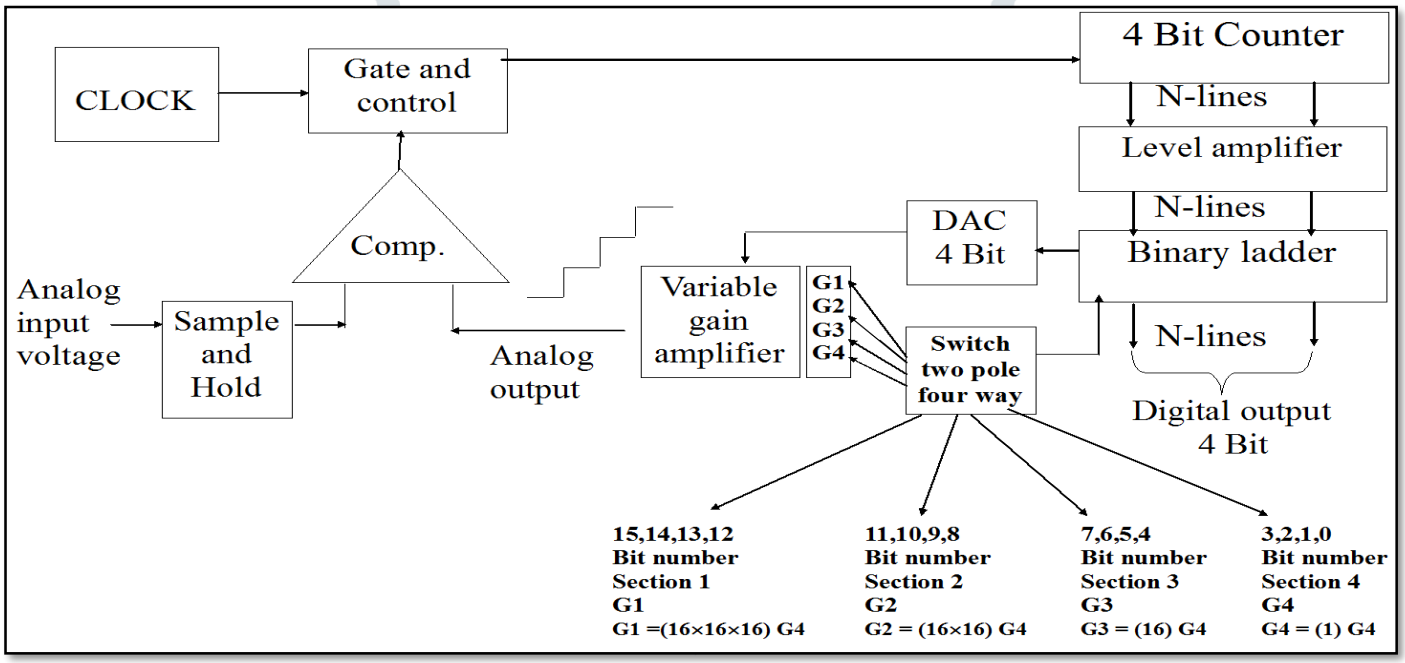

Fig.4: Block diagram of 16 bit sectional counter with 4 sections of 4 bit each.

III. RESULTS AND DISCUSSION

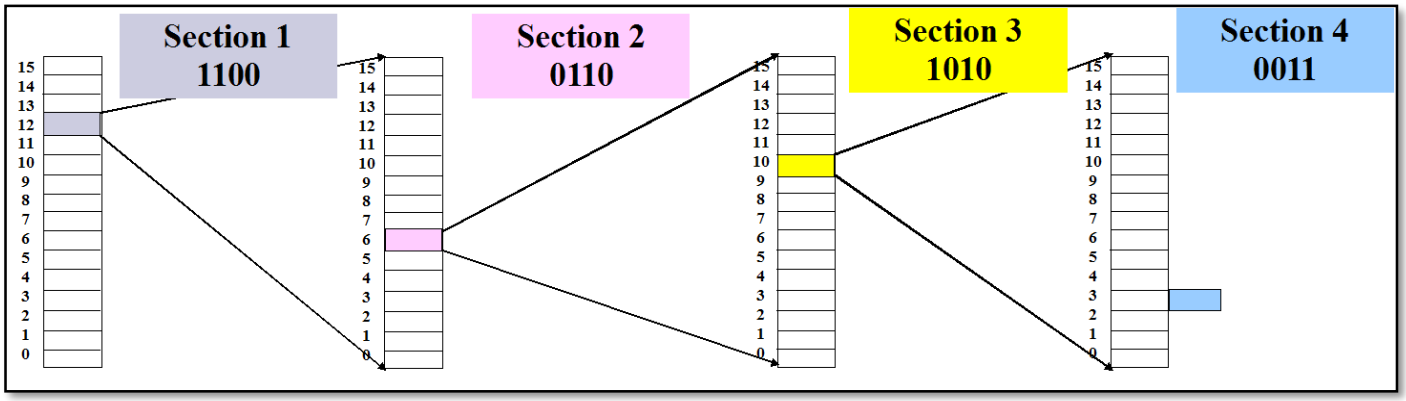

Fig.5: Sample output 16 bits are 1100,0110,1010,0011.

When the analog input is applied to the converter, first the highest value bits 15, 14, 13 and 12 are to be produced by section 1. For this purpose the gain of the variable gain amplifier is kept at highest value of G1 = (16 *16 * 16) * G4. The whole analog input voltage range is divided into equal 16 regions and the step height is largest and also resolution is lowest. When the signal is applied to ADC the 4 bit counter produces the highest 4 bits corresponding to the input value.

In the second stage the next lower 4 bits 11, 10, 9 and 8 are to be produced by the second section. Now the gain of the variable gain amplifier is at value of G2 = (16 * 16) * G4. The step height is now reduced by 16 and correspondingly the resolution is improved by 16 times.

In the third stage the next lower 4 bits 7, 6, 5 and 4 are to be produced by the third section. Now the gain of the variable gain amplifier is kept at value of G3 = (16) * G4. The step height is now reduced by 16 once more and correspondingly the resolution is improved by 16 times.

In the fourth last stage the next lower 4 bits 3, 2, 1 and 0 are to be produced by the fourth section. Now gain of variable gain amplifier is kept at value of G4 = 1 * G4. The step height is now reduced by 16 once more and correspondingly the resolution is improved by 16 times.

Figure sand Tables

IV. ACKNOWLEDGMENT

The Physics Department Gujarat University has received grants under DST-FIST and DRS-SAP Programs. The Funding agencies are gratefully acknowledged. Authors are also thankful to Prof. P.N.Gajjar, Head of Physics Department for providing necessary facilities. Authors thank all the teaching and non-teaching staff of physics department for their encouragement and help. The author is grateful to Prof. P.D.Lele research supervisor for his constant encouragement.
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