A Review Paper on Comparison ofConventional Null Convention Logic (NCL) Structure with Modified NCL Structures

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Abstract: For the last three decades, the focus of digital design has been primarily on synchronous, clocked architectures. However,as clock rates have significantly increased while feature size has decreased, clock skew has become a major problem.High performance chips must dedicate increasingly larger portions of their area for clock drivers to achieve acceptable skew, causing these chips to dissipate increasingly higher power,especially at the clock edge,when switching is most prevalent.One possible solution to this problem is use of Null Convention Logic(NCL).In this paper,this NCL structure will be compared with the modified NCL structures that are proposed for improvement in parameters like area, speed , delay,energy etc.

keyword **-Differential Cascode voltage switch logic NCL, Static holding free NCL, Gate mapping NCL, Low voltage NCL, Static Differential NCL, High speed NCL, Register less NCL, Hybrid Gate diffusion input NCL.**

I. INTRODUCTION

NULL CONVENTIONAL LOGIC is a new technique developed for designing asynchronous circuits.[1] NULL mean there is NODATA or spacer between corresponding DATA. It indicates no input or output is present. NCL logic design is implemented using threshold gates with hysteresis. These gates have many inputs and one output. Output from this gate is DATA when numbers of inputs reach or exceed the threshold. The hysteresis behaviour is achieved by keeping the output is same state as previous till all the input goes to NO DATA.

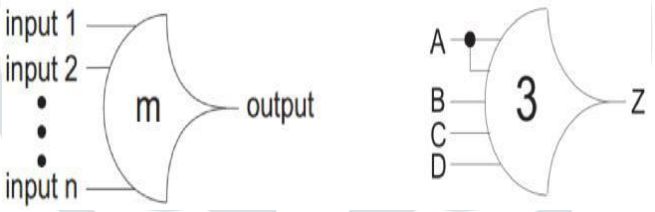

Fig. 1 Symbol for NCL

In fig. 1'n' represents number of inputs to the gate and m represents number of inputs that must be selected so that the output is selected or asserted.

II. VARIOUS NCL MODIFIED STRUCTURE

A. DCVSL NCL Implementation

DCVSL technique was originally developed for CMOS SET RESET technology.[1] It seeks the benefits of rationed circuits without the static power consumption. It consists of a differential N-channel MOSFET logic tree connected to a load which is usually a pair of cross-coupled P-channel MOSFETs. It uses both true and complementary input signals and computes both true and complementary outputs using a pair of NMOS Pull downNetworks (PDN). The pull down network within implements the logic function in a static CMOS gate, while the pull down network within uses inverted inputs feeding transistors arranged in the conduction complement. For any given input pattern, one of the pull down network is ON and the other is OFF. The pull down network that is ON will pull that output low[1]. This low output turns ON the PMOS transistor to pull the opposite output high. When the opposite output rises, the other PMOS transistor turns OFF so no static power dissipation occurs.

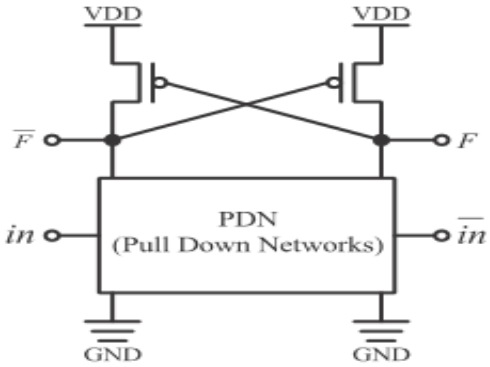

FIG. 2 DCVSL gate architecture

The proposed our NCL gate design is shown in Fig.2. It is similar to Differential Cascode Voltage-Switched Logic (DCVSL). Our proposed NCL circuit can implement complex functions with a single differential tree network, which reduces the number of stages required and lowers the propagation delay compared with the conventional static and semi static based NCL design. Another feature of the proposed Fig. 2: is that whenever the gate switches, the falling rail always switching first, therefore, our design guarantees that input switching will never cause one rail to become asserted without first fully deserting the other rail.

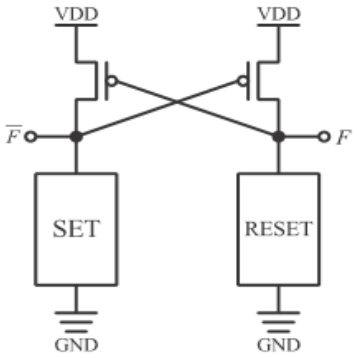

FIG.3 Proposed DCVSL based NCL implementation

B. State holding free Null Convention Logic

The aim of the proposed modification is to remove the combinational state-holding capability[2]. By doing so the input-completeness with regard to NULL front is violated. Let us consider a dual rail non optimized function designed such as all minterms are evaluated. Using conventional AND gates instead of TH22 gates could lead to unexpected outputs. For example, for a 1-bit XOR circuit with two inputs A and B, and one output S, an input set (A, B) equal to (DATA0, DATA0) leads to S equal to DATA0. When S has been acknowledged, the input register is authorized to provide a NULL front. Assuming that for any reason A becomes NULL and B remains DATA0, using AND gates will lead to an unexpected NULL value of S. Therefore removing state-holding capability violates the input-completeness rule as described in Rule 1, with regard to NULL front. However, to ensure data integrity, what is important to guarantee is not to prevent the combinational output to become NULL, but for the next stage to believe that it is receiving a new NULL front. In other words, it is enough to avoid the output register to be cleared. Thus Rule 1 is modified such as input-completeness with regard to DATA front remains the same, but with regard to NULL front, it is changed for verification at the output of the output register.We call this capability as Output State Holding Capability.

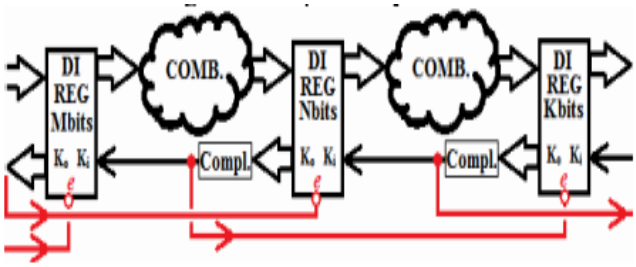

FIG. 4 Proposed state holding free NCL

C. New CMOS Technology for low voltage NCL gate design

This work proposes the alternative NCL topology displayed in Figure 5[3]. In it, output Q switches to 1 or 0, according to the set and reset transistors P0 and N0, respectively. Dimensioning of these follows a process similar to that of the output inverter for the topologies previously mentioned. The same RESET and SET networks control these transistors. However, latter are

respectively connected to their complements HOLD1 and HOLD0 networks. Accordingly, the P0 and N0 driving transistors are both turned off by a hold state input combination. This state uses transistors P1 to P3 and N1 to N3 to maintain the output stable. All these are minimum sized and the mechanism employs a loop of two inverters (P1-N1 and P3-N3), where the driving inverter (P3-N3) is controlled by HOLD1/RESET or by HOLD0/SET (through P2 and N2). Note that HOLD0 and HOLD1 transistors are also minimum size and transistors used for SET and RESET are dimensioned for driving P0 and N0 input capacitance loads. Also, since C-elements rely are special NCL gates the new scheme is also a new topology for C-elements.

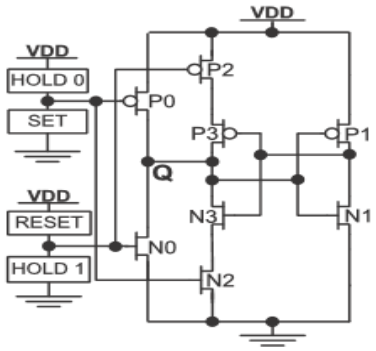

FIG.5 Proposed structure for low voltage NCL

D. Static Differential NCL gate:

1) Differential NCL:

Two recent works discuss DNCL. The first, a seminal work introduces the concept and demonstrates its benefits compared with conventional NCL. Accordingly, DNCL is superior in area and propagationdelay. Moreover, it provides better design space explorationfor large fan-in gates[4]. They propose the generic structure in Fig. 6as a gate template. The pull-down network namedSET provides the gate threshold functionality, which can setthe input of transistor P1 to "0," switching Q to "1." Wheninputs are all "0," the pull-down network labelled RESET putsQ to "0." The complement of the inputs controls the box thatdirectly drives Q. The cross-coupled pair of inverters (P0/N0and P1/N1) keeps the previous value in the output, whenever either SET nor does RESET drive the output. Note that SET and RESET must implement logic functions with disjoint ON-sets and that, in general, these functions are not complementary.

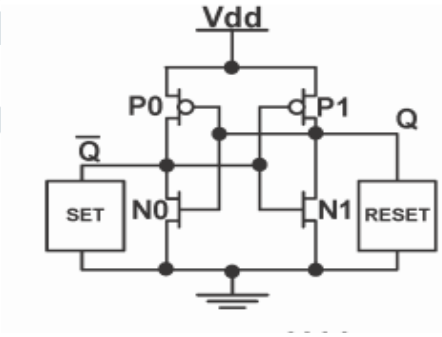

FIG. 6 Generic DNCL topology

2) Static Differential NCL:

Analyzing the DNCL gate topology in fig 7, onecan note that either P0 or P1 will be part of a low-resistance.In Fig. 7, we propose the addition of two pull-up networks formed by minimum-sized transistors (the boxes labeled COS and COR), to alleviate the opposition to change imposed by transistors P0 and P1.[4]The above figshows the implementation of a 2-of-3 gate using this new topology. COR comprises of a transistor arrangement that helps sending Q to "0." This arrangement is the same present in the RESET box, but p-type metal–oxide–semiconductor (PMOS) transistorsreplace-type metal–oxide–semiconductor, and uncomplemented input signals substitute the complemented input signals. Thus, when all inputs switch to "0", transistors C5 − C6 − C7deactivate transistor P1. COS uses the same transistor arrangement of the SET box but controlled by the input complements. The effect is similar to that of COR, but helps sending Q to "1." The mechanism is similar to that of classic static implementation of transition (EPT) NCL gates. Hence, we call the proposed topology static DNCL. forms Because this turns off feedback inverters while switching, SET and RESET blocks can employ smaller transistors, which to reductions on these blocks'

leakage. Even if the extra transistors cause moderate area overhead, power and propagation delay reduce, as the required energy to switch decreases.

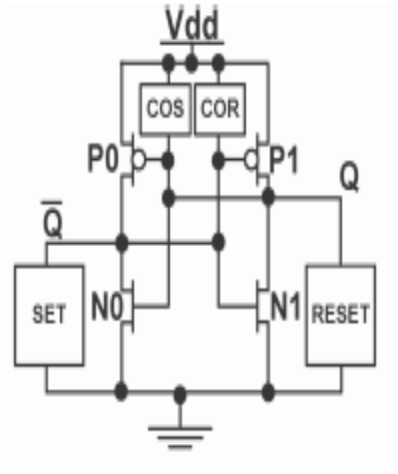

FIG. 7 Genericstatic DNCL topology

E. High speed NCL gate:

In this type, a new CMOS topology has been proposed for implementing gates required by NCL design at the standard-cell level as shown in Fig. 8. The proposed TH23 topology is revised from the semi-static NCL gate.[5] The semi-static NCL gate is the best transistor-level topology compared to other topology only if area overhead and wire complexity are considered. However, the main problem of the semi-static topology is the slow logic speed due to the weak inverter feedback and the number of PMOS serial stacks. The proposed topology doesn't have any PMOS stack like the differential one, while a pseudo-NMOS logic block for a reset function is added, and a feedback memory is formed by a inverter and a NOR gate. The pseudo-NMOS logic has the advantage of speed at the cost ofstatic power dissipation .However the power can be saved enough to use the pseudo-type logic in a real system ifenable signal (EN) is properly controlled. In Fig.8, MP3 isturned off by EN signal generated by the NCL completiontuned off by EN signal generated by the NCL completionasserted to the NCL completion block. That is, EN is changedfrom logic '0' to '1' right before NULL signals are asserted tothe NCL circuits. The feedback inverter is needed to hold output logic value, and the NAND gate is deployed to compensate for speed reduction due to the weak inverter feedback: the output switching time is reduced compared to the semi-static one because the output of the NAND gate is determined by Reset and Set block at the same time.

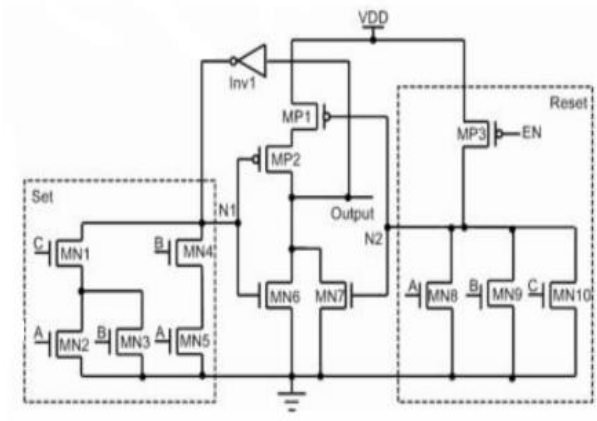

FIG. 8 Proposed TH23 gate

F. Register less gate:

The proposed RL-NCL requires no pipeline registers and is able to support fine-grained power gating. Fig. 9), shows the structure of the RL-NCL pipeline.

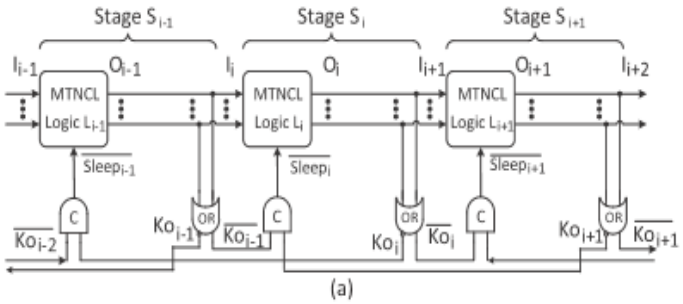

FIG 9 RL-NCL Pipeline

RL-NCL differs from normal NCL as follows.[6]

1) RL-NCL requires no pipeline registers.

2) In the RL-NCL pipeline, *Koi*+1, instead of *Koi* (as in the case of FPG-NCL), is used as one input of the C-element generating signal.

3)In RL-NCL, it is not viable for an input bit of the Logic block to be directly wired to an output bit without MTCMOS threshold gates placed between them, because pure wires themselves cannot operate in the sleep mode. If a logic block does contain pure wires in its input–output network, every pure wire must be replaced with an MTNCL buffer [see signals *Z*10 and *Z*11 of logic block *Li* in Fig. 4(b)], which is a 2-input OR gate (i.e., MTCMOS threshold gate TH12) with the two inputs tied together.

4) In the RL-NCL pipeline, all MTCMOS threshold gates of a logic block begin evaluation/nullification at the same time; thus, the output bit on the critical path of the logic block becomes DATA/NULL after all the other output bits have already become DATA/NULL. Therefore, RL-NCL can employ an OR gate, whose two inputs are connected to the pair of wires associated with the output bit on the critical path of the logic block , to replace the completion detector for detecting whether the output of a logic block is DATA or NULL.

G. Hybrid gated diffusion input NCL

Gate Diffusion Input (GDI) is a promising alternative to CMOS technology for considerable area/power reduction.[7] GDI basic cell design is depicted in Fig 10). It is a four- terminal device consisting of:

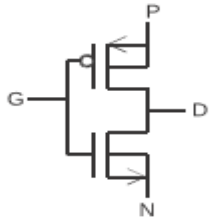

FIG. 10 Basic GDI Structure

1) G: common gate input for NMOS and PMOS transistors; 2) P and N: PMOS and NMOS transistors outer diffusion node; 3) D: common drain for both the transistors. Bulks of the PMOS and NMOS are connected to P or N respectively. Depending on the design requirement P, N and D can be either used as input or output ports.

Different multiple-input gates can also be realized by combining several GDI basic cells. GDI technology can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies but only few functions can be implemented in standard p-well CMOS process. In this paper, a hybrid GDI-NCL ripple carry adder (RCA) is designed based on OR, AND, NOT and MUX GDI functions.

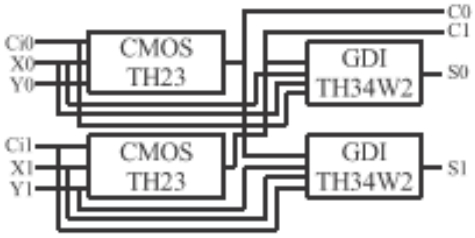

FIG. 11 Hybrid NCL Full Adder

III. Comparison and Discussion

Comparison of Modified NCL structures with normal NCL based on review of research papers is given in below table.

MODIFIED STRUCTURE	POWER	AREA	SPPED AND DELAY	ENERGY SAVING	STABILTY AT LOW SUPPLY VOLTAGE
DCVSL NCL	20%	I	30%	I	I
STATIC HOLDING FREE NCL	S	50%	S	I	NA
LOW VOLTAGE NCL	D	I	I	I	I
STATIC DIFFERE-NTIAL NCL	67%	S	8.9%	67.2%	NA
HIGH SPEED NCL	D	I	I	NA	NA
REGISTER-LESS NCL	72%	49%	NA	NA	NA
HYBRID GDI NCL	27%	11%	NA	NA	NA

TABLE 1 Comparison of Modified NCL structures with normal NCL

I=IMPROVED
NA=NOT APPLICABLE
S=SAME AS NORMAL NCL
D=DEGRADATION FROM NORMAL NCL

IV. Conclusion

This Paper presents comparison of Normal NCL with modified NCL Structures in terms of performance parameters like area, speed, power etc. From the results we conclude that DCVSL NCL structure gives best performance parameters as compared to normal NCL.

V. Acknowledgment

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