Design of Low power CMOS Borrow-Save Adders and 4 bit array multiplier

CH.Sharanya, M.Praveen kumar2, Dr.D.Lakshmaih3, , B. Sanjay Raj4, A.Sharan reddy5
Assistant professor[2] , professor[3], IV ECE students ,ECE Dept.
Vignana Bharathi Institute of Technology, Ghatkesar (Mdl.), Hyderabad, Telangana State, INDIA

Abstract*—In this paper we introduced 10T cmos Full Adder, including the most motivating of those are designed and comparison of area, power and delay. The simulations are approved using 60nm and 90nm technology. Furthermore, design of Borrow Save Adder is introduced to increase the performance better than ripple carry adder. In Microprocessor chip Multiplier is most significant arithmetic design in power dissipation is main parameter. Reducing the power dissipation of multipliers is a key to satisfy the overall power budget of various digital circuits and systems. In this multiplier are CMOS full adder are main building module The main purpose of our work is to calculate the average power, delay and PDP of multiplier. The multiplier architecture will be designed using the 10 transistor Full Adder and the simulation results are compared to existing work our modified proposed multiplier are better performance.

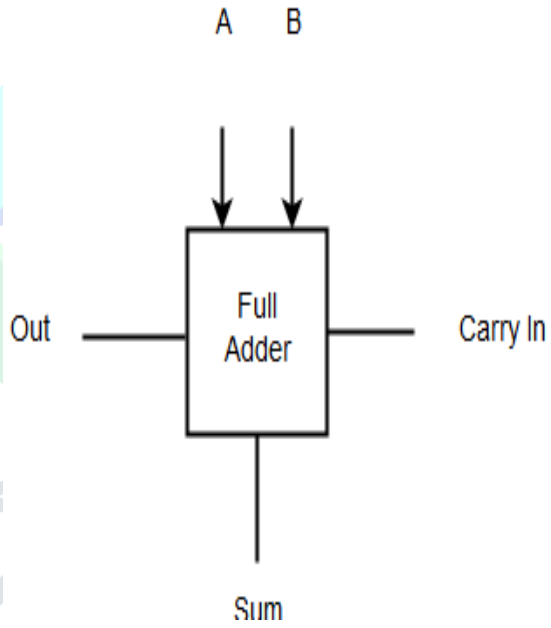
Index Terms-Borrow save Adder, Full Adder, Array Multiplier

I. INTRODUCTION

While the growth of the electronics market has driven the VLSI industry towards very high integration density and system on chip designs and beyond few GHz operating frequencies, power consumption is increases very difficulties sin chip so we need reduce the power consumption.[1] Moreover, with the explosive growth the demand and popularity of portable electronics is driving designers to strive for smaller silicon area, less delay, battery life time is increases, and more consistency[2-4]. Power is the one of the main resource in design system chip. The most important plan of proposed work is to reduce the power dissipation, delay and increase the performance of the 10 transistor Full Adder and design a BSA & 4 bit array multiplier. Full Adder is which adds three inputs and produces two output are sum and carry[5-6] . The first two inputs are A and B and the third input is an input as Cin. The output carry is chosen as Cout and the normal output is designated as S which is SUM.

In this project, we are decreasing the count of the transistor from 28T count to 10T in Full Adder. In the existing work , they designed a BSA and 4 bit array multiplier by using Full Adders having 28 transistors. In the proposed project, we are designing a BSA & 4 bit array multiplier using Full Adder with 10 transistors.

Fig.1 Full Adder



Tabl1.1 Full Adder Truth Table**:**

Input			Output	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logical Expression for SUM:
= A'B'Cin + A'BCin+ABCin+ ABCin
= Cin(A' B' + A B) + Cin'(A' B + A B')
= Cin XOR (A XOR B)
= (1,2,4,7)

Logical Expression for Cout:
= A' B Cin+ A B' Cin+ A B Cin' + A B Cin
= A B + B Cin+ A Cin
= (3,5,6,7)

Another form in which Cout can be implemented:
= A B + A Cin+ B Cin(A + A')
= A B Cin+ A B + A Cin+ A' B Cin
= A B (1 +Cin) + A Cin+ A' B Cin
= A B + A Cin+ A' B Cin
= A B + A Cin(B + B') + A' B Cin
= A B Cin+ A B + A B' Cin+ A' B Cin
= A B (Cin+ 1) + A B' Cin+ A' B Cin
= A B + A B' Cin+ A' B Cin
= AB + Cin(A' B + A B')

Therefore Cout = AB + Cin(A EX – OR B)

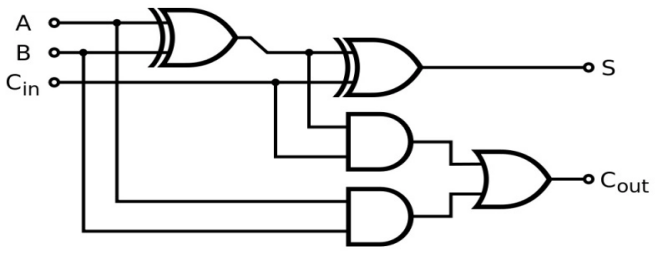
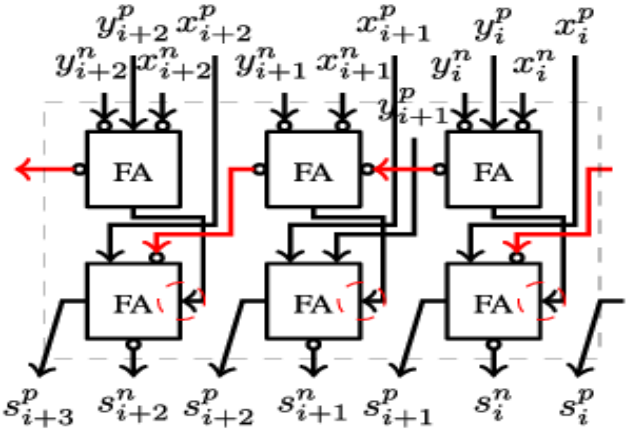


Fig.2. Borrow Save Adder(BSA)



BSA consists of 4-to-2 compressors, composed of two FAs, implementing the carry-free addition algorithm . The addition of operands, already expressed in BS encoding, resembles the addition of operands expressed in carry-save encoding, with the exception of certain inversions in the beginning and at the end of the processing .BSA architecture demonstrates the advantage of reduced ripple-effect over RCA architecture.

3. Array Architecture

Array architecture based MAC uses short wires that go from one Full Adder to adjacent Full Adders horizontally, upright or obliquely. In CMOS array architecture based n x n bit multiplier uses array of AND gates can compute all the ai .bj terms simultaneously. The terms are summed by an array of n [n - 2] Full Adders and n half adders..The advantage of array architecture is its regular structure. Thus it is easy to layout and has small size. The size of array architecture based multiplier increases in size at a rate equal to square of the multiplier operand size.

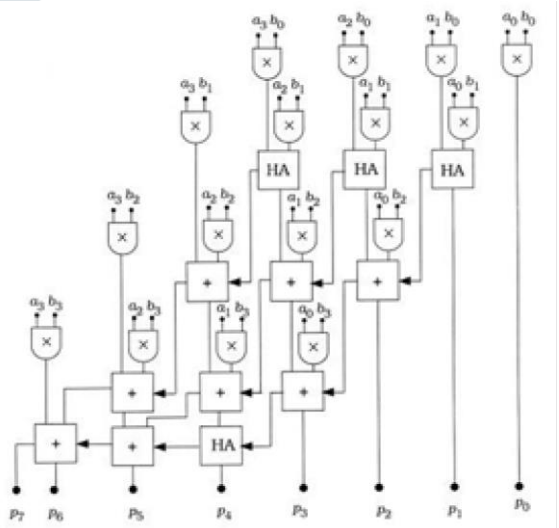


Fig.3 Array multiplier

II. PROPOSED WORK

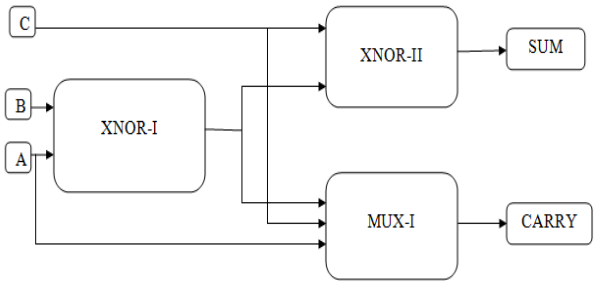


Fig.4 Block diagram of proposed 10T- Full Adder

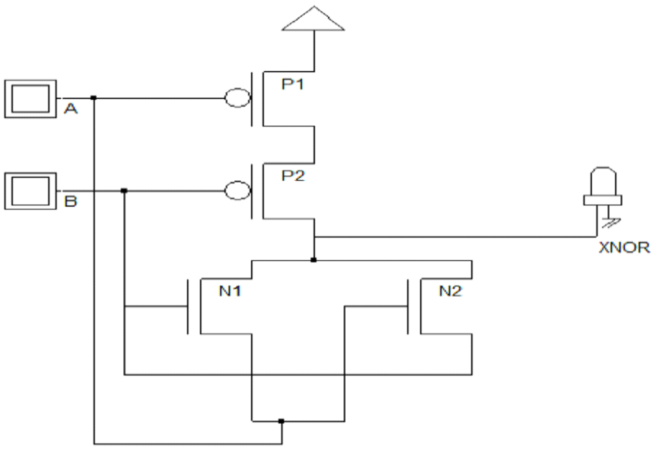


Fig.5 10T- Full Adder circuit of XNOR MOS circuits

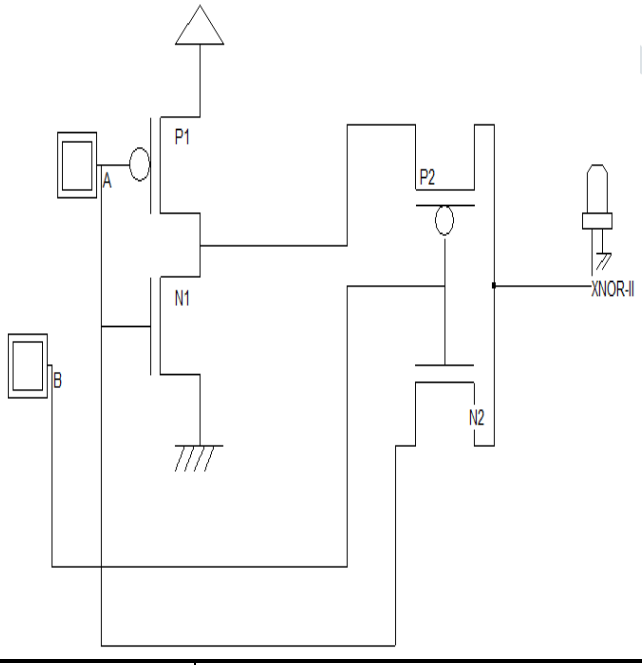


Fig.6 Proposed 10T- Full Adder circuit of XNOR –II MOS circuits

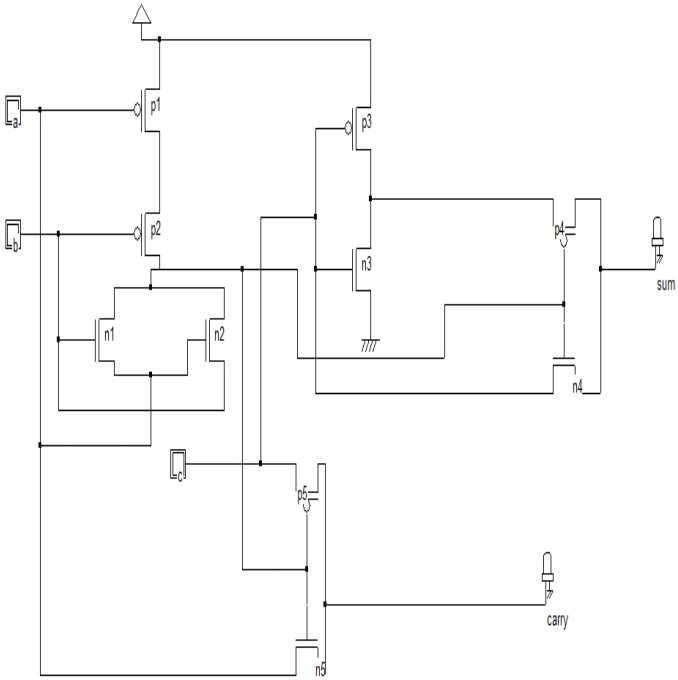


Fig.7 Proposed 10T- Total Full Adder circuit

Verilog | Hierarchy | Netlist | Critical path

Path n°	Symbol	Pin	Node	Delay (ns)
1	light1(8)	carry(1)	7	0.720
2	pmos(3)	d(3)	7	0.720
3	pmos(3)	g(2)	5	0.550
4	pmos(2)	d(3)	5	0.550
5	pmos(2)	s(1)	3	0.100
6	pmos(1)	d(3)	3	0.100
7	nmos(5)	d(3)	5	0.450
8	nmos(6)	d(3)	5	0.450
9	nmos(7)	d(3)	7	0.720
10	nmos(7)	g(2)	5	0.550
11	pmos(2)	d(3)	5	0.550
12	pmos(2)	s(1)	3	0.100
13	pmos(1)	d(3)	3	0.100
14	nmos(5)	d(3)	5	0.450
15	nmos(6)	d(3)	5	0.450
16				

Fig.8Delay report of 10T- Total Full Adder model circuits

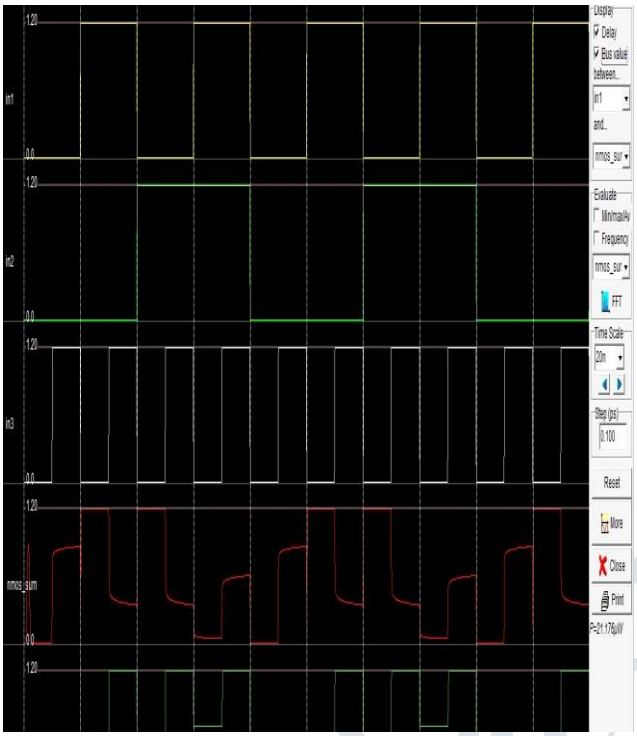


Fig.9Simulation of 10T- Total Full Adder model circuits

Borrow Save Adder

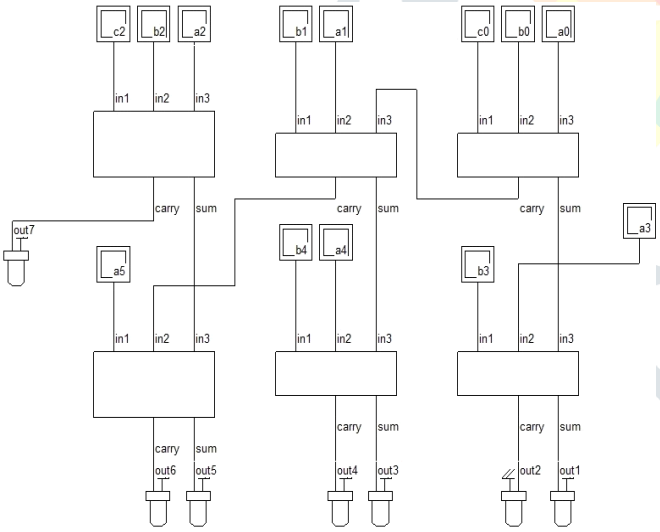


Fig.10 Borrow Save Adder using 10-T Full Adder

Verilog | Hierarchy | Netlist | Critical path

Path n°	Symbol	Pin	Node	Delay (ns)
1	light5(22)	out5(1)	24	2.435
2	10tcmosnew(26)	sum(5)	24	2.435
3	10tcmosnew(26)	in2(3)	20	1.565
4	10tcmosnew(6)	carry(4)	20	1.130
5	10tcmosnew(6)	in3(1)	17	1.200
6	10tcmosnew(7)	carry(4)	17	1.200
7	pmos_1043(69)	carry(3)	17	1.200
8	pmos_1043(69)	w4(2)	40	0.765
9	pmos_1042(68)	w4(3)	40	0.765
10	pmos_1042(68)	w2(1)	39	0.120
11	pmos_1041(67)	w2(3)	39	0.120
12	nmos_1044(70)	w4(3)	40	0.645
13	nmos_1045(71)	w4(3)	40	0.645
14	nmos_1046(72)	carry(3)	17	1.200
15	nmos_1046(72)	w4(2)	40	0.765
16	pmos_1042(68)	w4(3)	40	0.765
17	pmos_1042(68)	w2(1)	39	0.120
18	pmos_1041(67)	w2(3)	39	0.120
19	nmos_1044(70)	w4(3)	40	0.645
20	nmos_1045(71)	w4(3)	40	0.645
21	pmos_1033(59)	carry(3)	20	1.565
22	pmos_1033(59)	in3(1)	17	1.200
23	10tcmosnew(7)	carry(4)	17	1.200
24	pmos_1043(69)	carry(3)	17	1.200
25	pmos_1043(69)	w4(2)	40	0.765
26	pmos_1042(68)	w4(3)	40	0.765

Fig.11.Delay report of Borrow Save Adder using 10-T Full Adder

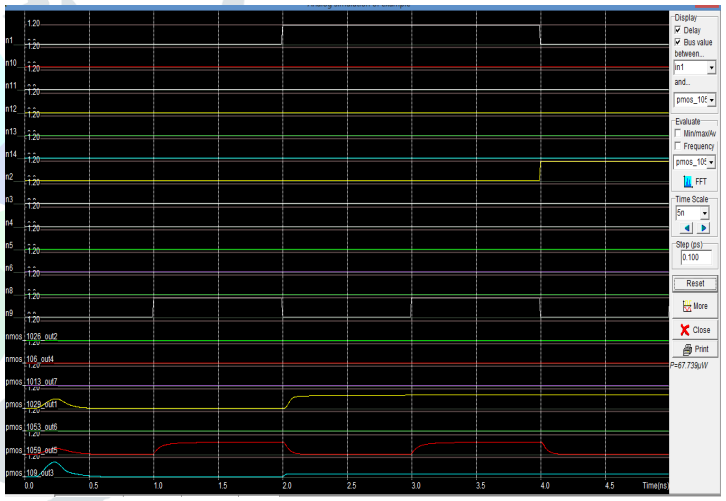


Fig.12.Simulation of Bsa using 10-T Full Adder

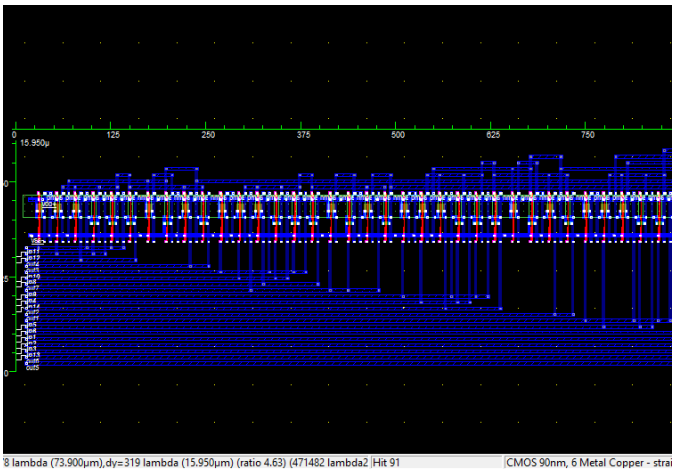


Fig.13 Layout of Bsa using 10-T Full Adder

	EXISTING	PROPOSED
DELAY	6.475 ns	2.425ns
POWER	217(µW)	67.739(µW)
AREA	105×67(µm×µm)	73X15(µm×µm)

T6able.2 Comparison table for Borrow save adder

4 bit array multiplier

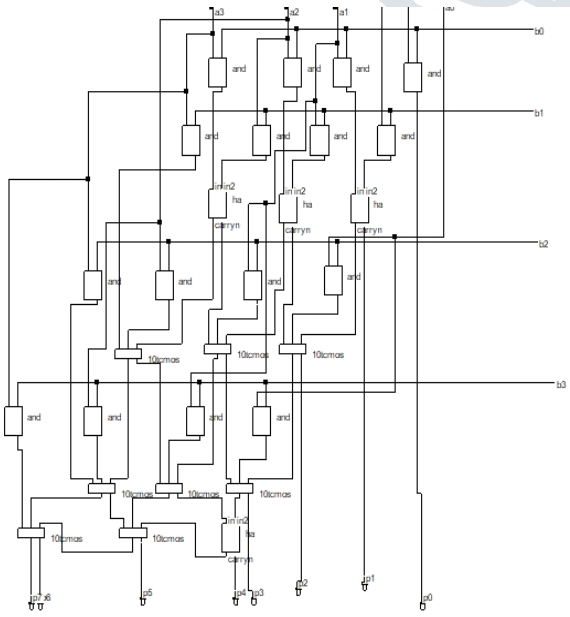


Fig.14 4- bit Array Multiplier Architecture

Verilog | Hierarchy | Netlist | Critical path

Path n°	Symbol	Pin	Node	Delay (ns)
1	light14(43)	p6(1)	45	5.720
2	10tcmos(20)	out2(5)	45	5.600
3	10tcmos(20)	in3(3)	32	5.270
4	10tcmos(16)	out1(4)	32	4.490
5	10tcmos(16)	in3(3)	13	4.835
6	ha(3)	carry(4)	13	5.315
7	ha(3)	in2(2)	11	4.350
8	10tcmos(17)	out1(4)	11	4.350
9	10tcmos(17)	in1(1)	34	2.835
10	10tcmos(19)	out2(5)	34	2.835
11	10tcmos(19)	in1(1)	8	1.425
12	ha(2)	sum(3)	8	2.035
13	ha(2)	in2(2)	7	0.870
14	and(12)	out1(3)	7	0.870
15	inv_an82(126)	out1(2)	7	0.870
16	inv_an82(126)	w2(1)	76	0.330
17	pmos_an78(122	w2(3)	76	0.330
18	pmos_an79(123	w2(3)	76	0.330
19	nmos_an80(124	w2(3)	76	0.450
20	nmos_an80(124	w4(1)	77	0.120
21	nmos_an81(125	w4(3)	77	0.120
22	xornew_ha15(59	sum(3)	8	1.425
23	xornew_ha15(59	in2(2)	7	0.870
24	and(12)	out1(3)	7	0.870
25	inv_an82(126)	out1(2)	7	0.870
26	inv_an82(126)	w2(1)	76	0.330

Fig.15Delay Report of 4-bit Array Multiplier

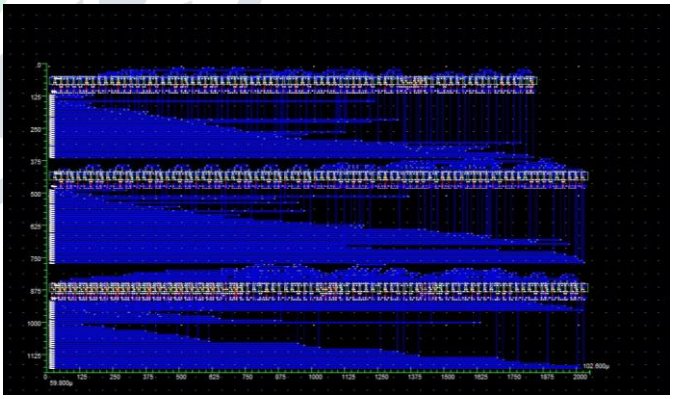


Fig.16 Layout Diagram

Results:

Delay: 5.720ns

Power: 89.275uw

Area: 102X32um

III. CONCLUSION

We comparatively examine the power, delay and area of Borrow Save Adder using 28T Full Adder and 10T Full Adder. We estimate the standard deviation of maximum delay for the two aforementioned architectures. The evaluation shows that 10T Full Adder BSA achieves smaller delay, power and area than 28T Full Adder. Furthermore it is possible to reduce the count of the transistor in the full adder so that delay , power and area further decreases.

IV. REFERENCES

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