A Novel Low power CMOS Compressors

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Abstract— VLSI circuit design is a rising demand as a computing platform in the digital CMOS designs that recompenses the compulsion of exact reckoning for enhancing speed and power performance. This paper proposes Novel low power CMOS compressors in which different compressors are designed like 3/2, 4/2, 5/3, 6/3. These compressors provide a better performance or speed for desired target fidelity. Comparison with the previous compressors, the proposed compressor designs provide a better performance in terms of power, area, delay and PDP. Lower power consumption and good performance simulation results are verified with the 90nm CMOS technology software.

Index Terms—compressors, power, delay, PDP, Area.

I . INDRODUCTION

Approximate computing has been proposed as an alternative to exact reckoning for the power reduction and improve the system performance for the digital design systems in terms of power, area and delay. This approach is becoming more and more important for the embedded computing systems which are characterized by energy and speed constraints. This can be successfully applied in some of the applications such as data-minnig, Multimedia processing, machine learning. Approximation can help to reduce the computation effort and lower the power consumption.

A Compressor is a logic circuit that takes N-bits of same significance and generates a sum bit with several carry bits as the output. Though the compressor gives the output as sum and carry but it is different from a conventional adder. Compressor adds N-bits of the same precision but a adder adds two operands of N-bit number of different precision. Compressors are XOR rich circuits which are also used for power reduction in terms of power, area and delay.

CMOS (Complementary metal oxide semiconductor) is a technology for the construction of integrated circuits such as microprocessors, static RAM and other digital logic circuits. The power dissipation is becoming a major problem in the CMOS logic due to which the error Probability increases and performance decreases. This is mainly due to two factors i.e, static and dynamic. The static power dissipation is defined as that both pmos and nmos have a gate-source threshold voltage, below which the current through the device Decreases exponentially. The CMOS circuits discharges power by charging the various load capacitances whenever they are switched which is termed as dynamic power dissipation. These dissipations can be reduced by some techniques like leakage power techniques, voltage scaling, etc.

In this proposed paper, we introduce a family of compressors which are aimed to reduce the power dissipation in CMOS. The Proposed compressors are designed using simple AND-OR gate (no XOR gates are used) and outplay the previously proposed circuits in terms of both precision and hardware complexity. These are then documented with the previous existing compressors using a 90nm CMOS technology.

This paper is described as follows. Section II describes the exact compressors which are used for the computation. The proposed CMOS compressors are summarized in the section III with comparion of workless with the previous existing works. Section IV gives the composite results and comparision with the previous approximate compressors, While the conclusion is taut in the section V.

II. EXACT COMPRESSORS

Let us consider two unsigned n bit inputs

$$X=x_{n-1}2^{n-1}+\ldots\ldots+x_0$$

$$Y= y_{n-1}2^{n-1}+\ldots\ldots+y_0$$

Then , the product Z, between X and Y is as below

$$Z = X.Y=P_{2n-1}2^{2n-1}+\ldots..+P_0 \qquad (1)$$

The partial products is given by

$$S= \{P_0, P_1, P_2\ldots\ldots\ldots P_{j-1}\} \qquad (2)$$

A compressor computes the arithmetic sum in the equation (2) and encodes the desired results in the binary format. The most commonly used compressor is full adder circuit which has 3 inputs and with output divided into two that is sum and carry. But in the AND-OR design there is no sum and carry output. The outputs are the expressions of logical AND and logical OR.

III. PROPOSED CMOS COMPRESSORS

The proposed CMOS compressors are explained in the following estimated way as the arithmetic sum as in equation (2).

A . ESTIMATED 2/1 COMPRESSOR

Let us consider two inputs P_0 and P_1 such that the output is denoted by W_1. Here the name itself indicates that there are two inputs and one output.

The sum of the partial products is given as follows,

$S= \{P_0, P_1\}$ (3)

The output of the 2/1 compressor is

$W_1= \{P_0P_1, P_0+P_1\}$ (4)

Eq(3) represents the outputs of the two partial inputs which are specified by using the logical AND and logical OR circuits.

Table I

2/1 Compressor Truth table

Estimated 2/1 Compressor		
P_1	P_0	W_1
0	0	0
0	1	1
1	0	1
1	1	1

Table I shows the behavior of the proposed CMOS estimated 2/1 compressor.

B. ESTIMATED 3/2 COMPRESSOR

The term 3/2 compressor itself indicates that the compressor comprises of three inputs and two outputs. The AND-OR logic diagram for 3/2 Compressor in the CMOS logic is as shown below.

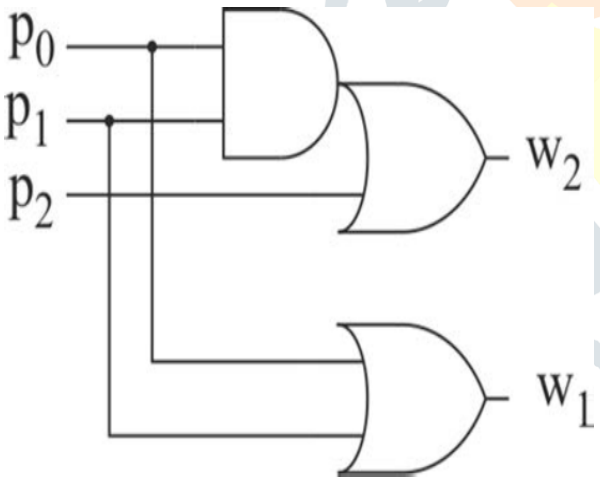


Fig: 1. Schematic of proposed 3/2 Compressor

From the logic diagram we obtain the following equations

$$S= \{P_0P_1, P_0+P_1, P_2\} \quad (5)$$

$$W_1 = (P_0P_1+ P_2) \quad (6)$$

$$W_2 = (P_0 + P_1) \quad (7)$$

Eq (5) represents the sum of the partial products in the logical diagram.

Eqs (6) and (7) are the output expressions of the proposed 3/2 compressor.

Table II

3/2 compressor Truth table

Estimated 3/2 Compressor				
P_2	P_1	P_0	W_2	W_1
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Table II shows the behavior of the proposed 3/2 compressor.

C. ESTIMATED 4/2 COMPRESSOR

The proposed 4/2 compressor comprises of four inputs i.e, P0, P1, P2,P3 and two outputs as of suggested in the name itself. The Logical AND-OR diagram for the proposed 4/2 compressor is as shown below.

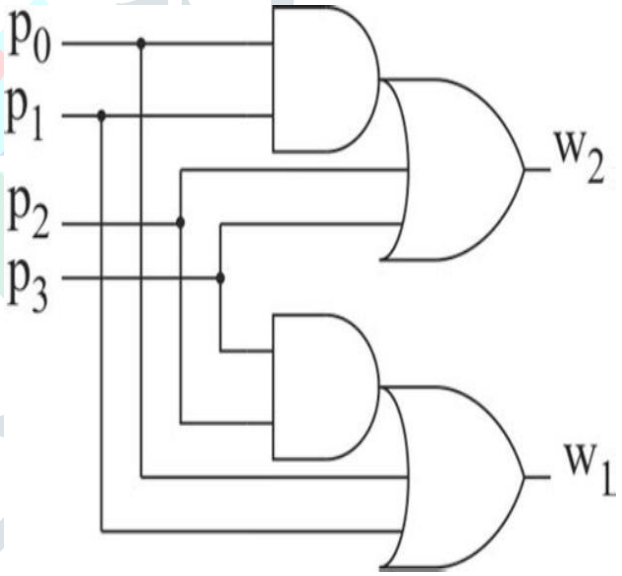


Fig : 2. Schematic of estimated 4/2 compressor

The sum of the partial products is written as follows,

$$S= \{P_0P_1, P_2P_3, P_2+P_3, P_1+P_0\} \quad (8)$$

The AND-OR expressions for the given logic diagram is as follows

$$W_1 = P_2 P_3+ P_0+P_1 \quad (9)$$

$$W_2 = P_0 P_1+ P_2+P_3 \quad (10)$$

Eq (8) represents the partial products of the above

proposed logic diagram i.e, fig 2.

Eq(9) and (10) shows the logical expressions for the proposed 3/2 compressor using AND-OR logic designs

Table III

4/2 Compressor Truth table

Estimated 4/2 Compressor					
P_3	P_2	P_2	P_0	W_2	W_1
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	1	0
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

Table III shows the behavior of the proposed CMOS 4/2 compressor.

D. ESTIMATED 5/3 COMPRESSOR

The proposed 5/3 compressor comprises of five inputs and the 3 estimated outputs. The logical diagram for the estimated 5/3 compressor is as shown below.

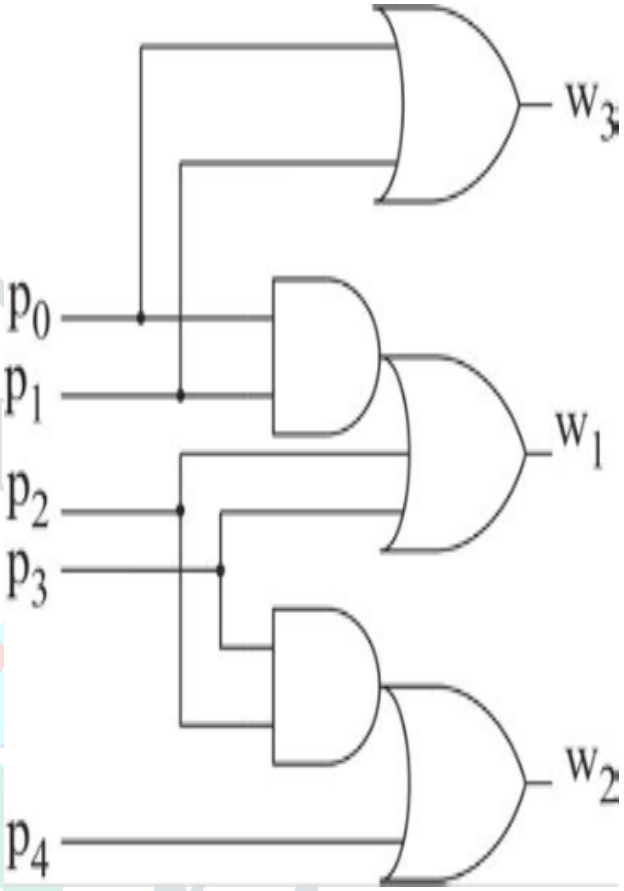


Fig: 3. Schematic of estimated 5/3 Compressor

The sum of partial products is as follows

$$S= \{ P_0P_1, P_2P_3, P_0+P_1, P_2+P_3, P_4 \} \quad (11)$$

The logical expressions to get the desired output is

$$W_1 = P_0 P_1+P_2+P_3 \quad (12)$$

$$W_2 = P_2P_3+P_4 \quad (13)$$

$$W_3 = P_0+P_1 \quad (14)$$

Eq (12),(13), and (14) are the output expressions obtained by the AND-OR logic for the proposed 5/3 compressor.

Table IV represents the behavior of the proposed 5/3 compressor for only partial products.

Table IV

5/3 Compressor Truth table

Estimated 5/3 compressor							
P_4	P_3	P_2	P_1	P_0	W_3	W_2	W_1
0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	1	0	1
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	1
0	0	1	1	0	1	0	1
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	1	0	1
0	1	0	1	0	1	0	1
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	1
0	1	1	0	1	1	1	1
0	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1
1	0	0	0	0	0	1	0
1	0	0	0	1	1	1	0
1	0	0	1	0	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	0	0	1	1
1	0	1	0	1	1	1	1
1	0	1	1	0	1	1	1
1	0	1	1	1	1	1	1
1	1	0	0	0	0	1	1
1	1	0	0	1	1	1	1
1	1	0	1	0	1	1	1
1	1	0	1	1	1	1	1
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1
1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1

E. ESTIMATED 6/3 COMPRESSOR

The name 6/3 compressor suggests that the compressor comprises of six inputs and three outputs. The logical diagram for the proposed 6/3 compressor is as shown in the figure.

The sum of partial products is as follows,

$$S = \{ P_0P_1, P_2P_3, P_2+P_3, P_4+P_5, P_4P_5, P_0+P_1\} \quad (15)$$

The logical expressions for the desired outputs is as follows

$$W_1 = P_0\, P_1+P_2+P_3 \quad (16)$$

$$W_2 = P_4P_5+P_0+P_1 \quad (17)$$

$$W_3 = P_2P_3+ P_4+P_5 \quad (18)$$

Eq (16),\(17),(18) represent the output logics expressions for the proposed 6/3 compressor using AND-Or gates.

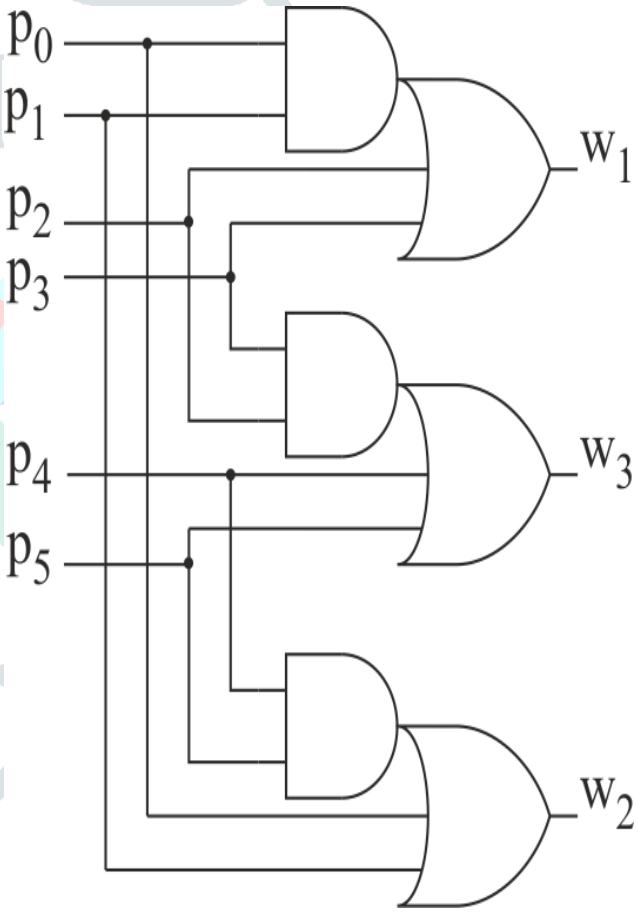


Fig: 4. Schematic of estimated 6/3 compressor

Table V represents the behavior of the proposed 6/3 compressor.

Table V

6/3 compressor Truth table

P_5	P_4	P_3	P_2	P_1	P_0	W_3	W_2	W_1
0	0	0	1	1	1	0	1	1
0	0	1	0	1	1	0	1	1
0	0	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1
0	1	1	0	1	1	1	1	1
0	1	1	1	0	1	1	1	1
0	1	1	1	0	0	1	0	1
0	1	1	1	0	1	1	1	1
0	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1
1	0	1	1	0	0	1	0	1
1	0	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	1
1	1	0	0	0	1	1	1	0
1	1	0	0	1	0	1	1	0
1	1	0	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1
1	1	0	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1
1	1	1	0	0	1	1	1	1
1	1	1	0	1	0	1	1	1
1	1	1	0	1	1	1	1	1
1	1	1	1	0	0	1	1	1
1	1	1	1	0	1	1	1	1
1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1	1

IV. IMPLEMENTATION OF RESULTS

The results of all the proposed CMOS compressors using the AND-Or logic circuits in the 90nm technology are obtained. The Transistor logic diagram, delay report, simulation results are as shown below.

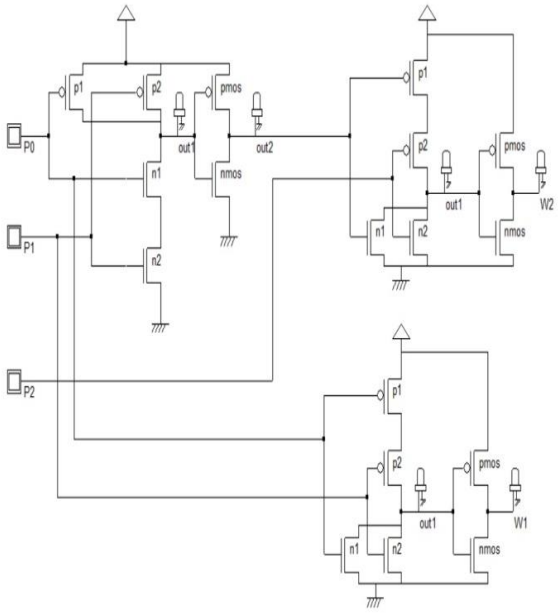
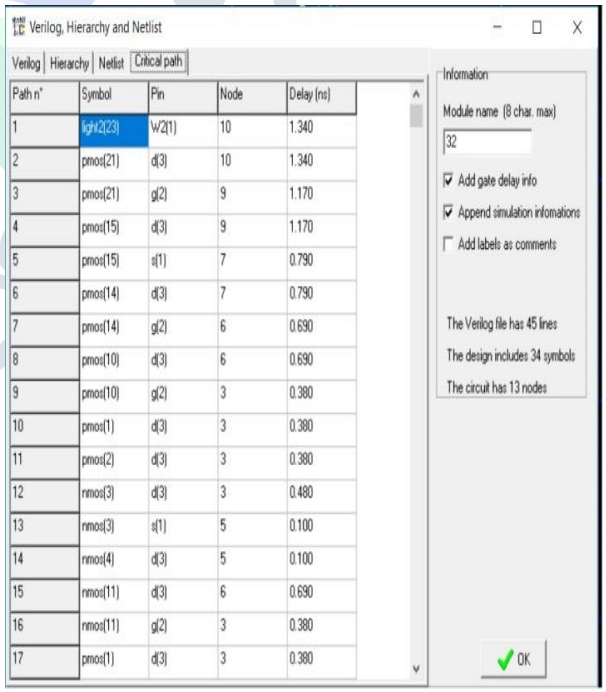


Fig: 5. 3/2 compressor logic diagram using AND-OR gate



Path n°	Symbol	Pin	Node	Delay (ns)
1	light2(23)	W2(1)	10	1.340
2	pmos(21)	d(3)	10	1.340
3	pmos(21)	g(2)	9	1.170
4	pmos(15)	d(3)	9	1.170
5	pmos(15)	s(1)	7	0.790
6	pmos(14)	d(3)	7	0.790
7	pmos(14)	g(2)	6	0.690
8	pmos(10)	d(3)	6	0.690
9	pmos(10)	g(2)	3	0.380
10	pmos(1)	d(3)	3	0.380
11	pmos(2)	d(3)	3	0.380
12	nmos(3)	d(3)	3	0.480
13	nmos(3)	s(1)	5	0.100
14	nmos(4)	d(3)	5	0.100
15	nmos(11)	d(3)	6	0.690
16	nmos(11)	g(2)	3	0.380
17	pmos(1)	d(3)	3	0.380

Fig: 6. 3/2 compressor CMOS Circuits Delay report

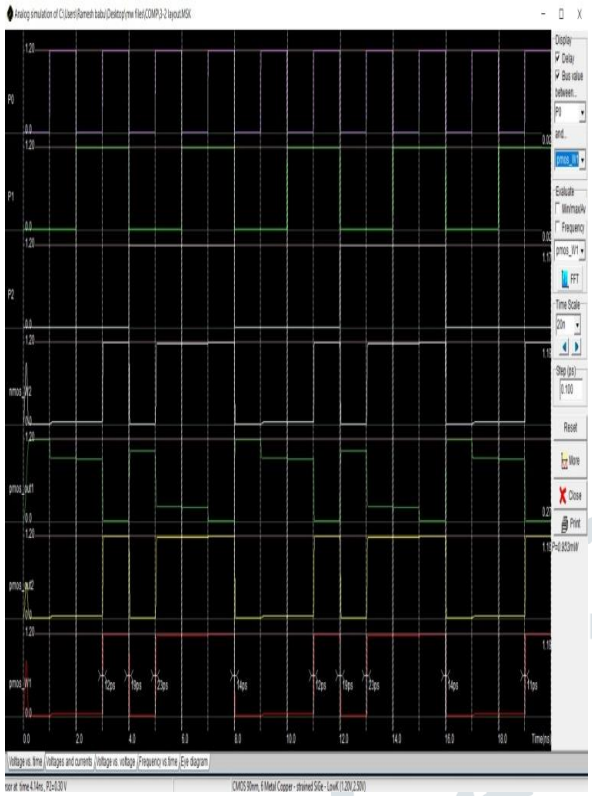
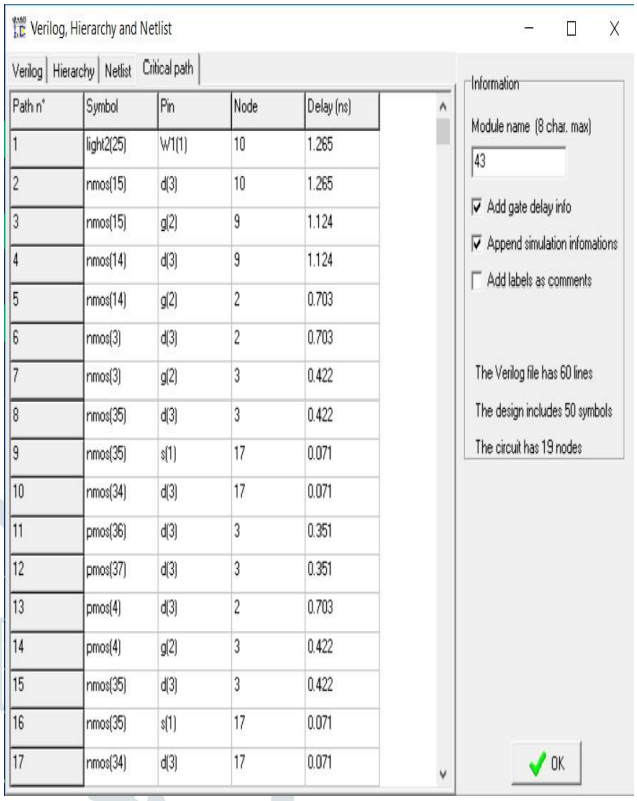


Fig: 7. 3/2 Compressor CMOS Circuit Simulation Results



Path n°	Symbol	Pin	Node	Delay (ns)
1	light2(25)	W1(1)	10	1.265
2	nmos(15)	d(3)	10	1.265
3	nmos(15)	g(2)	9	1.124
4	nmos(14)	d(3)	9	1.124
5	nmos(14)	g(2)	2	0.703
6	nmos(3)	d(3)	2	0.703
7	nmos(3)	g(2)	3	0.422
8	nmos(35)	d(3)	3	0.422
9	nmos(35)	s(1)	17	0.071
10	nmos(34)	d(3)	17	0.071
11	pmos(36)	d(3)	3	0.351
12	pmos(37)	d(3)	3	0.351
13	pmos(4)	d(3)	2	0.703
14	pmos(4)	g(2)	3	0.422
15	nmos(35)	d(3)	3	0.422
16	nmos(35)	s(1)	17	0.071
17	nmos(34)	d(3)	17	0.071

Fig: 9. 4/2 Compressor CMOS Circuits Delay report

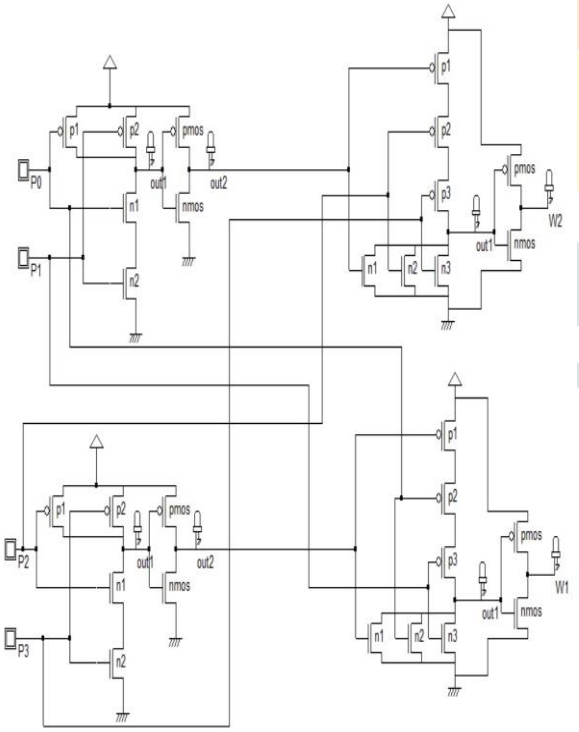


Fig: 8. 4/2 Compressor logic diagram using AND-OR gates

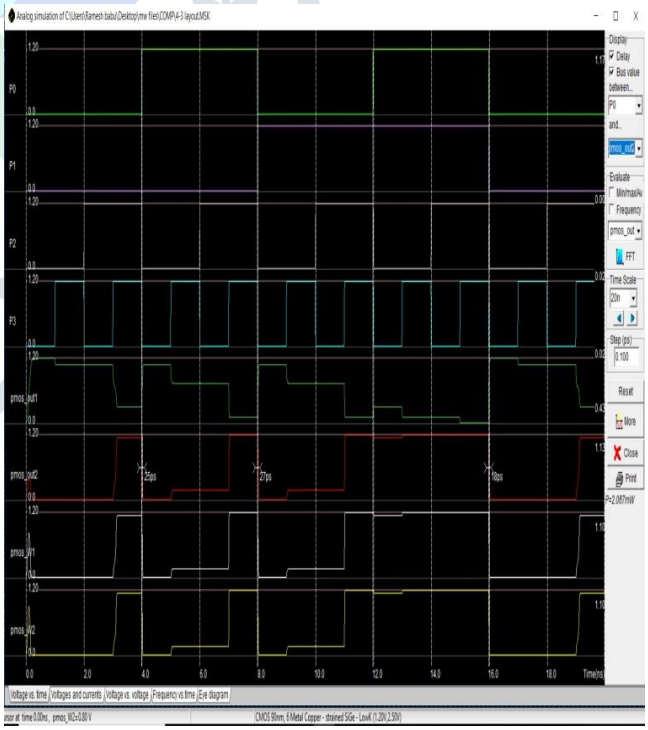


Fig: 10.4/2 Compressor CMOS Circuit Simulation Results

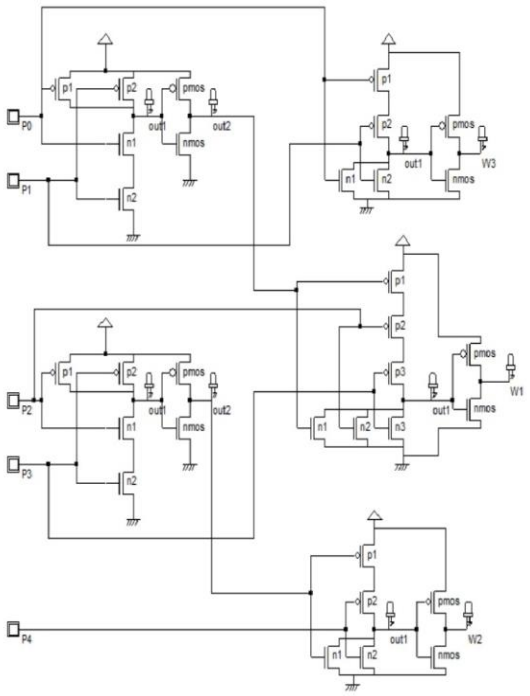
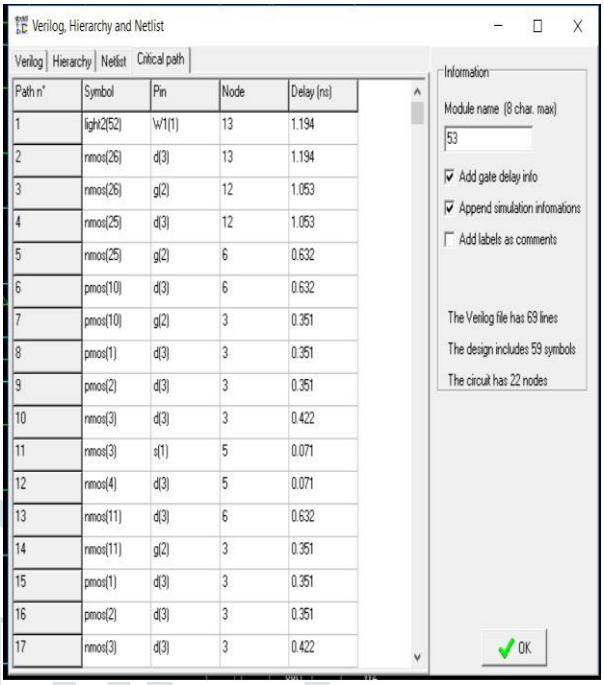


Fig: 11. 5/3 compressor logic diagram using AND-OR gates



Path n°	Symbol	Pin	Node	Delay (ns)
1	light2(52)	W1(1)	13	1.194
2	nmos(26)	d(3)	13	1.194
3	nmos(26)	g(2)	12	1.053
4	nmos(25)	d(3)	12	1.053
5	nmos(25)	g(2)	6	0.632
6	pmos(10)	d(3)	6	0.632
7	pmos(10)	g(2)	3	0.351
8	pmos(1)	d(3)	3	0.351
9	pmos(2)	d(3)	3	0.351
10	nmos(3)	d(3)	3	0.422
11	nmos(3)	s(1)	5	0.071
12	nmos(4)	d(3)	5	0.071
13	nmos(11)	d(3)	6	0.632
14	nmos(11)	g(2)	3	0.351
15	pmos(1)	d(3)	3	0.351
16	pmos(2)	d(3)	3	0.351
17	nmos(3)	d(3)	3	0.422

Fig: 13.5/3 Compressor CMOS Circuit Delay report

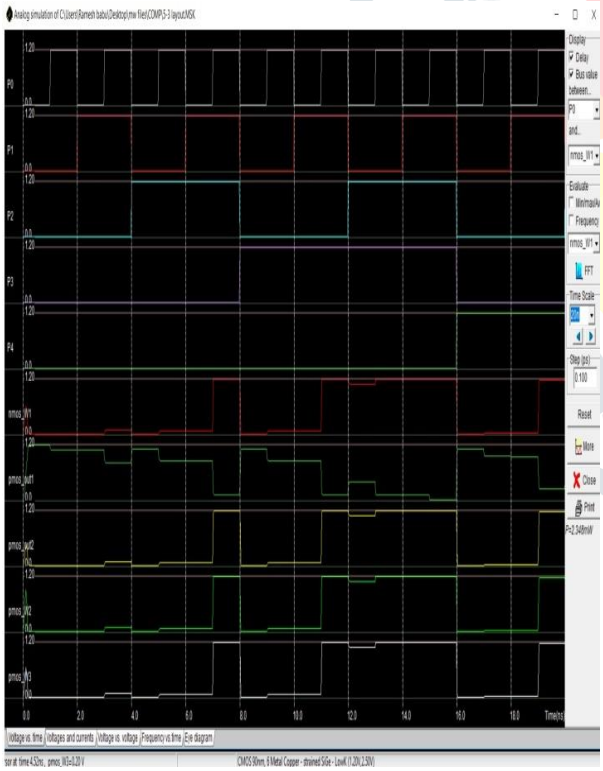


Fig: 12. 5/3 Compressor CMOS Circuit Simulation Results

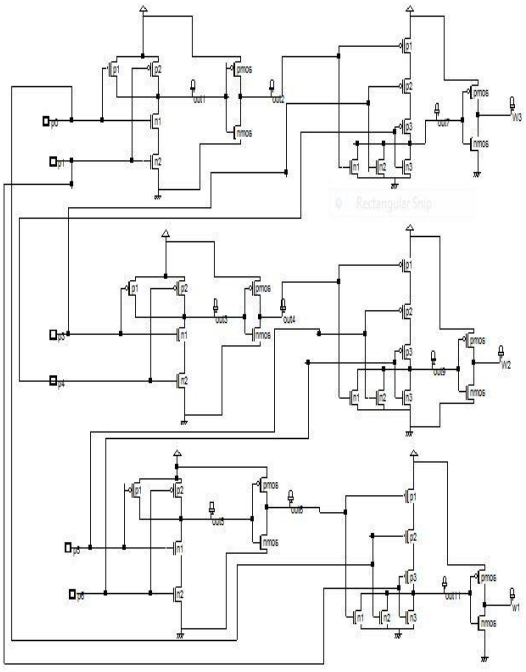


Fig: 14. 6/3 compressor logic diagram using AND-OR gates

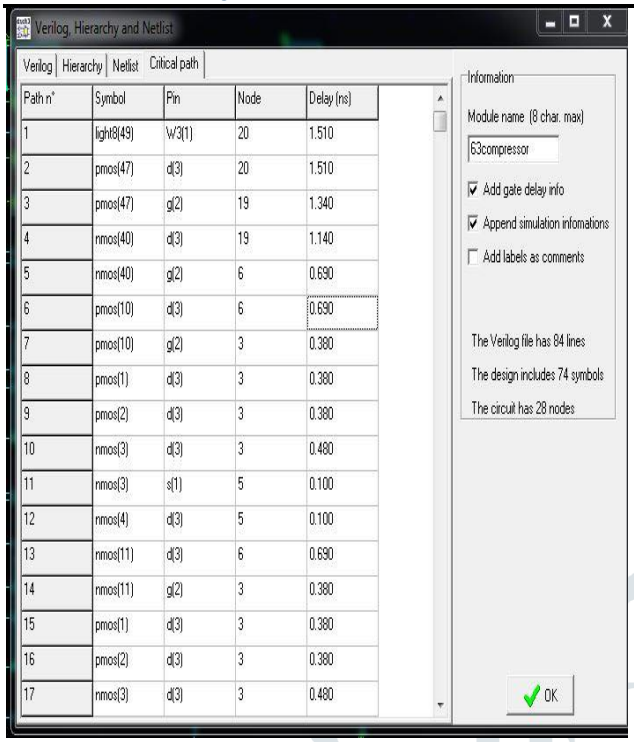


Fig: 15. 6/3 Compressor CMOS Circuit Delay Report

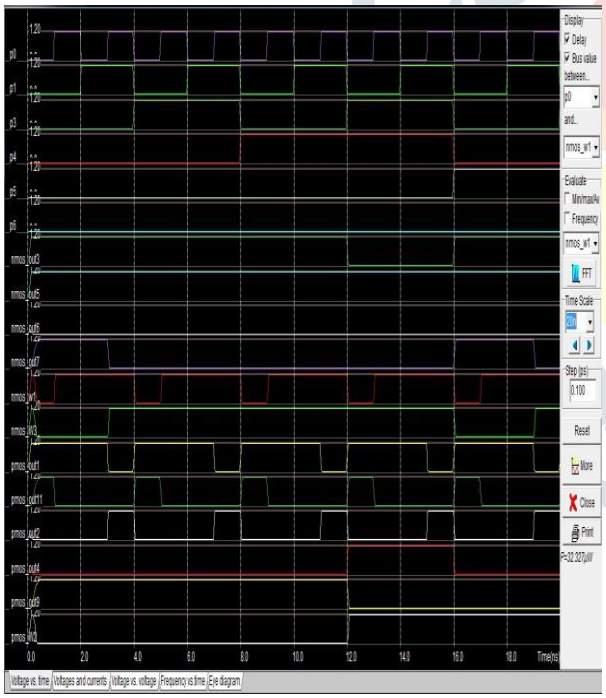


Fig: 16. 6/3 Compressor CMOS Circuit Simulation Results

Proposed methods	Power (W)	Delay (ns)	PDP (femito)	Area (μm^2)
3/2 compressor	0.953 mW	1.340	1.277	40.68
4/3 compressor	2.067 mW	1.265	2.614	583.95
5/3 compressor	2.348 mW	1.194	2.803	1014.6
6/3 compressor	32.327 µW	1.510	48.813	1327.37

V. CONCLUSION

In this paper, the proposed CMOS compressors compared with the existing workless power consumption and high performance. These proposed work with less power consumption and the good performance results are documented in the 90nm CMOS technology software.

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