Optimisation Techniques for Static Power Dissipation in VLSI Circuits

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***Abstract* :** In Today's market, energy consumption to perform any task is of utmost importance. Life of battery operated devices can be enhanced by considering dynamic and leakage power as the primary goal for VLSI circuits. Electronic industries have developed various technologies focussing on size compactness for power reduction. This paper concentrates mainly on static power dissipation. There are eight techniques that are introduced in this paper which lowers the leakage power in the circuit. Paper concentrates on the static power dissipation which is caused by subthreshold voltage and current. Realization of these circuits is done using VLSI designing tool TannerEDA 11.2.

I. INTRODUCTION

Power dissipation in CMOS circuits is caused by: **Dynamic Power dissipation** (P_D) is caused by the charging and discharging of capacitor at the load side, also caused by the "short-circuit" current when nMOS and pMOS are partially ON.

Static Power dissipation (P_S) is caused by the subthreshold leakage when pMOS and nMOS transistors are in OFF state, also affected by the gate leakage through gate dielectric and junction leakage at source/drain diffusions and contention current[2].

Total power dissipated through the circuit is:

$$P_T = P_S + P_D \quad (1)$$

Static Power Dissipation: Static power is dissipated when the circuit is in OFF state. CMOS is used instead of nMOS circuits as the contention current ingrained to nMOS logic transistors uses limited transistors which are allowed to be integrated on a single chip. And also there is no contention current in static CMOS circuits. Static power is caused from subthreshold, gate and junction leakage currents and contention current. [3, 5]

Dynamic Power Dissipation: Dynamic Power is the switching power dissipation as the power is dissipated when MOSFETs are in ON operation. It is caused only when there is a continuous process of switching and leakage power due to leakage current. It can be reduced by reducing the switching process and the clock frequency of the circuit. Dynamic power, comprises switching power (P_{SP}) and the short-circuit power (P_{SCP}). Switching power is caused due to dissipated in the load capacitor. And later is dissipated by the continuous connection between V_{DD} and GND when the gate switches their states.

$$P_D = P_{SP} + P_{SCP} \quad (2)$$

LOW POWER CIRCUIT TECHNIQUES

Sleep Transistor Technique

During the sleep mode, it is the simplest way to lower down the static current. This technique is also called power gating technique and Multi-Threshold CMOS (MTCMOS) as it reduces the standby or leaky power. [3]

One of the two high threshold valued sleep transistors is positioned in between V_{DD} and pull-up network (pMOS) and other is positioned in between pull-down network (nMOS) and GND.

pMOS transistor is pull-up network whereas nMOS transistor is pull-down network are used in place of two high valued sleep transistors.

When the mode of operation is active, the sleep transistors must operates i.e. goes ON, a high logic signal (SLP) i.e. logic 1 and a low logic signal (SLPbar) i.e. logic 0 is given to both the sleep transistors. Thus, there is a lower potential difference between Vp and Vn, which reduces the current to flow through the circuit and hence power gets reduced, where Vp and Vn are the potentials between 2 pMOS and 2 nMOS respectively.

When the mode of operation is standby, both sleep transistors will not operate i.e. goes OFF, a low logic signal (SLPbar) i.e. logic 0 and a high logic signal (SLP) i.e. logic 1 is given to both the sleep transistors respectively.

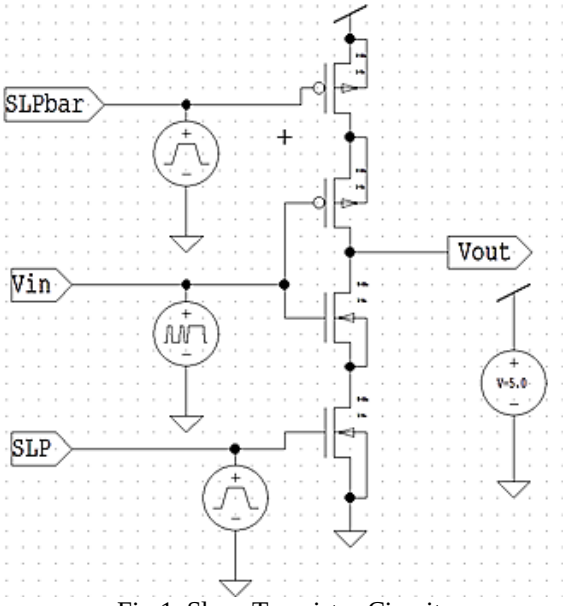

Fig 1. Sleep Transistor Circuit

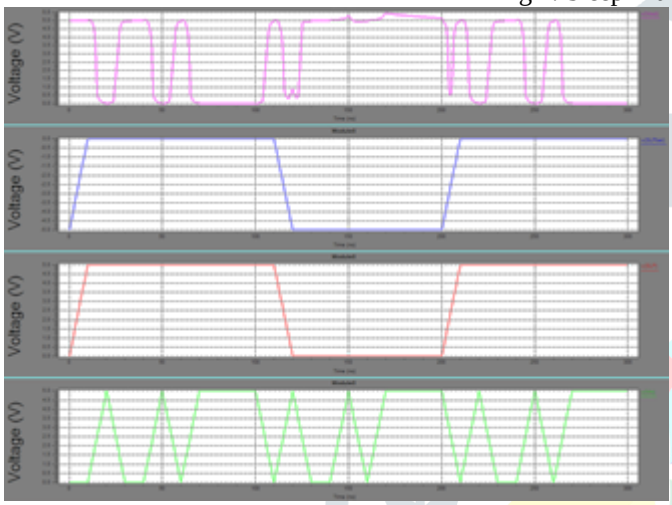

Fig 2. Waveform for Active Mode

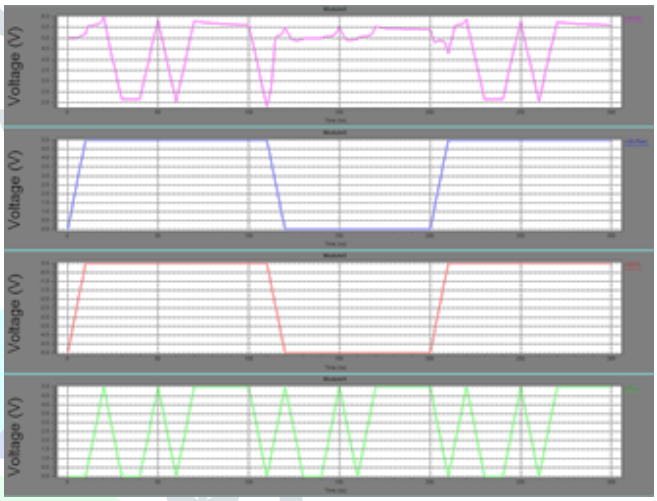

Fig 3. Waveform for Standby Mode

The circuit goes on high impedance state which lowers the leakage current hence reduces the power dissipation.

State Retention Low Leak Inverter

In latter technique, the present state is lost at its corresponding output in the active mode of operation, to retain the present state in order to have its corresponding output, state retention low leak inverter technique comes into account. To retain the present state, a state retaining transistor will connect to sleep transistors in parallel. There are 4 sleep transistors in this circuit of inverter connected in parallel on either side of pMOS and nMOS respectively.[4] State Retention Low Leak Inverter works majorly on 4 modes of operation, these are:

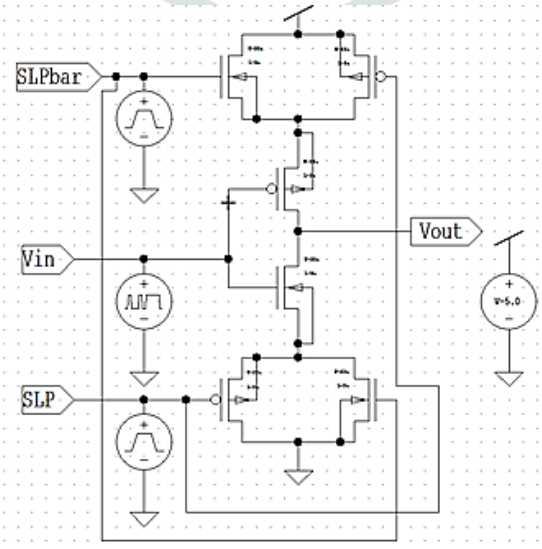

Fig 4. State Retention Low Leak Inverter Circuit

a. **Deep Sleep Mode:** When a high logic signal (SLP) i.e. logic 1 and low logic signal (SLPbar) i.e. logic 0 are provided to sleep transistors respectively then these sleep transistors goes in OFF state. By providing these signals, a high resistance network forms between V_{DD} and GND, hence leakage current lowers accordingly.

b. **Active Mode:** When a high logic signal (SLP) i.e. logic 1 and low logic signal (SLPbar) i.e. logic 0 are provided to sleep transistors respectively then sleep transistors goes in ON. The Vout provides adequate voltage level.

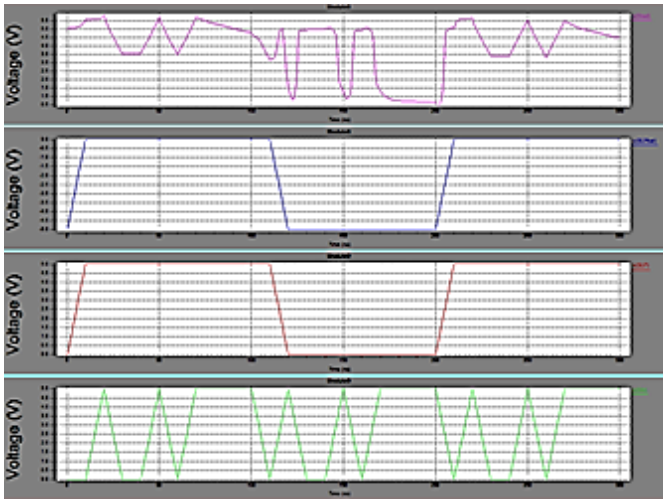

Fig 5. Waveform for Deep Sleep Mode

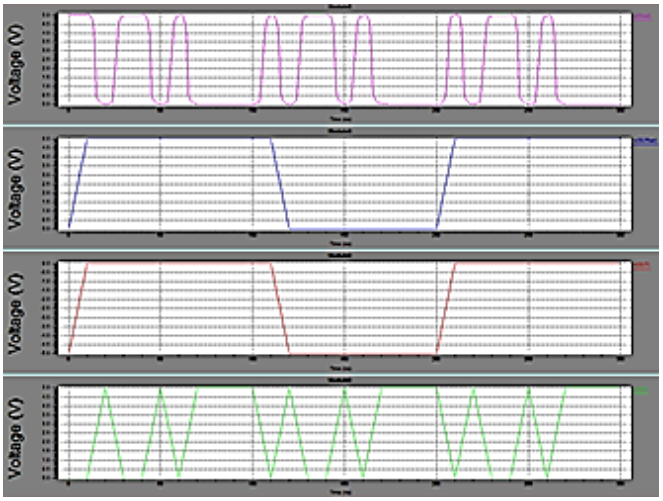

Fig 6. Waveform for Active Mode

c. **State Retention with good logic 0:** When a high logic signal (SLP) i.e. logic 1 is provided to all the sleep transistors. By providing only signal to transistors, leakage current lowers as one transistor goes in OFF state.

d. **State Retention with good logic 1:** When a low logic signal (SLPbar) i.e. logic 0 is provided to all the sleep transistors. By providing only signal to transistors, leakage current lowers state retention occurs.

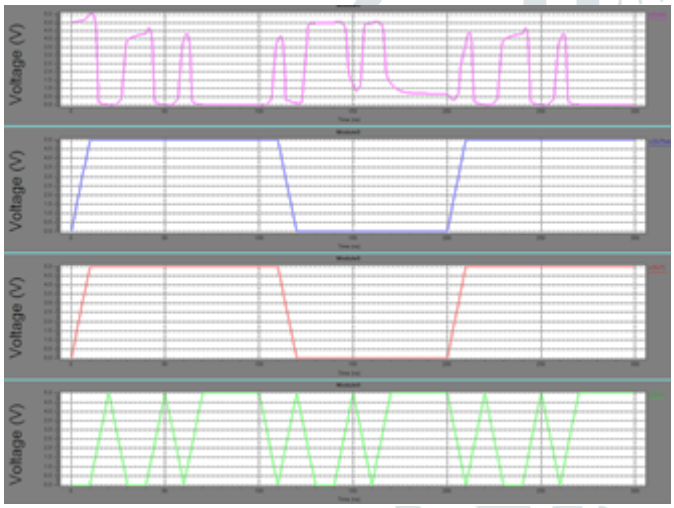

Fig 7. Waveform for State Retention Good Logic 0

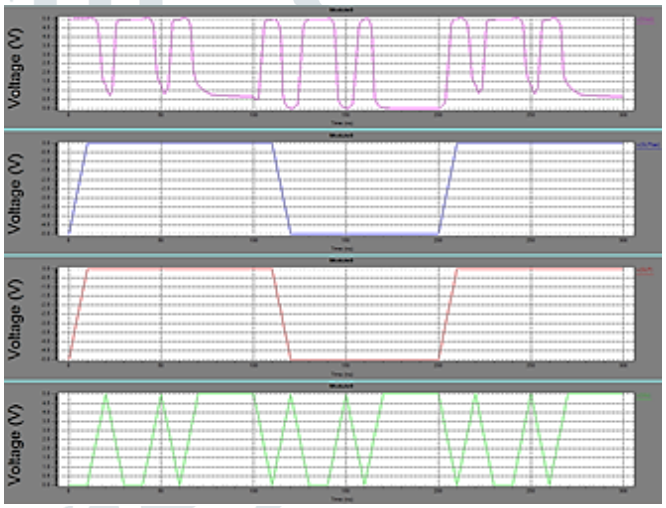

Fig 8. Waveform for State Retention Good Logic 1

Transistor Gating (TG) Technique

As the name suggests, this technique lowers the flow of leaky current by padding extra sleep transistors in between supply voltage (V_{DD}) and ground (GND). Out of two sleep transistors, one is positioned in between V_{DD} and pull-up network (pMOS network) whereas other is positioned between pull-down network (nMOS) and GND.

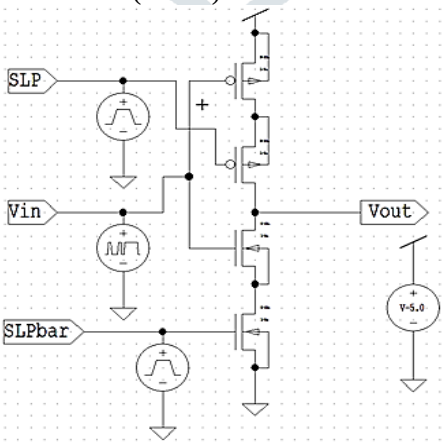

Fig 9. Transistor Gating Circuit

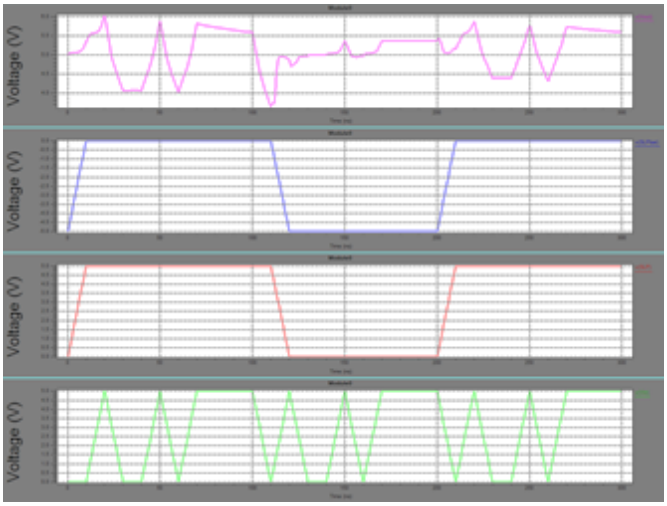

Fig 10. Waveform for TG when SLP = 1, SLPbar = 0

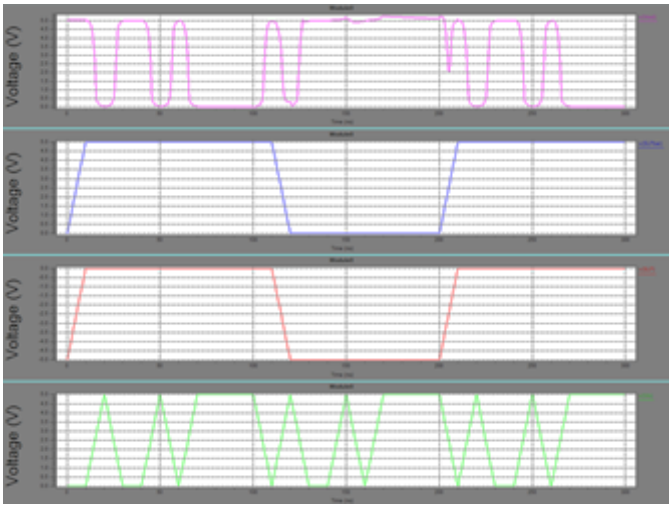

Fig 11. Waveform for TG when SLP = 0, SLPbar = 1

Zig-Zag Technique

The design of the circuit resembles with the name of the technique 'Zig-Zag'. In Zig-Zag Technique, one sleep transistor is used either along pull-up (PUN) or along pull-down (PDN) network depending on the output required. Due to this, leakage power consumption is lowest. [1]

If the required output is logic 1, sleep transistor is positioned in between nMOS network and GND whereas if the required output is logic 0, sleep transistor is placed between pMOS network and V_{DD}. This technique works for the reduction of the wakeup cost of the sleep transistor when required.

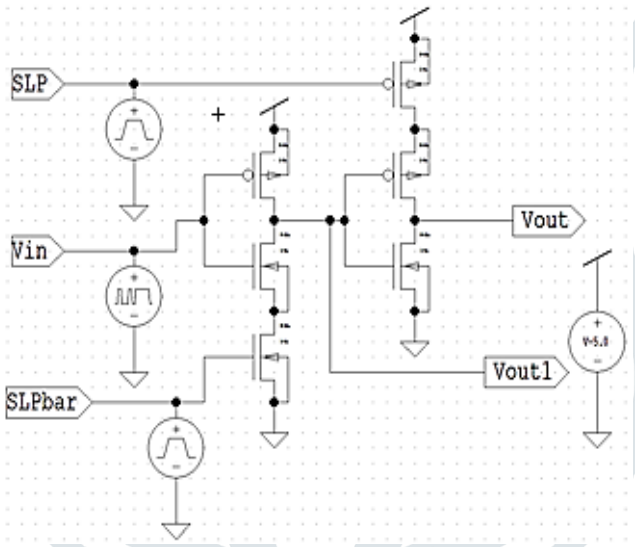

Fig 12. Zig-Zag Circuit

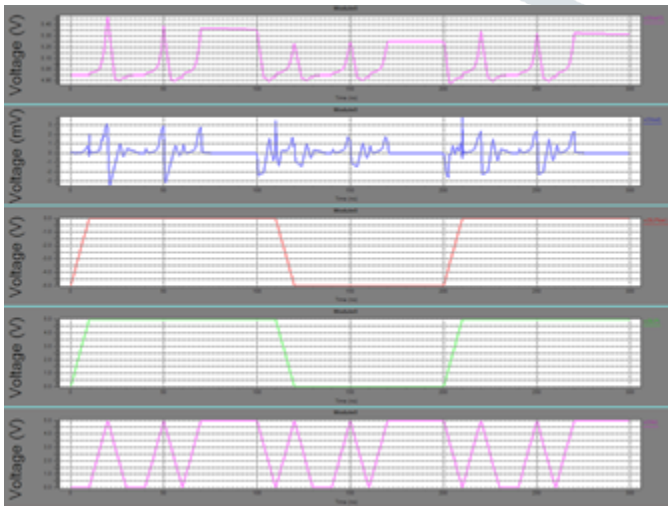

Fig 13. Waveform for Zig-Zag when SLP = 1, SLPbar = 0

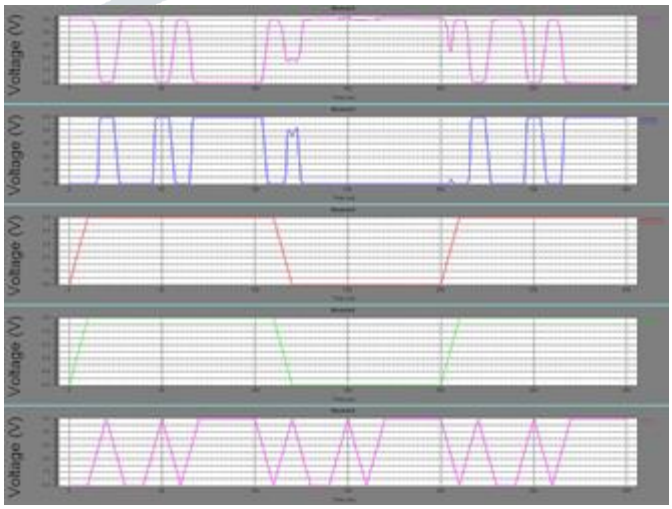

Fig 14. Waveform for Zig-Zag when SLP = 0, SLPbar = 1

Stack Technique

This technique also lowers the leakage power by dividing the transistor on the basis of their aspect ratio into two equal halves, like if the aspect ratio of a transistor is 6, then this transistor is replaced with two transistors having aspect ratio of 3 each. Due to this,

when two transistors goes in non-operative state together then reverse biasing induces in between those two transistors, hence flow of subthreshold leakage current occurs which is lowered due reverse biasing.[4] Due to the division of size of the transistors, delay get increased which limits the use of stack technique.

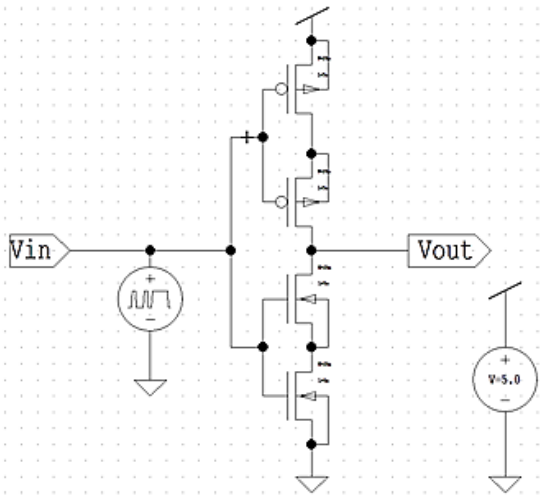

Fig 15. Stack Circuit

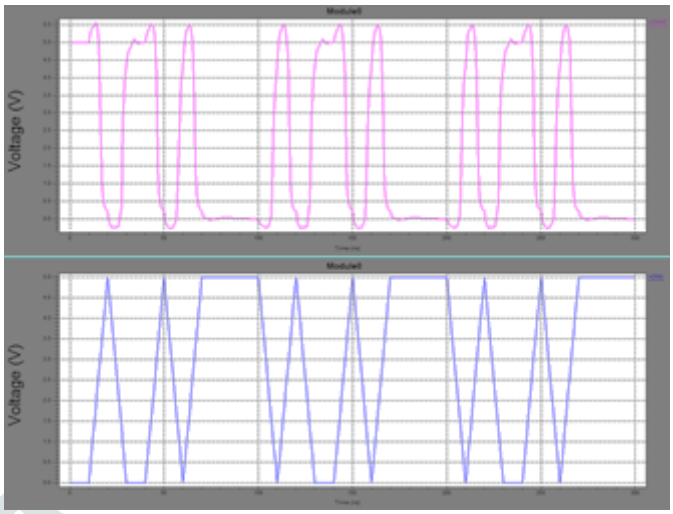

Fig 16. Waveform for Stack Technique

Sleepy Keeper Approach

CMOS (pMOS and nMOS) technology, when pMOS is linked to V_{DD} and nMOS is linked to ground (GND), works as an inverter. pMOS and nMOS transistors have a disadvantage that they are not efficient when GND and V_{DD} is passed through them respectively.[4]

As the name of this technique denotes that sleep mode has to be maintained i.e if a high logic value (logic 1) is to be maintained when it is already the logic 1 by calculation, the technique sleepy keeper approach utilize the high logic output by connecting nMOS transistor to V_{DD} along with pull-up network in order to maintain logic 1 output in sleep mode. In sleep mode, this nMOS transistor is the transistor which is making connection from V_{DD} to pMOS network as sleep transistor goes in OFF state.

If low logic value (logic 0) is to be maintained when given that logic 0 value has already been calculated, the technique sleepy keeper approach utilizes the low logic output by connecting pMOS transistor to GND along with nMOS network in order to maintain logic 0 output in sleep mode. In sleep mode, this pMOS transistor is the transistor which is making connecting network from GND to nMOS network as sleep transistor goes in OFF state.

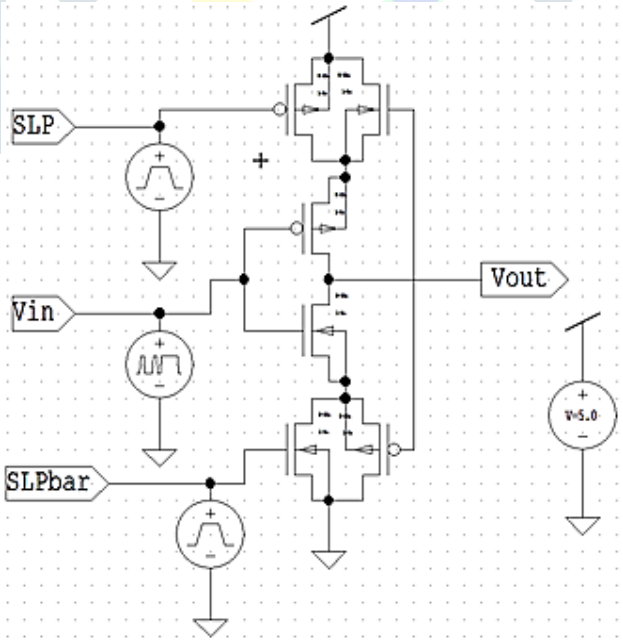

Fig 17. Sleepy Keeper Circuit

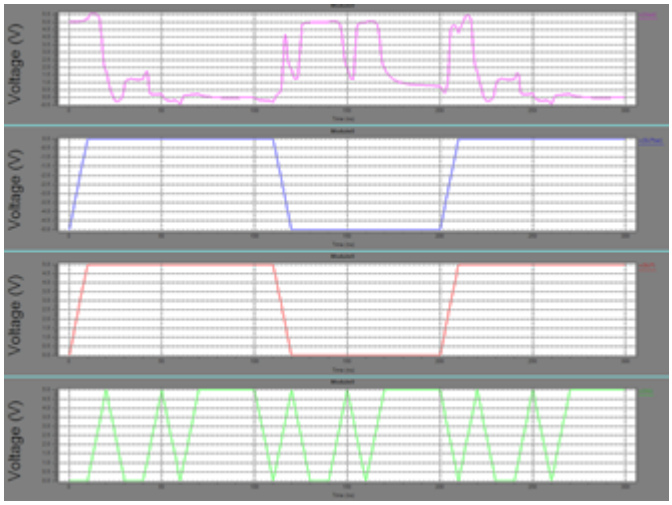

Fig 18. Waveform when SLP = 1, SLPbar = 0

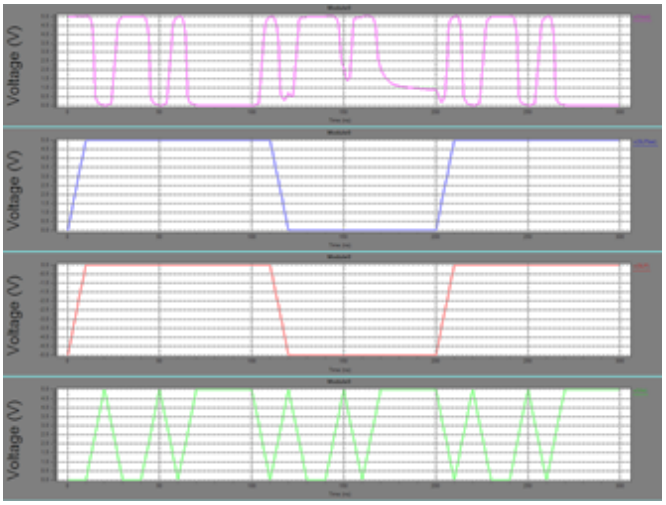

Fig 19. Waveform when SLP = 0, SLPbar = 1

Sleepy Stack

The technique name shows that it is the combination of Sleepy Keeper Approach and Stack Approach. In this technique, there is division of the transistor on the basis of their aspect ratio into two equal halves, a parallel connection between sleep transistor and divided transistors is done. Transistors are divided on the basis of their aspect ratio, which are responsible for the reduction of leakage power by retaining the states. The sleep transistors operates same as they works in Sleep technique i.e. turns ON or operates in active mode whereas turns OFF or not operates in sleep mode.[4]

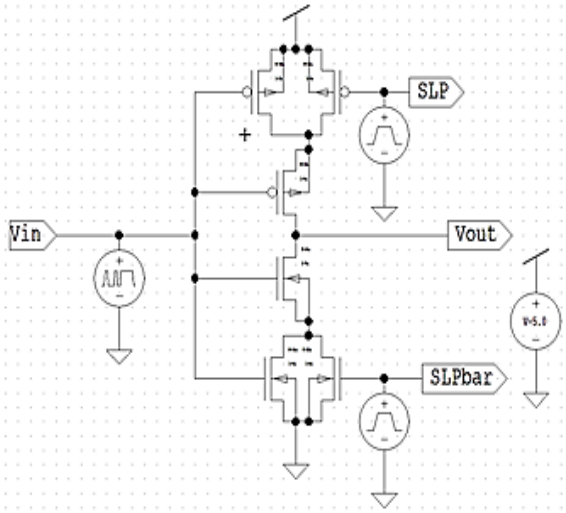

Fig 20. Sleepy Stack Circuit

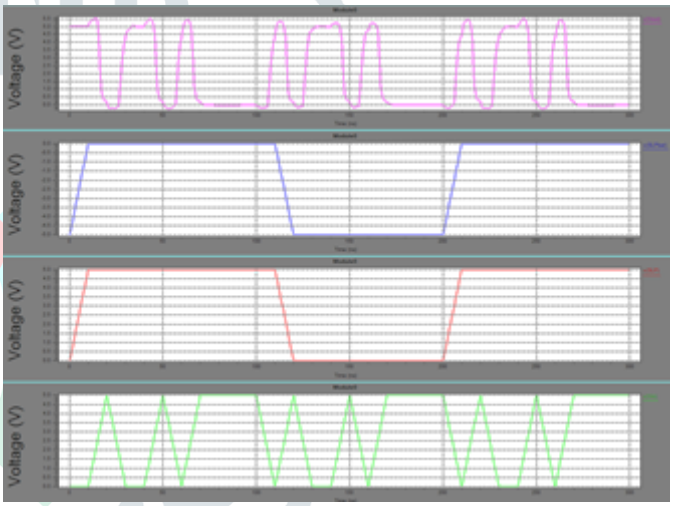

Fig 21. Waveform for Sleepy Stack when SLP = 1, SLPbar = 0

Zig-Zag Sleepy Keeper Approach

It is combination of Zig-Zag and Sleepy Keeper Approach techniques. It uses sleep transistor along with additional transistor which operates on calculated output which further helps to maintain the state of circuit during sleep mode. Hence, this technique achieves the aim of power optimization without losing the state i.e. retains the state. [1]

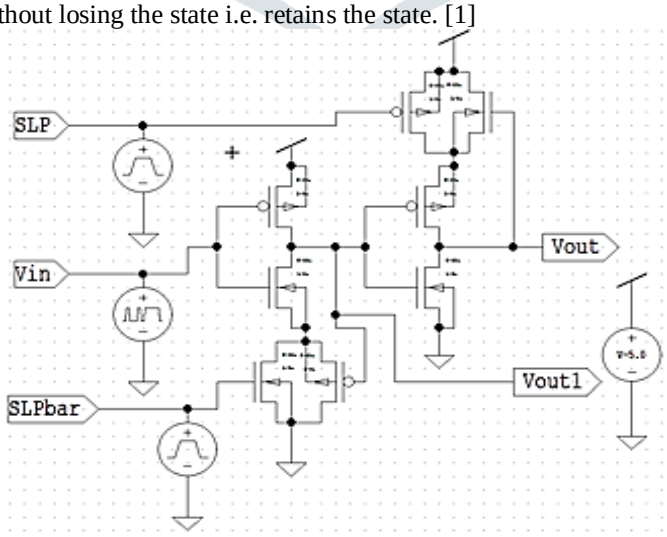

Fig 22. Zig-Zag Sleepy Keeper Circuit

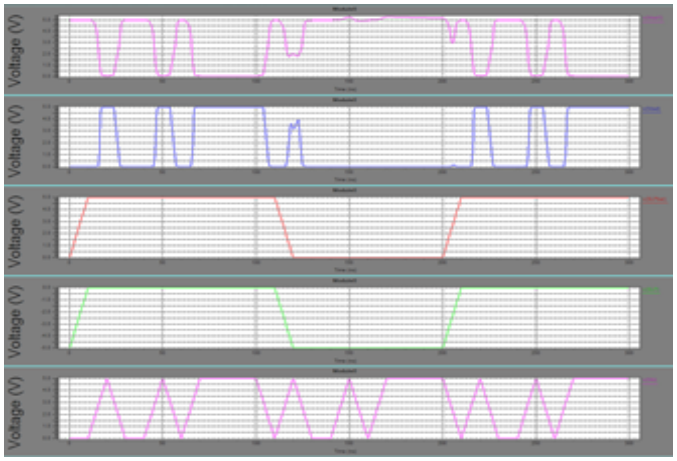

Fig 23. Waveform when SLP = 0, SLPbar = 1

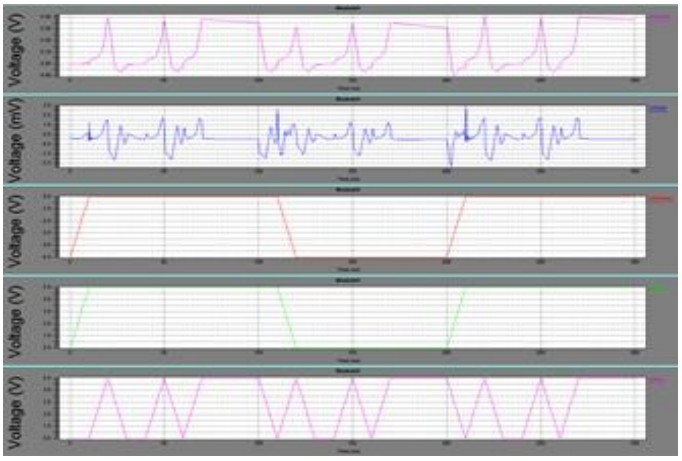

Fig 24. Waveform when SLP = 1, SLPbar = 0

RESULT

Table 1: Descriptive Statics

Technique	Fig. No.	SLP	SLPbar
Sleep Transistor Active Mode	2	1	0
Sleep Transistor Standby Mode	3	0	1
State Retention Low Leak Inverter Deep Sleep Mode	5	1	0
State Retention Low Leak Inverter Active Mode	6	0	1
State Retention Low Leak Inverter Good Logic 0	7	0	0
State Retention Low Leak Inverter Good Logic 1	8	1	1
Transistor Gating	10	1	0
Transistor Gating	11	0	1
Zig-Zag	13	1	0
Zig-Zag	14	0	1
Stack	16	--	--
Sleepy Keeper Approach	18	1	0
Sleepy Keeper Approach	19	0	1
Sleepy Stack	21	1	0
Zig-Zag Sleepy Keeper	23	0	1
Zig-Zag Sleepy Keeper	24	1	0

CONCLUSION

This paper gives the power optimization techniques to design VLSI circuits with all approximate ideal parameters like area, delay by miniaturization technique which can be used in the electronic industry. In this paper, all eight techniques are studied using VLSI designing tool TannerEDA 11.2 tool by simulating their circuits and plotting their waveforms at various inputs and comparing each other depending on their operation and their characteristics. Techniques can be used by the circuit designer depending on the need of the circuit.

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