A Novel Differential Switching Capacitor DAC for 10-bit SAR ADC

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Abstract: An Analog to Digital Converter (ADC) is a circuit which converts analog voltage signal into digital signal form. Practically most of the data is characterized using analog signals but the input to different processors cannot be an analog signal hence it needs to be converted into digital signals, so that processors will be able to read, understand and manipulate the data. The basic process in conversion involves sampling and quantization of the input signal. The continuous time domain analog signal is converted to a signal discrete in amplitude and time. In this paper we propose a novel architecture for Digital-to-Analog converter for the purpose of implementation on successive approximation register type Analog-to-Digital converter. Compared to conventional converters the differential switching enhances the resolution time, efficiency and area. The architecture implemented on 45nm reduces the capacitor and hence enhancing both timing and area of the circuit.

Index Terms **- Differential Switching Capacitor, Digital-to-Analog, SAR-ADC**

I. INTRODUCTION

Successive approximation Register Analog-to-Digital converters being the most recurrently and extensively used type of ADC in low power integrated circuits, with the exhaustively progressing technology and shrinking die area, it's an ever challenging job for design community to get the best performance, efficiency and speed while keeping the assurance of reliability intact even at the smallest tech nodes. Any and every electronic system is constituted of Analog signals and digital signal, data capture into the system and out of the system is analog in nature, while the processing of data and logical implementation of system is digital. Every data captured hence has basic requirement of sampling and quantization to a digital logic levels, faster that happens with reliability faster and more efficient would the response of the whole system would be. Hence ADC being a simple and welcoming block for a system is still at the utmost importance for the whole system performance.

In this paper we propose a novel architecture for Digital-to-Analog converters in successive approximation register (SAR) type Analog-to-Digital converters. This architecture reduces the capacitance required by utilizing charging path capacitance and as well widening the charging path in a binary weighted format. By utilizing the differential architecture this method also achieves a good enhancement as: (i) Increase the input range [−Vref, Vref] (ii) Good common mode rejection ratio and (iii) Canceling of even order harmonics.

In the next section 2 we would discuss on the background idea on ADC's and a brief note on SAR ADC types and enhancements and improvisation brought with age, Section 3 is solely dedicated on the proposed differential CAP-DAC ADC.

II. BACKGROUND DETAILS

Based on speed, Performance, dynamic range, different applications along with their interfaces and degrees of accuracy ADC's are classified into various types based on Nyquist rate and oversampling mechanism. The most common types of ADCs are, Flash type ADC, Pipeline ADC, SAR ADC and Sigma Delta ADC etc. An ADC samples an analog signal at uniform time intervals and assigns a digital value to each sample. The digital value appears on the converter's output in a binary coded format. The value is obtained by dividing the sampled analog input voltage by the reference voltage and them multiplying by the number of digital codes. The resolution of converter is set by the number of binary bits in the output code.

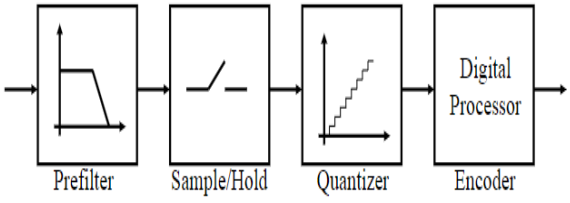

Figure 1 Working Principle of ADC

The above fig.1 shows the basic block diagram of Analog to digital converter. The above figure consists of pre-filter, Sample/hold circuit, quantizer and encoder block. The pre-filter block filters (removes) unwanted input frequencies from the analog signal

using binary search logic, then the filtered signal is sent to the sample/hold logic where the analog signal is sampled. Later the signal is quantized in quantizer block and finally the quantized signal is sent to encoder where the signal is processed in digital form and the digital output is obtained.

The representation of an analog signal in an ADC with an infinite resolution is converted and represented in the form of digital code with finite resolution [8]. The ADC produces 2N digital values where N represents the number of binary output bits. The analog input signal will fall between the quantization levels because the converter has finite resolution resulting in uncertainty or quantization error. That error determines the maximum dynamic range of the converter. The sampling process represents a continuous time domain signal with values measured at discrete and uniform time intervals [1]. This process determines the maximum bandwidth of the sampled signal in accordance with the Nyquist Theory. Nyquist theory states that the signal frequency must be less than or equal to one half the sampling frequency to prevent aliasing. Quantization process is representation of an analog signal having infinite resolution with a digital signal having finite resolution. It assigns binary code to sampled and hold value, range and granularity. This process even helps to achieve maximum dynamic range. This process of quantization encounters quantization error or quantization noise.

The two main performance metrics considered in this conversion are static (DC specification) and dynamic (AC specification). These are further classified as static- monotonicity, offset error, gain error, differential non-linearity (DNL), Integral non-linearity (INL) and dynamic- Delay setting time, signal to noise ratio (SNR). Signal to noise + distortion ratio (SNDR), spurious-free dynamic range (SFDR).Each of the above parameters are explained in detail. Monotonicity in an ADC is that if the input in analog form and output in digital form either increase or decrease or stay in the same state. Non-monotonic behavior of ADC results in oscillations [2].Offset error is defined as the deviation from the code transition points which is present across various output codes [2].This function either shifts the entire code towards right or towards left. Gain error is defined as the deviation from the ideal slope of ADC transfer function curve [4]. This is determined by the location of last transition code and then comparing with the ideal case. DNL it is defined as the difference between the actual increment height of transition n and the ideal increment height. INL at any point is defined as the difference between the output values for input code n to the output value of the reference line at that point [7].

Delay setting time is defined as the time taken by an output to reach the final value with desired accuracy in application of a step input. SNR is defined as the ratio of signal power to that of the noise power [7]. Theoretically the maximum SNR of an ADC is given as

SNR = 6.02 N + 1.76 (dB) -- (1)

where N is the resolution of the converter.

SFDR is defined as the ratio of signal power to that of the largest magnitude of any spectral component. A spectral component can be a harmonic of an input signal.

$$SFDR = \frac{P_S}{\max(P_{spectrum}(f))},\ f \in \{1,\ldots., Fs/2\}\backslash\{fin\} \quad --(2)$$

$P_{spectrum}(f)$ is the spectral component excluding the DC Component.

SNDR is a parameter which completely indicates overall dynamic performance of the converter. This is completely a combination of various performance degradation elements.

$$SNDR = \frac{P_S}{\sum_{i=2}^{h} P_H(i) + P_j + P_{q+DNL} + P_{th}} = 10^{\frac{THD}{10}} + 10^{\frac{-SNR}{10}} \quad --(3)$$

P_j, P_{q+DNL}, P_H and P_{th} are the jitter, quantization plus DNL, harmonics and thermal noise power respectively.

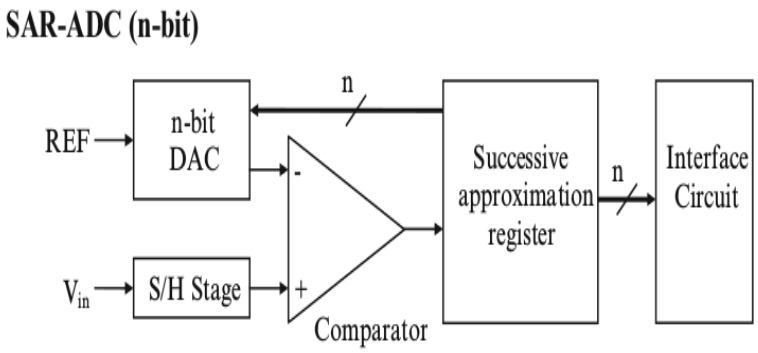

Figure 2 Conventional SAR ADC block level description

An advantage of SAR ADCs compared to other architectures is the compact design. Another common ADC type, the flash converter, performs simultaneous comparisons of the input voltage with (2^n-1) reference voltage levels, each requiring its own comparator. In contrast, the SAR ADC only needs a single comparator, trading increased conversion time for lower power consumption and chip area

Conventional SAR ADC (fig. 2) algorithm is as that shown in fig. 3. The first step of the successive approximation algorithm is determining the most significant bit (MSB). This is done by comparing the sampled input voltage V S&H to the voltage V DAC = 1 / 2 V F S corresponding to the digital code 10...00. If the input voltage exceeds this level the MSB value is set to 1 and vice versa. This procedure is repeated for determining the next bit with a V DAC of either 3 / 4 V F S or 1 / 4 V F S , corresponding to 11...00 and 01...0 respectively, depending on the value of the MSB. When all bits are determined at the end of the conversion cycle the digital output of the ADC is updated and a new conversion cycle begins.

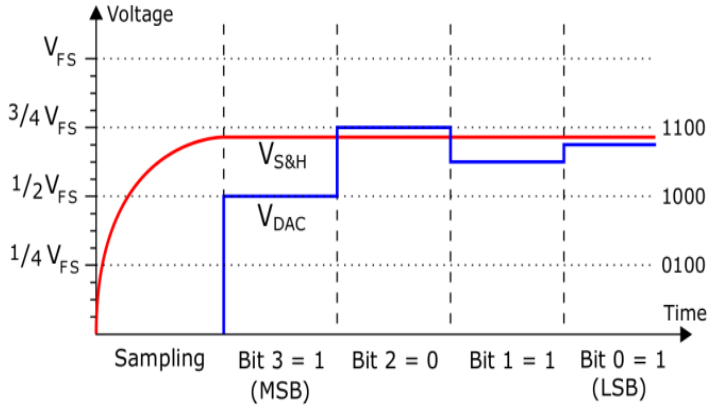

Figure 3 Binary search algorithm for SAR ADC

III. DIFFERENTIAL SWITCHING CAPACITOR

DAC

Advanced and improvised ADC have DAC implemented in Capacitive C-2C ladder logic or capacitive charge redistribution logic [12]-[16], With Capacitor being pulled in, the necessity for a sample and hold circuit is bypassed by the Capacitor array, and additionally can handhold the function of subtraction as well. An advantage of this implementation is that the DAC only consumes power during charging and discharging of the capacitive network. The SAR is a digital block which can be implemented in CMOS with good power efficiency resulting in low power consumption determined mainly by capacitor charging and power dissipated in the comparator. The common technique is to store the input as common mode voltage (Vcm) -Vin and compare with Vcm, if comparator output is high transition MSB is set 1 else 0, the bit to DAC is fed as switching it between gnd and Vref. This method is analogous to usual weight balance technique of keeping one hand constant at Vcm and trying to achieve balance by varying the other end.

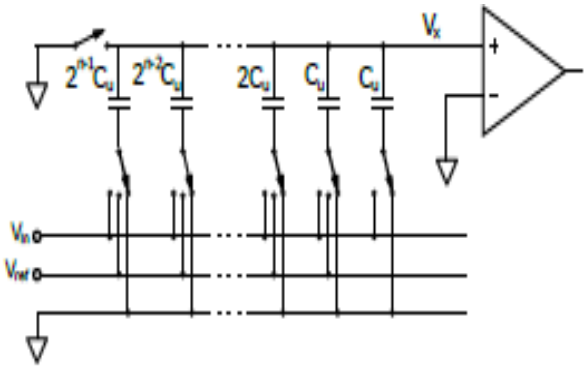

Figure 4 Conventional charge redistribution type DAC

In this paper we propose a differential Switching capacitor DAC, where both the arms of comparator have a capacitor array included, both being controlled to achieve balance equally. Significance of this paper comes at the point that all the capacitors used are of same capacitance as compared to the previous works, were either binary weighted or C-2C network is being used, to counter par for the capacitance values the charging path on switching have been made wide in a binary weighted manner with a coupling capacitor too added in the midway of array. By using a differential implementation we are also able to increase the input range [−V ref, V ref]. This is achieved by using an additional pair of reference voltages, this increase in maximum signal power can attribute to making the influence of noise less critical. Importantly a differential architecture makes great achievement in common mode rejection and hence rejection of discrepancies common to both the nodes. And also contribute to suppression of even-order harmonics.

In this proposed method, both the arms of comparator has an array of capacitor DAC, the capacitors are initially charged to Vcm-(+Vin) and Vcm-(-Vin) values respectively, the array has additional branch of capacitor on both the arms whose bottom plates are connected to Vrefp and Vrefn for p and n comparator nodes respectively, hence there is always a imbalance on the arms while sampling, when loaded if Vin >Vcm the p arm weights greater or if Vin<Vcm n arm would weight more, accordingly the MSB be would be set to 0 or 1. And the bit fed DAC would do switching of Capacitor bottom plate to Vrefp or Vrefn the function would be complementary on both the arms, Say if bit is 0 the nth arm will switch to Vrefp while the corresponding switch in p^{th} arm would switch to Vrefn. Figures 5 to 8 presents the circuit diagram for a 3-bit logic of the same.

Sample	Bit	P-arm	N-arm
0	0	Vrefn	Vrefp
0	1	Vrefp	Vrefn
1	X	Vin	Vin

Switching Logic

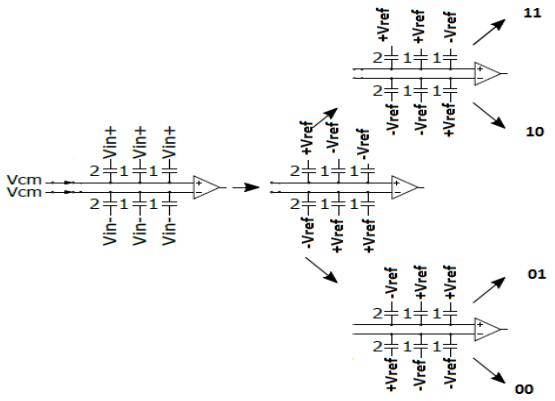

Figure 5 Proposed algorithm demonstrated for 2-Bits

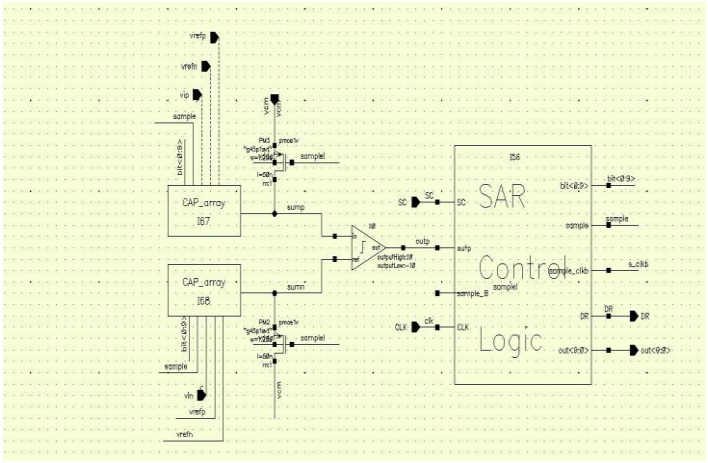

Figure 6: Top Level Circuit for differential CAP-DAC SAR ADC

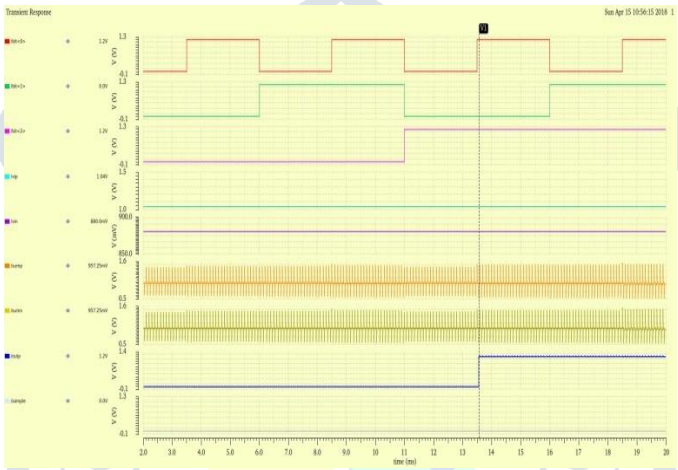

Figure 7 Data Capturing for the proposed DAC for 3-bit realization (operating 0.72v-1.2v) detecting binary 101 for application of 1040mv

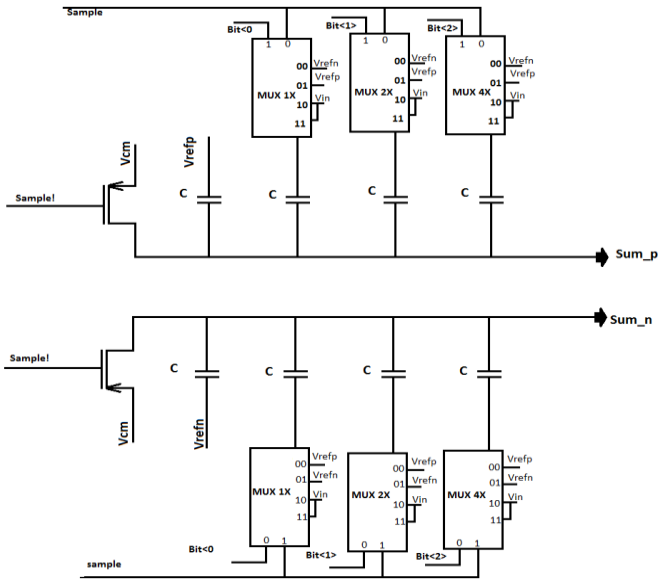

Figure 8: Proposed CAP-DAC architecture for 3-Bit

IV. CONCLUSION

This proposed DAC architecture presents a reliable and area and time efficient method for successive approximation logic ADC, and is able to achieve a bit rate of 50Ms/s and SINAD of 56.52 dB in 45nm technology a very near value to ideal one , the differential switching algorithm has very considerable hand in noise reduction. Using the mux logic has contributed to reliable reduction in area.

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