

Design and Implementation of 4x4 bit Multiplier using Dadda Algorithm

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ABSTRACT

Multiplier is one of the most important arithmetic modules in the fast computing applications. Multipliers and their associated circuits like half adders, full adders and accumulators consume a significant portion of most high speed applications. In order to reduce the hardware which ultimately reduces an area, power and propagation delay, efficient full adders are used in the multipliers. They also reduce the power and propagation delay of the multiplier. In this paper 4x4 multiplier is designed using Dadda algorithm and 10T full adder. Use of Dadda algorithm reduces 10.47% of the power dissipation, 27.67% of the propagation delay and 35.34% power delay product compared to Array multiplier. The simulations are performed using Tanner EDA of 45nm technology.

Keywords:

Multiplier, Full adder, Half Adder, Array, Wallace, Vedic, Dadda, Power dissipation, Propagation Delay, Power delay product.

1.INTRODUCTION

Multiplier plays an important role in digital signal processors and various other applications. More than 70% of instructions in microprocessors are performing addition and multiplication operations, so these operations are dominating the execution time of processor. There is a need of high speed multiplier to decrease the execution time of the processor and also in the VLSI design power dissipation, propagation delay and area are the important parameters which should be taken into consideration. In the design of multiplier more number of full adder blocks is used. Decrease of power consumption and propagation delay in the full adder can decrease the total power consumption and propagation delay of the multiplier. So here low power and high speed multiplier is implemented using Dadda algorithm and 10T full adder. Section-2 describes the Existing multipliers like Array, Wallace and Vedic multiplier. Section-3 describes the proposed multiplier which is Dadda multiplier. Section-4 contains the results and discussions. Section-5 concludes the paper.

2. Existing Multipliers:

2.1 Array Multiplier:

It is the conventional Multiplier. It uses the same steps as used in the normal multiplication. It is based on shift and add algorithm. 4x4 multiplier uses 16 AND gates, 4 half adders, 8 full adders and 12 total adders are used [2]. In Fig.1 a0, a1, a2 and a3 are bits in the multiplicand and b0, b1, b2 and b3 are the bits in multiplier. P0, p1, p2, p3, p4, p5, p6 and p7 are the output bits. Where HA is the half adder and FA is the full adder.

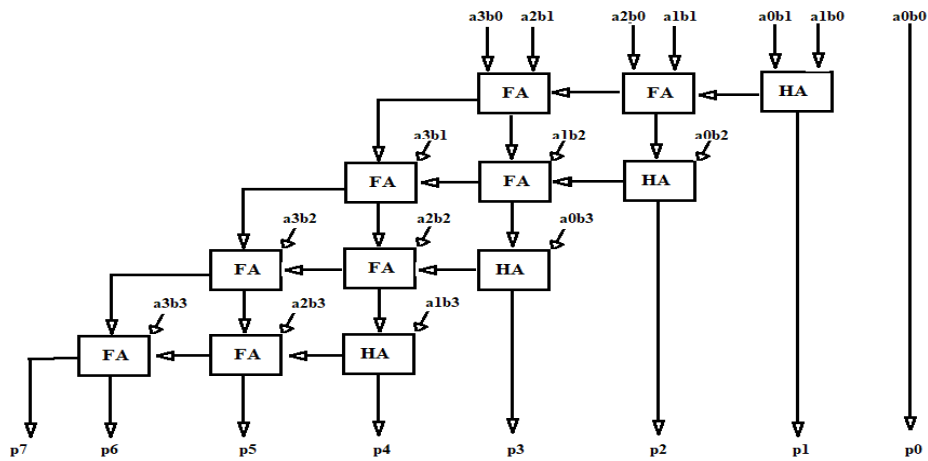


Fig.1 4x4 Array Multiplier

It has a regular structure. It is easy for implementation, but it consumes more power. Use of large number of digital gates resulted in large chip area. For further reduction of power dissipation and propagation delay, different multipliers are designed based on the different algorithms.

2.2 Wallace Multiplier

Every Multiplication algorithm consists of three stages. They are i) Generation of partial products ii) Reduction of partial products iii) Addition of partial products. Generation of partial products is same in every algorithm. In the reduction process, use full adders wherever the three elements are present. And use half adders wherever the two elements are there. Generated sum and carry bits from the half and full adders will be passed to the next stage. Pass the left over elements to the next stage. Repeat this process until getting the two rows [1][6]. Figure.3 shows the dot diagram of Wallace multiplier. Finally add last two rows to get the output [3]. In Fig.2 p0, p1, p2, p3, p4, p5, p6 and p7 are output bits.

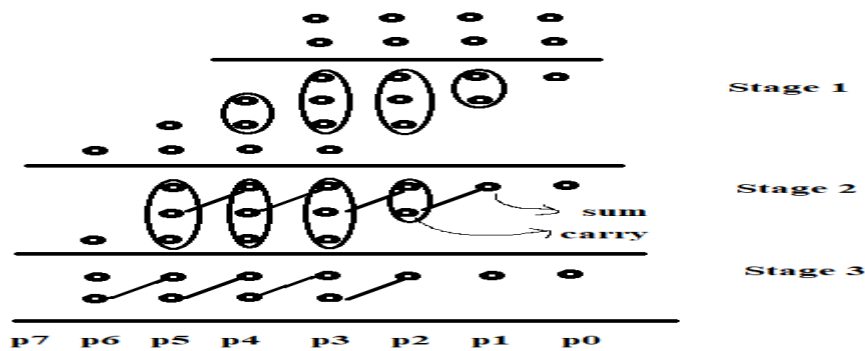


Fig.2 4x4 Wallace algorithm dot diagram [1]

2.3 Vedic Multiplier:

It is based on the vertically and crosswise method. Consider two numbers $A=A_3A_2A_1A_0$ and $B=B_3B_2B_1B_0$. $A_3, A_2, A_1, A_0, B_3, B_2, B_1$ and B_0 are the bits in the number. Multiply A_0 and B_0 and the result is sum s_0 . In the step2, multiply A_0 and B_1 and add the result to the product of A_1 and B_0 . The result obtained is s_1 and the carry is c_1 . In this manner multiply and add the bits as shown in Fig.3 for remaining steps. Here carry generated from one step will be added to the sum in the next step [7].

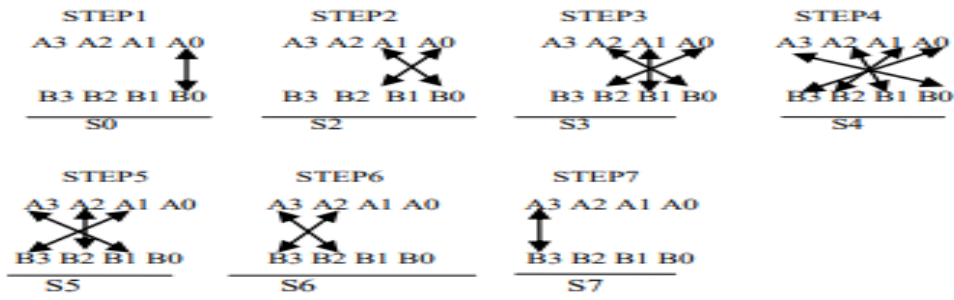


Figure.3 4x4 Vedic Multiplier

Step1: $S_0 = A_0B_0$

Step2: $S_1 = A_1B_0 + A_0B_1$; sum= S_1 , carry= C_1 ;

Step3: $S_2 = A_2B_0 + A_1B_1 + A_0B_2 + C_1$; sum= S_2 , carry= C_2 ;

Step4: $S_3 = A_3B_0 + A_0B_3 + A_2B_1 + A_1B_2 + C_2$; sum= S_3 , carry= C_3 ;

Step5: $S_4 = A_3B_1 + A_1B_3 + A_2B_2 + C_3$; sum= S_4 , carry= C_4 ;

Step6: $S_5 = A_3B_2 + A_2B_3 + C_4$; sum= S_5 , carry= C_5 ;

Step7: $S_6 = A_3B_3 + C_5$; sum= S_6 , carry= C_6 ;

Final Output= $C_6S_6S_5S_4S_3S_2S_1S_0$.

Here in this multiplier 4 full adders and three half adders are used. It is more efficient than Array and Wallace multipliers in terms of power and propagation delay. The disadvantage of this multiplier is that the system becomes complex for complex numbers.

3. Proposed Multiplier

3.1 Dadda Multiplier:

Array multiplier has more power consumption and propagation delay compared to other multipliers. Wallace multiplier has large area wastage problem due to irregularity in the structure. Vedic multiplier system becomes complex for complex numbers. To overcome these disadvantages in the existing multipliers Dadda multiplier is proposed.

Dadda multiplier is a fast parallel multiplier presented by Luigi Dadda in 1965. It is a refinement of Wallace multiplier so its algorithm also has three general stages. The procedure of the three stages is same for Dadda multiplier as in Wallace multiplier. But in Dadda multiplier, the row reduction processed by placing adders at maximum heights of matrix in optimal manner. Thus it requires less adders compared to Wallace multiplier.

Reduction process is controlled by d_j value. Where d_j is the maximum height of the sequence, $d_j=2$ then $d_{j+1}=\text{floor}(1.5d_j)$. The sequence is $d_1=2, d_2=3, d_3=4, d_4=6, d_5=9, d_6=13, \dots$. The initial value of d_j is chosen as the largest value such that $d_j < \min(m, n)$. Where m and n are the input bits in the input multiplicand and multiplier. If height (C_i) $\leq d_j$ then that column does not require reduction, move to next column. If height of $C_i = d_{j+1}$ add top two elements in a half adder, place the result at the bottom of the column and carry at the top of column C_{i+1} , then move to column C_{i+1} . Else add top three elements in a full adder, place the result at the bottom of the column and carry at the top of the column C_{i+1} , restart C_i at step1.

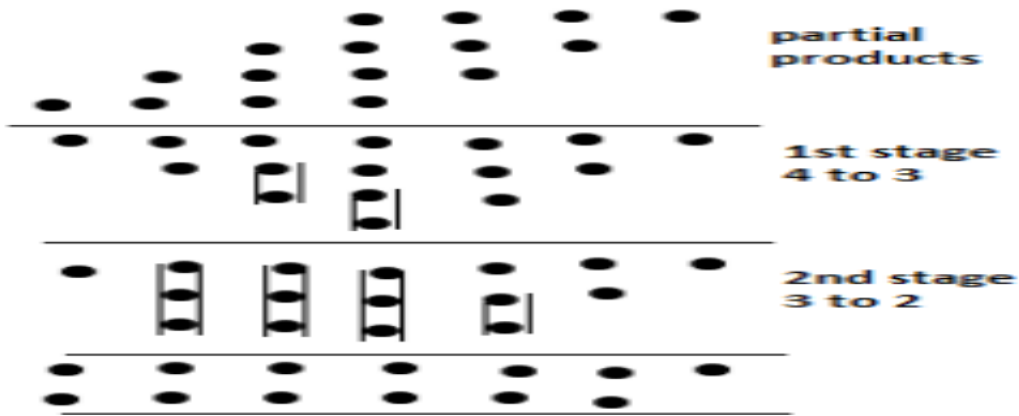


Fig.4 4x4 Dadda algorithm dot diagram

4x4 bit Dadda multiplier algorithm process is shown in Fig.4. The number of full and half adders needed for Dadda multiplier is depend on size of the operands, determined by the following equations [5].

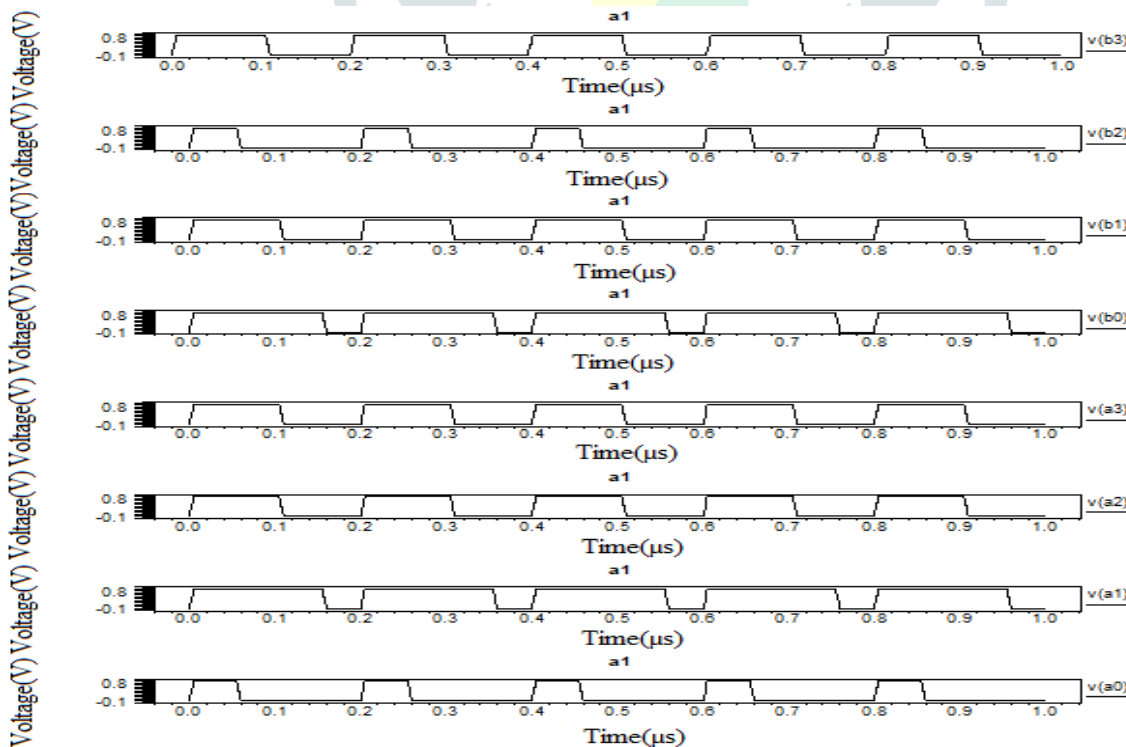
$$\text{Number of Full adders required} = 3$$

$$\text{Number of half adders required} = 3$$

Thus the Dadda multiplier requires less number of adders compared to all other multipliers. Hence area of multiplier is reduced .The power dissipation is reduced and speed is also reduced, because of reduction of partial products which is necessary at each level.

4. Simulation Results of Existing and Proposed Multipliers

Simulations are performed using Tanner EDA tool. The inputs to the multiplier are $A=a_3a_2a_1a_0$ and $B=b_3b_2b_1b_0$. The simulation waveforms analyzed for different multiplier circuits with the inputs $a_0=1000$, $a_1=1110$, $a_2=1100$, $a_3=1100$ and $b_0=1110$, $b_1=1100$, $b_2=1000$ and $b_3=1100$.The results are shown in figures.



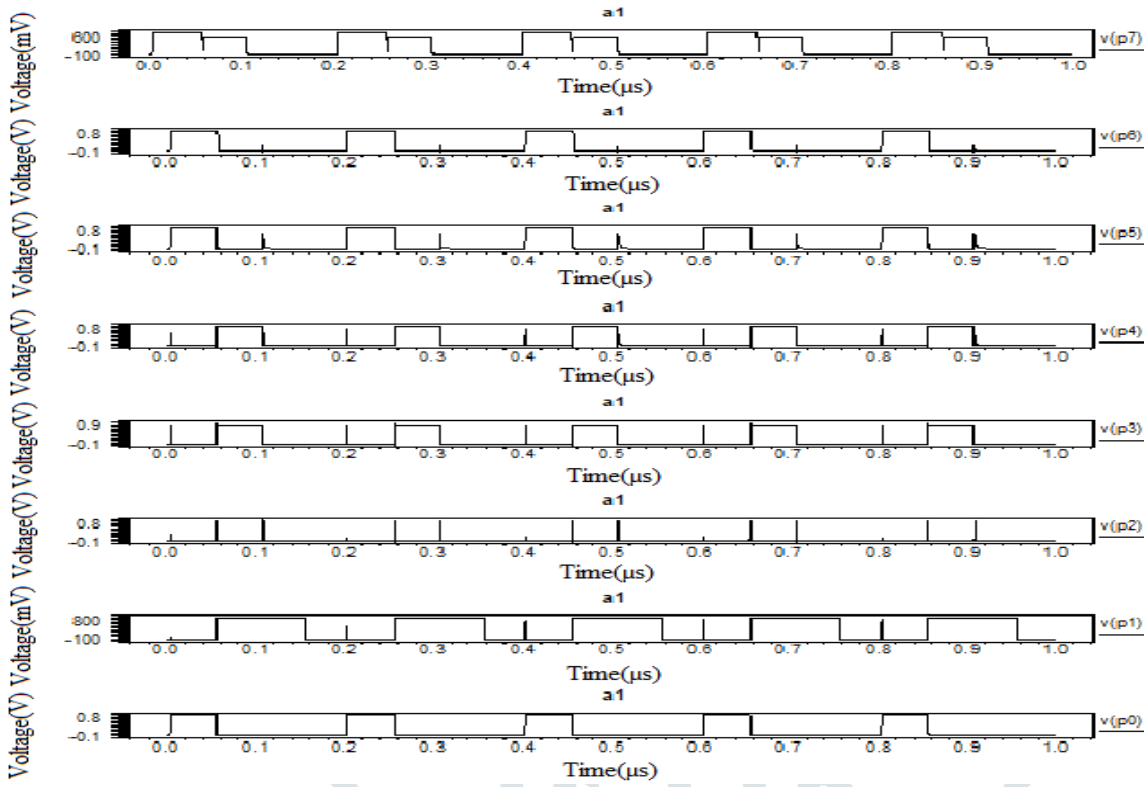
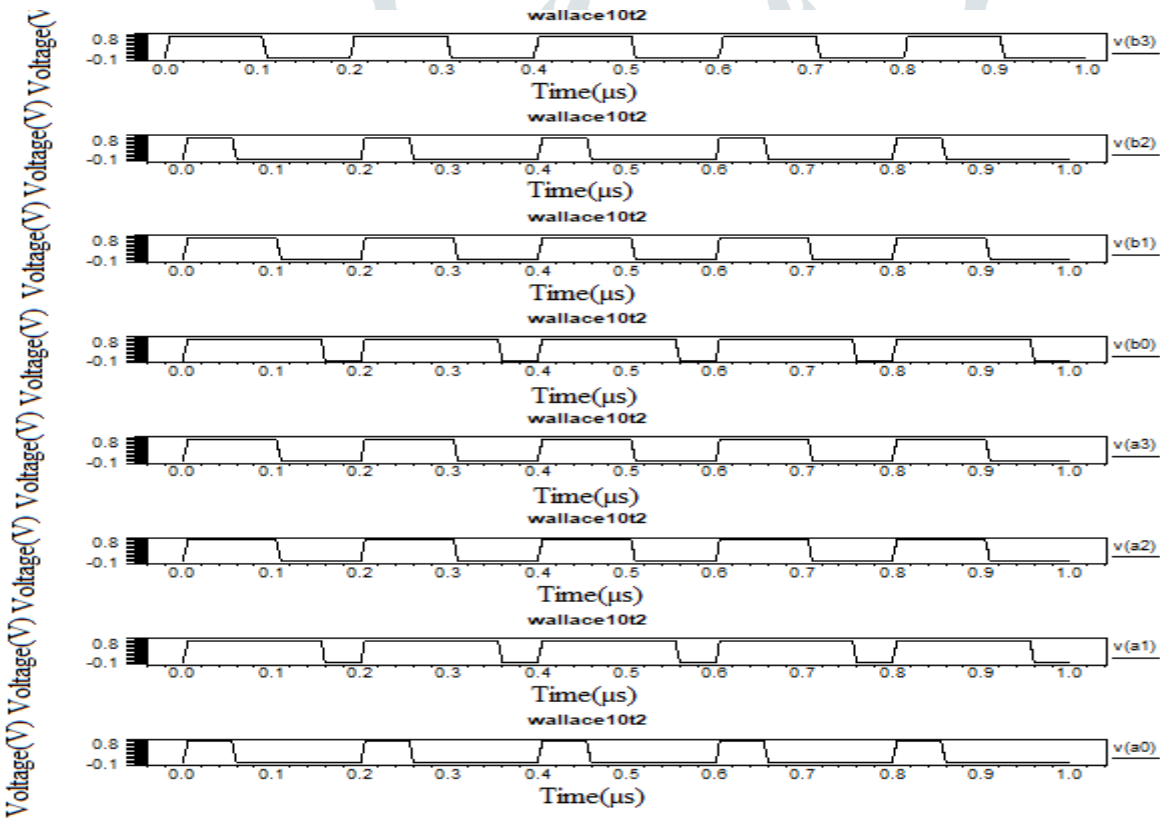


Fig.5 Simulated waveforms of 4x4 Array multiplier



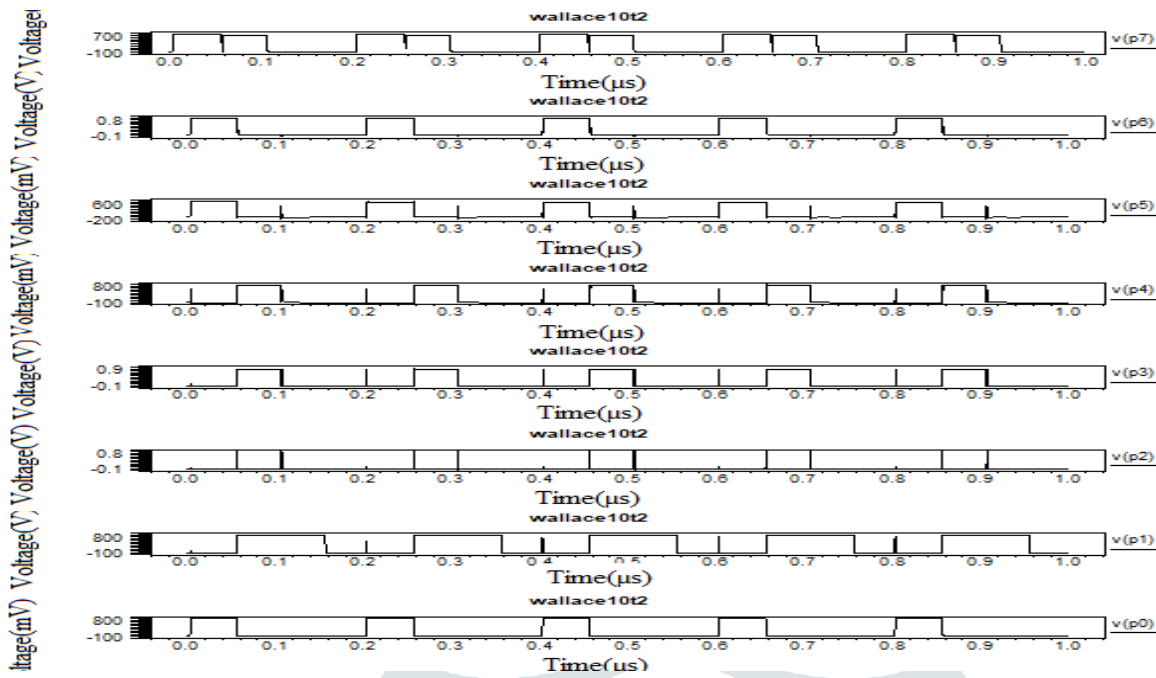
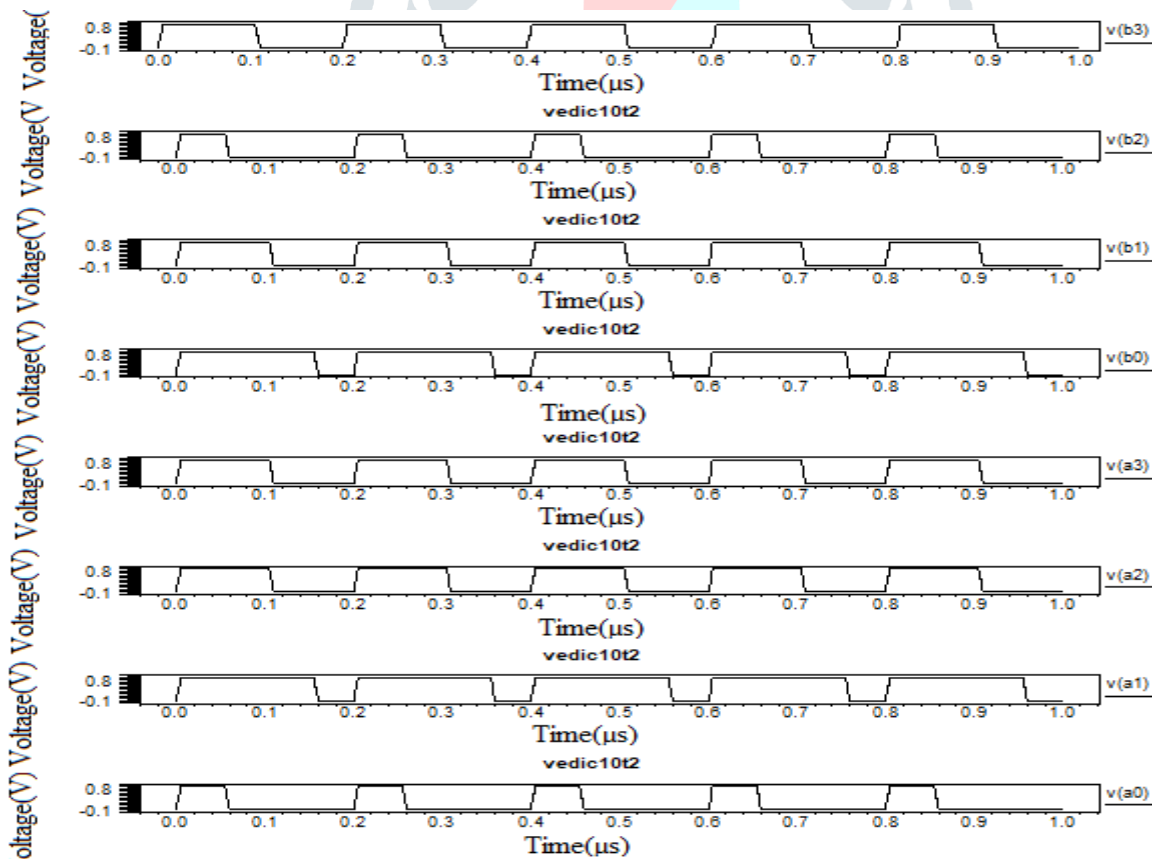
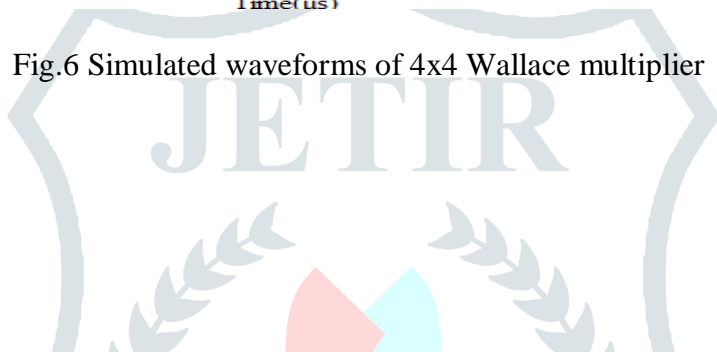


Fig.6 Simulated waveforms of 4x4 Wallace multiplier



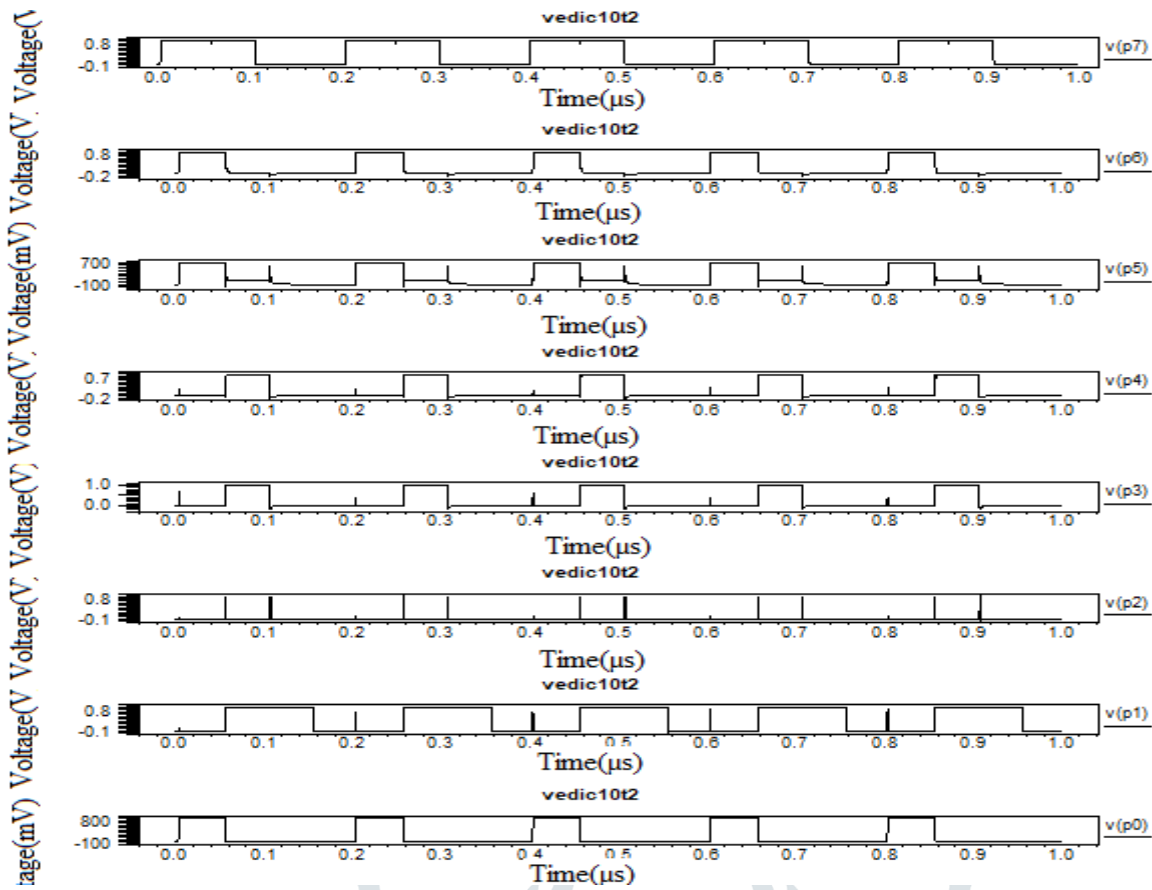
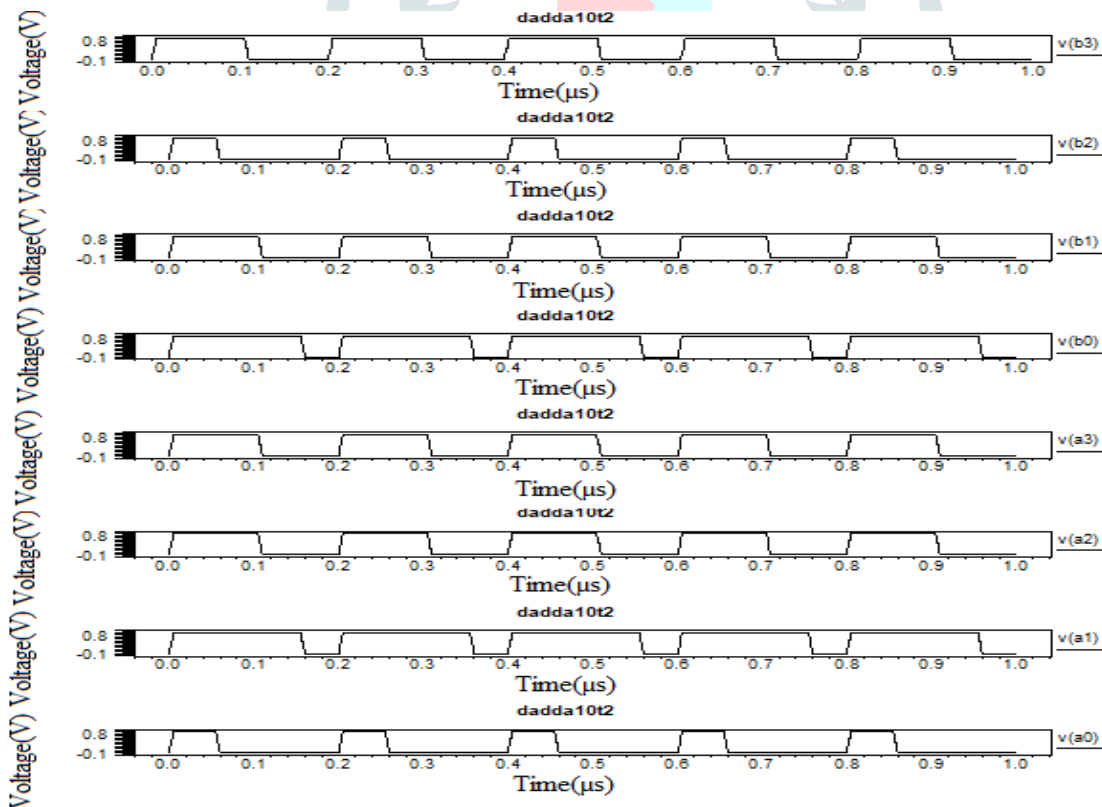


Fig.7 Simulated waveforms of 4x4 Vedic multiplier



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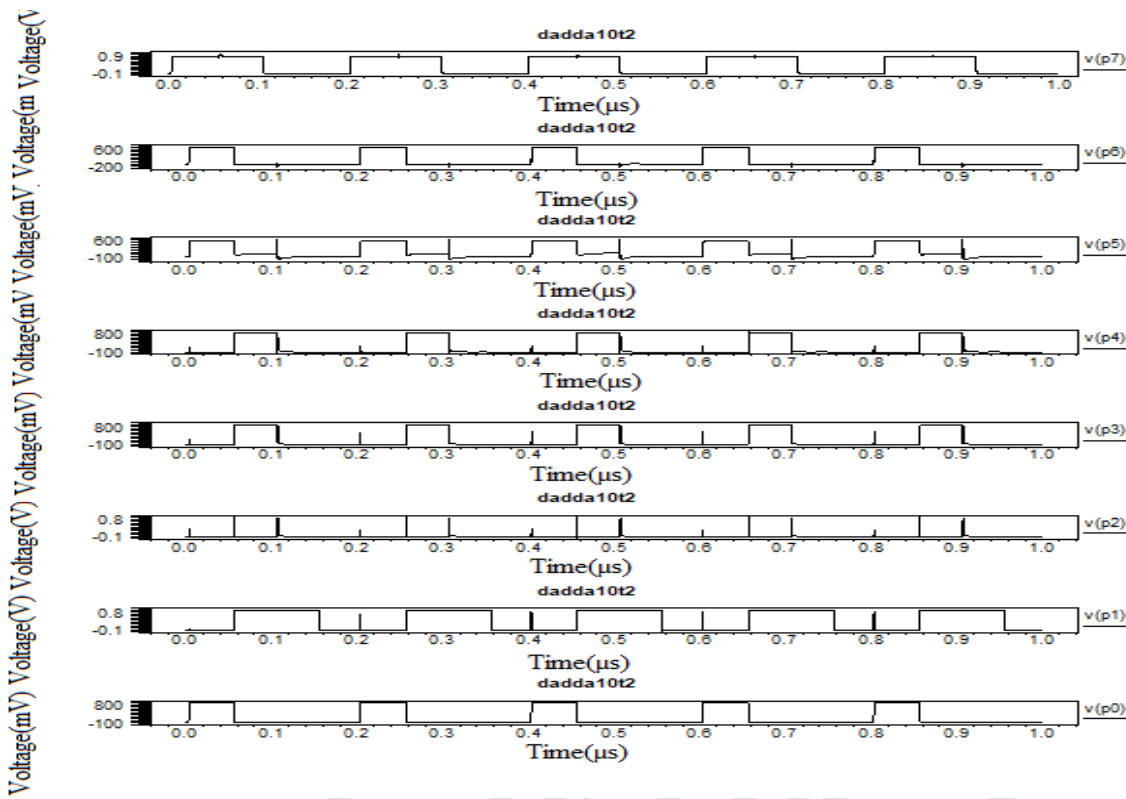


Fig.9 Simulated waveforms of 4x4 Dadda multiplier

From the results, all the multipliers are functioning properly at 45nm technology with $V_{dd}=1V$. The power, propagation delay and power delay product are observed for different 4x4 multipliers and the results are tabulated.

Simulation results of existing and proposed multipliers:

4x4 multiplier	Power(μw)	Propagation Delay(μs)	Power delay product(pJ)
Array	39.4	2.1	0.843
Wallace	37.7	1.8	0.692
Vedic	35.3	1.7	0.615
Dadda	35.3	1.6	0.545

Result Analysis:

Array multiplier has more power consumption and propagation delay compared to all other 4x4 multipliers like Wallace, Vedic and Dadda multipliers. Because more number of full adders is used in the Array multiplier compared to other multipliers. Carry generated from one adder is the input to the other adder. In the generation of output bit of p7, it has to travel from the first half adder in the first stage to final stage. So the propagation delay is more in this multiplier. Here more number of digital gates is used so the power consumption and chip area are more. Every adder has partial product inputs, sum and carry inputs and two outputs. So it has regular structure.

Wallace multiplier has simple carry propagate adder compared to other multipliers but Wallace multiplier is less regular than Array multiplier. Because of the less regularity it is suffering from the large area wastage.

Vedic multiplier performs the fast multiplication. But as the number of bits increases, system becomes complex. Carry propagate adder used in the Vedic multiplier is high compared to Wallace multiplier and power consumption and propagation delay are less compared to Array and Wallace multipliers.

Multipliers vary depending on the partial product reduction algorithms used in the multiplier designs. The purpose of algorithms used in the digital design is the reduction of hardware. Dadda multiplier uses 3 full adders, Vedic multiplier uses 4 full

adders and Wallace multiplier uses 3 full adders, so number of full adders used in the Dadda multiplier is less compared to other multipliers and number of half adders used in the Dadda multiplier also less so the power consumption of Dadda multiplier is less.

5. Conclusions and Future Scope

Proposed Dadda multiplier has low power consumption and low propagation delay compared to existing multipliers where as Array multiplier has more power consumption, propagation delay and power delay product. Dadda multiplier has achieved 10.47% reduction in power dissipation, 27.67% reduction in propagation delay and 35.34% power delay product compared to Array multiplier.

These multiplier designs can be implemented for 8x8 multipliers. Every multiplier has its own advantages and disadvantages using hybrid techniques new multiplier design can be implemented. Dadda multiplier has the complex carry propagate adder at the final stage whereas the Wallace multiplier has less complex carry propagate adder. By combining these two algorithms new hybrid multiplier can be designed.

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