Reliable Multiplier Design Implementation On FPGA with Adaptive Hold Logic

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Abstract—Digital multipliers are among the most critical arithmetic functional units. The overall performance of these systems depends on the throughput of the multiplier. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias (Vgs = −Vdd), increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Therefore, it is important to design reliable high-performance multipliers. In this paper, we propose an aging-aware multiplier design with novel adaptive hold logic (AHL) circuit. Moreover, the proposed architecture can be applied to a column- or row-bypassing multiplier. The experimental results show that our proposed architecture with 16 ×16 column-bypassing multipliers or with 16 × 16 row-bypassing multipliers.

In Proposed System an aging-aware reliable multiplier design is inserted with a novel adaptive hold logic (AHL) circuit. The multiplier is based on the variable-latency technique. The AHL circuit is to achieve reliable operation under the influence of NBTI and PBTI effects. This architecture can be applied to fourier transform, discrete cosine transforms and digital filtering. The adaptive hold logic (AHL) can be implemented in FPGA Spartan 3/ Spartan 3AN and is simulated in ModelSim6.4c and Xilinx 9.1/13.2 software using Verilog HDL (VHDL). It has an advantage of minimizing the performance degradation and reducing the delay produced in the multiplier. For future enhancement, a RS-Encoder based design can be introduced in the multiplier.

Keywords – NBTI, PBTI, Adaptive Hold Logic, Verilog HDL, FPGA

I. INTRODUCTION

Typical DSP applications such as fourier transform, discrete cosine transforms and digital filtering, where multipliers play an important role. Multipliers are complex circuits and it operates at a high clock rate. So to obtain a satisfactory performance the delay of the multiplier should be minimum. The reliability degradation of the circuit is a critical issue in nanometer technologies. One of the main reason for performance degradation in nanoscale circuits is Bias Temperature Instability (BTI). PMOS transistors operating with negative gate to source voltage face Negative Bias Temperature Instability (NBTI) [4]. Due to this effect, threshold voltage V_{th} increases with time. So the performance of the system reduces over time. The similar effect in NMOS transistor is Positive Bias Temperature Instability (PBTI). These effects may cause timing violations in multiplier with time and it affects the whole system. Hence, a reliable multiplier design is essential to obtain satisfactory performance. For the proper performance of the system, critical path delay is used as system clock cycle in traditional circuits and it may cause significant timing wastage. The timing wastage in traditional circuits can be minimized by incorporating variable latency design in the system. In variable latency design, the circuit contains two paths: a shorter path and a longer path. Shorter path can execute the operation correctly in one cycle and longer path can execute the operation correctly in two cycles.

In this paper, a reliable variable latency multiplier design is proposed to reduce BTI effect. AHL circuit ensures proper performance by adjusting cycle periods. An ECPL circuit is used to detect timing violations.

Section II and III of this paper discusses with related work and the proposed method respectively. The analysis of results is discussed in Section IV and Section V contains the conclusion.

II. EXISTING METHOD

In the existing system, column/row bypass multiplier is used along with AHL circuit to reduce aging effect. Timing violations are detected using razor flip-flop before the arrival of next input pattern. Array multipliers are well known for its regular shape. Commonly used multiplication method is Add and shift algorithm.

Column bypass multiplier is a modified form of normal array multiplier. In array multiplier all the full adders are active irrespective of input. The working of column/row bypass multiplier depends on input number pattern. In column bypass multiplier if any bit of the multiplier is zero then the corresponding partial product will be zero. Therefore, it deactivates the corresponding column of adders and bypass the previous result to next stage. So it utilizes less power and provide high speed of operation as compared to array multiplier. Here, the bypassing operation is done using a multiplexer. The existing architecture consists of a column/row bypass multiplier along with AHL and razor flip-flops. The column bypass multipliers consume more area. The column/row bypass multipliers use large number of full adders, tristate buffers and multiplexers. So it results in high delay. A delayed output is obtained at the output of the razor flip flop.

In this paper, they propose a new circuit for timing error detection and correction. This approach is characterized by low cost, less power consumption and reduced design complexity with respect to earlier design schemes in the literature.

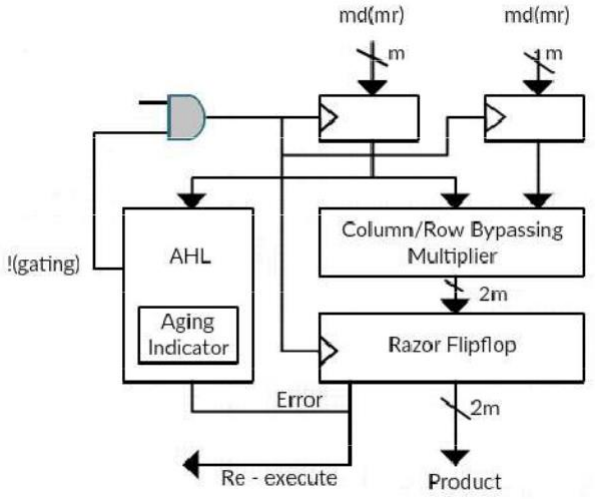

Fig. 1. Existing Architecture [1]

III. PROPOSED METHOD

The selection of proper multiplier for digital circuits is very critical. After comparing the results of array multiplier, column bypass multiplier, booth multiplier and vedic multiplier, it is observed that booth multiplier is most efficient. Modified Booth algorithm performs both addition and subtraction and treats both +ve and -ve operands uniformly. Fig. 2 shows the architecture of proposed circuit. It consists of three main blocks. A radix 4 booth multiplier, an ECPL circuit to detect timing violation and an AHL circuit to detect whether it is a one cycle or two cycle operation are the three main blocks.

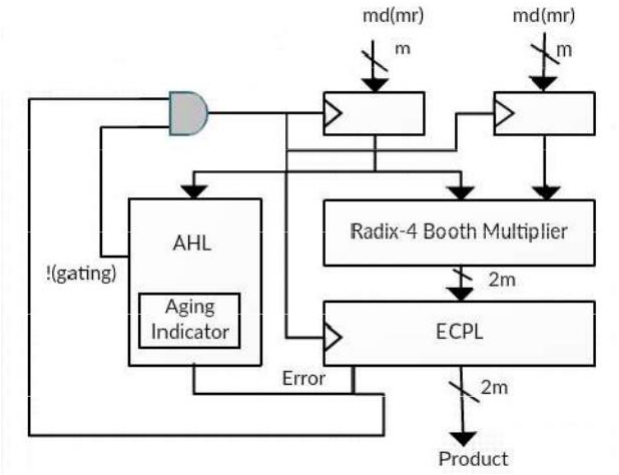

Fig. 2. Proposed architecture

A. Timing error detection and correction pulsed latch

A pulsed latch is a latch that is clocked by a brief pulse and it retains the qualities of both latch or flip-flop. The architecture of ECPL circuit is shown in fig. 3. A main latch PLM, a correction latch PLC and two XOR gates are used for the designing ECPL circuit. A pulsed clock signal drives the main latch whereas a delayed clock signal drives the correction latch. Asynchronous reset is used in PLC. The XOR gate 1will detect whether there is any error by comparing the input of PLM with the output of PLM. If there is a timing violation then the output of the XOR gate will be logic 1 otherwise, it is 0. XOR gate passes this result to correction latch. For the proper working of the circuit the PLC should be reset to zero initially. The PLC captures this comparison result using a delayed clock pulse. In the presence of timing violation Er-ror L signal moves to logic 1 and it is given to XOR gate 2.The XOR gate 2 correct the false value at the output of PLM by inverting the result. If there is no timing violation then the output of the Error L signal goes to logic zero and the XOR gate 2 passes the output signal F as it is.

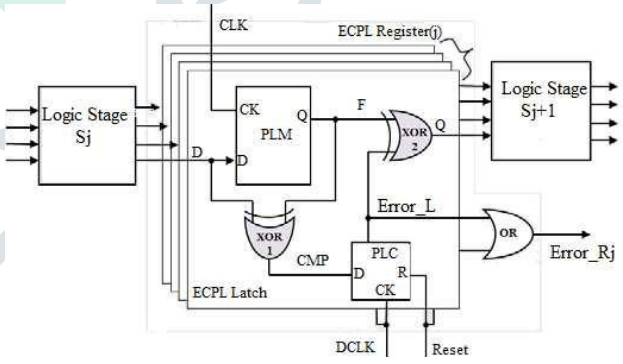

Fig. 3. Error Correction Pulsed Latch (ECPL) [3]

B. Adaptive Hold Logic

Clock period of the system is determined by the AHL circuit. Fig. 4 shows the illustration of AHL circuit. It consist of two judging block, one mux, one D flip-flop and an aging indicator. A counter is used as aging indicator. Shorter cycle period may cause timing violations whereas longer cycle period cause timing wastage. So depending on the input signal AHL circuit determines the cycle

period. In the beginning, chances of timing violation are negligible. Hence , a logic zero is obtained at the output of aging indicator and it will select the first judging block. If there is any timing violation due to aging then the ECPL will detect this timing violation and it is given to aging indicator. If error exceeds a predefined threshold, it means t he aging effect is significant and the aging indicator will sel ect the second judging block. In this case, the system will execute only smaller number of patterns in one cycle.

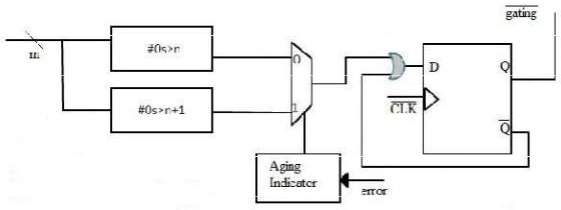

Fig. 4. Adaptive Hold Logic (AHL) [1]

If it is a one cycle pattern then the output of the multiplexer will be 1 and it is given to d flip-flop. Then the !(gating) signal will move to logic 1 and it direct the input flip-flops to latch new data in the next clock cycle. If the input signal is two cycle pattern then the output of the multiplexer will be 0. Then the !(gating) signal will move to logic 0 to disable the clock signal of the i nput flip-flop. Hence, the input flip-flops can not latch new data in the next clock cycle.

IV. RESULT AND ANALYSIS

The simulation results are obtained with the help of Xilinx ISE.

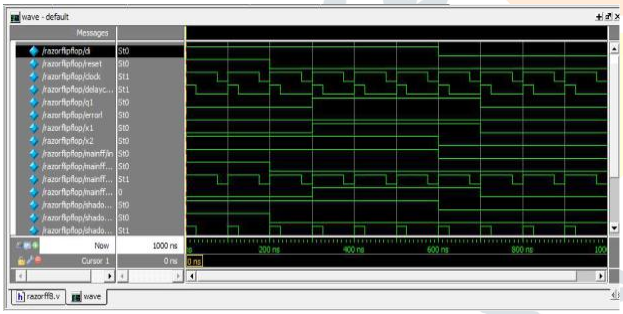

Fig.5. Razor FlipFlop 1-Bit

Razor flip-flop, Error Detection Correction (EDC) latch and ECPL are the three timing error tolerance circuits simulated in xilinx. Table I shows the comparison result of these circuits with respect to delay. From table I, it is found that ECPL has less delay. Simulation result of 8 bit ECPL circuit is shown in fig. 5.

Table II shows the comparison result of four m ultipliers with different bit size. Among the four multiplier d esign radix- 4 booth multiplier gives better performance. T he simulation results show that using booth multiplier delay and area can be reduced and it also shows that the average fano ut is less. The simulation result of existing 32 bit column by pass multiplier without error is shown in fig. 6 respectively. Multiple errors are injected by inserting an XOR gate before t he input of the PLM block in each ECPL latch. An error control signal is given to the input of the XOR gate whi ch can be controlled by an external. Simulation result of proposed multiplier with error is shown in fig. 8.

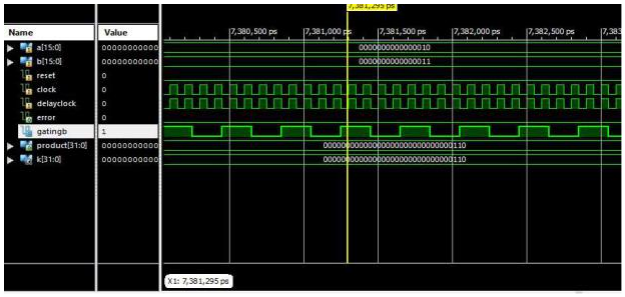

Fig.6. Column Bypass Technique

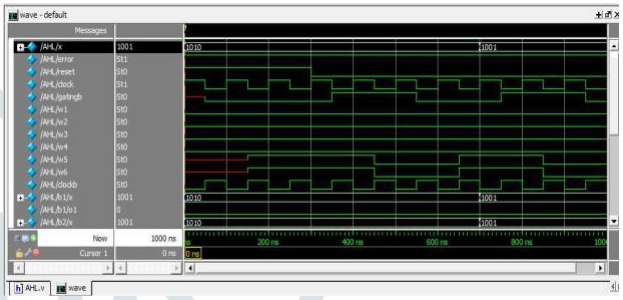

Fig.7. Adaptive Hold Logic

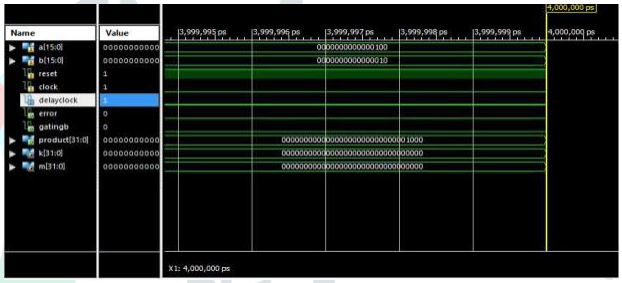

Fig.8. Proposed Booth Multiplication Technique

TABLE I COMPARISION OF DIFF ERENT MULTIPLIERS ON BASIS OF AREA

DESCRIPTION	AREA ANASLYSIS
COLUMN BYPASS TECHNIQUE	682 L UTs
BOOTH MULTIPLIER	390 L UTs
DADDA MULTIPLIER	340 L UTs
VEDIC MULTIPLIER	541 L UTs

TABLE II COMPARISION OF DIFF ERENT MULTIPLIERS ON BASIS OF TIMING REPORT

DESCRIPTION	TIMIN G REPOERT
COLUMN BYPASS TECHNIQUE	85.803 ns
BOOTH MULTIPLIER	25.26n s
DADDA MULTIPLIER	20.516 ns
VEDIC MULTIPLIER	1115.8 11ns

V. CONCLUSION

An aging aware multiplier is designed with AHL and ECPL circuit. The multiplier is successfully simulated using Xilinx ISE. By using ECPL circuit we can reduce the delay of the circuit and it ensure proper working of the multiplier. AHL circuit analyse the input pattern in each clock cycle and by selecting proper clock cycle it can avoid timing violations. Booth multiplier gives good performance as compared to other multipliers. The amount of area taken by the booth multiplier is less as compared to column/row bypass multiplier. Apart from this, it has less delay and maximum throughput.

VI. REFERENCES

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