

DESIGN AND ANALYSIS OF EFFICIENT PHASE LOCKED LOOP FOR FAST PHASE AND FREQUENCY ACQUISITION

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Abstract

The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high-performance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range. Hence there is a necessity of a PLL which must operate in the GHz range with less lock time. PLL is a mixed signal circuit as its architecture involves both digital and analog signal processing units. The present work focuses on the redesign of a PLL system using the 90 nm process technology (GPDK090 library) in CADENCE Virtuoso Analog Design Environment. Here a current starved ring oscillator has been considered for its superior performance in form of its low chip area, low power consumption and wide tuneable frequency range. The layout structure of the PLL is drawn in CADENCE VirtuosoXL Layout editor. Different types of simulations are carried out in the Spectre simulator. The pre and post layout simulation results of PLL are reported in this work. It is found that the designed PLL consumes 11.68mW power from a 1.8V D.C. supply and have a lock time 280.6 ns. As the voltage controlled oscillator (VCO) is the heart of the PLL, so the optimization of the VCO circuit is also carried out using the convex optimization technique. The results of the VCO designed using the convex optimization method is compared with traditional method.

I.INTRODUCTION

1.1 Overview:

Phase locked loop (PLL) [1-3] is the heart of the many modern electronics as well as communication system. Recently plenty of the researches have conducted on the design of phase locked loop (PLL) circuit and still research is going on this topic. Most of the researches have conducted to realize a higher lock range PLL with lesser lock time [4] and have tolerable phase noise. The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high-performance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction [5]. Phase locked loops find wide application in several modern applications mostly in advance communication and instrumentation systems. PLL being a mixed signal circuit involves design challenge at high frequency.

Since its inspection in early 1930s, where it was used in the synchronization of the horizontal and vertical scans of television, it has come to an advanced form of integrated circuit (IC). Today found uses in many other applications. The first PLL ICs were available around 1965; it was built using purely analog component. Recent advances in integrate circuit design techniques have led to the

development of high performance PLL which has become more economical and reliable. Now a whole PLL circuit can be integrated as a part of a larger circuit on a single chip.

There are mainly five blocks in a PLL. These are phase frequency detector (PFD), charge pump (CP), low pass loop filter (LPF), voltage controlled oscillator (VCO) and frequency divider. Presently almost all communication and electronics devices operate at a higher frequency, so for that purpose we need a faster locking PLL. So there are a lot of challenges in designing the mentioned different blocks of the PLL to operate at a higher frequency. And these challenges motivated me towards this research topic. In this work mainly the faster locking of the PLL is concentrated by properly choosing the circuit architectures and parameters. The optimization of the VCO circuit is also carried out in this work to get a better frequency precision.

1.2 PLL

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock CK_{ref} to produce a high-frequency clock CK_{out} this is known as clock synthesis.

A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

Types of PLL

There are mainly 4 types of PLL are available. They are

1. Linear PLL
2. Digital PLL
3. All Digital PLL
4. Soft PLL

The basic block diagram of the PLL is shown in the Figure 1.1. In general a PLL consists of five main blocks:

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divide by N Counter

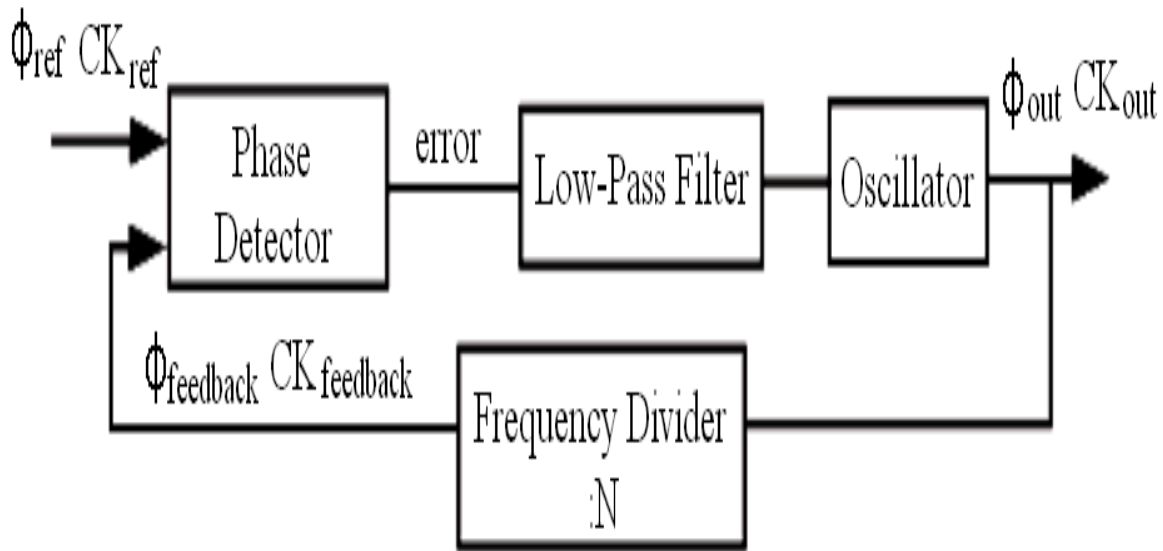


Figure1.1 Basic block diagram of a PLL

The “Phase frequency Detector” (PFD) is one of the main parts in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals “UP” and “DOWN”. The “Charge Pump” (CP) circuit is used in the PLL to combine both the outputs of the PFD and give a single output. The output of the CP circuit is fed to a “Low Pass Filter” (LPF) to generate a DC control voltage. The phase and frequency of the “Voltage Controlled Oscillator” (VCO) output depends on the generated DC control voltage. If the PFD generates an “UP” signal, the error voltage at the output of LPF increases which in turn increase the VCO output signal frequency. On the contrary, if a “DOWN” signal is generated, the VCO output signal frequency decreases. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, and then we can create closed loop frequency control system.

2.2 PLL Architecture

The architecture of a charge-pump PLL is shown in Figure 1.2. A PLL comprises of several components. They are (1) phase or phase frequency detector, (2) charge pump, (3) loop filter, (4) voltage-controlled oscillator, and (5) frequency divider. The functioning of each block is briefly explained below.

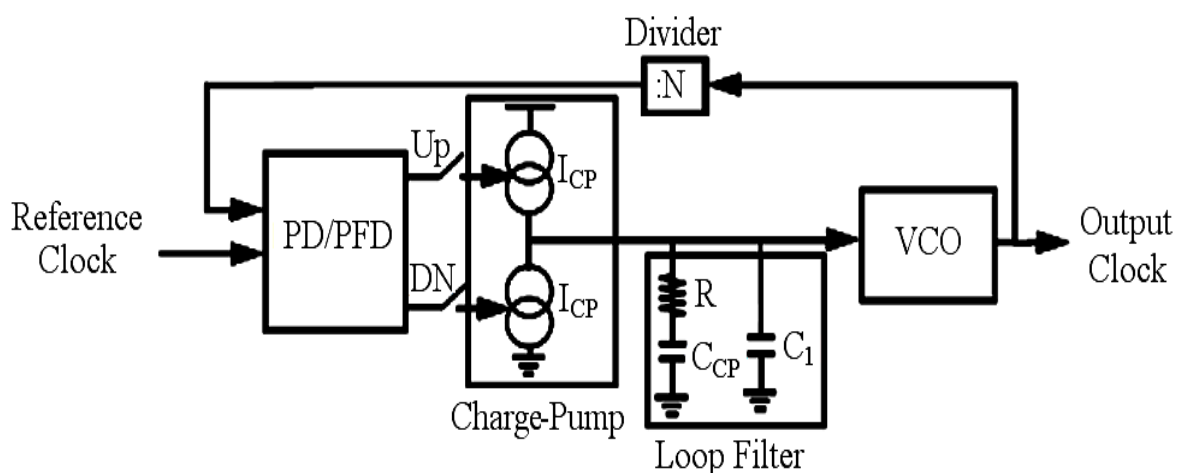


Figure1.2 Architecture of a PLL

2.2.1 Phase Frequency Detector

The “Phase frequency Detector” (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals “UP” and “DOWN”. Figure 1.3 shows traditional PFD circuit.

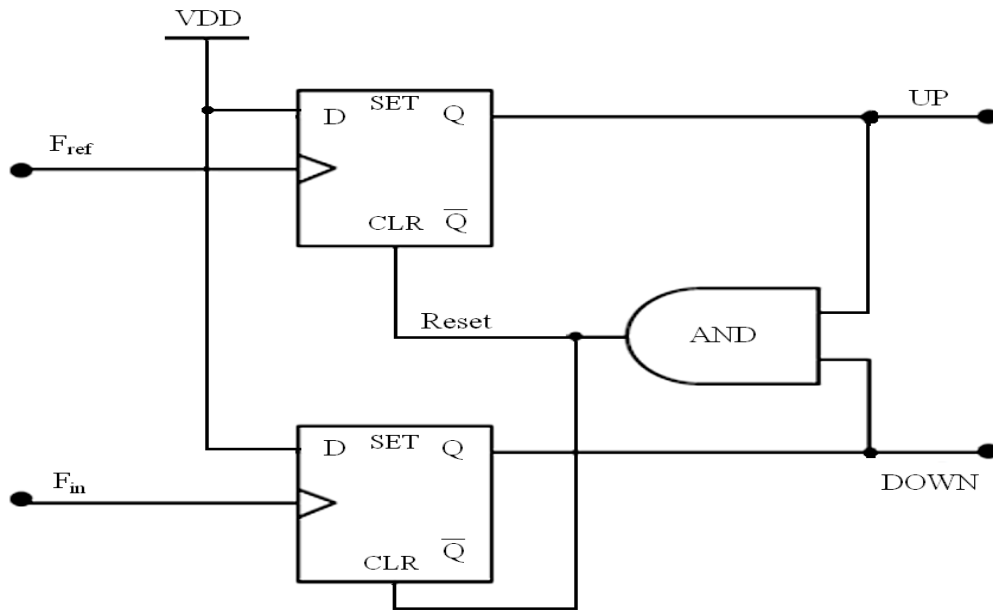


Figure1.3 Block diagram of a traditional PFD circuit

2.2.2 Charge Pump and Loop Filter

Charge pump circuit is an important block of the whole PLL system. It converts the phase or frequency difference information into a voltage, used to tune the VCO. Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. Charge pump circuit gives a constant current of value I_{PDI} which should be insensitive to the supply voltage variation [8].

The amplitude of the current always remains same but the polarity changes which depend on the value of the “UP” and “DOWN” signal. The schematic diagram of the charge pump circuit with loop filter is shown in the Figure 1.4.

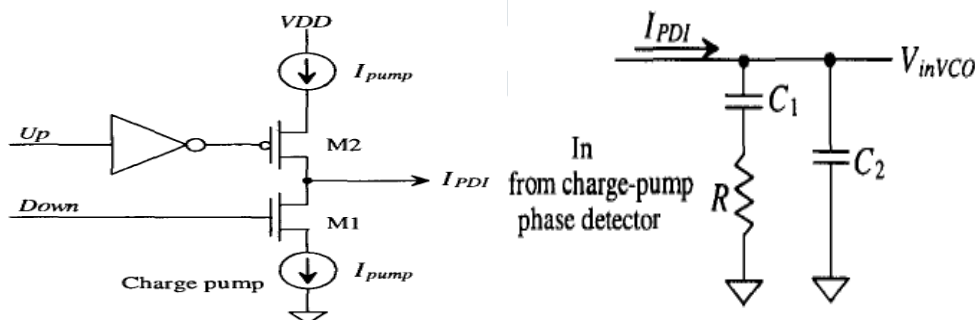


Figure1.4 Schematic diagram of the charge pump circuit with loop filter

2.2.3 Voltage Controlled Oscillator

An oscillator is an autonomous system which generates a periodic output without any input. The most popular type of the VCO circuit is the current starved voltage controlled oscillator (CSVCO). Here the number of inverter stages is fixed with 5. The simplified view of a single stage current starved oscillator is shown in the Figure 1.5.

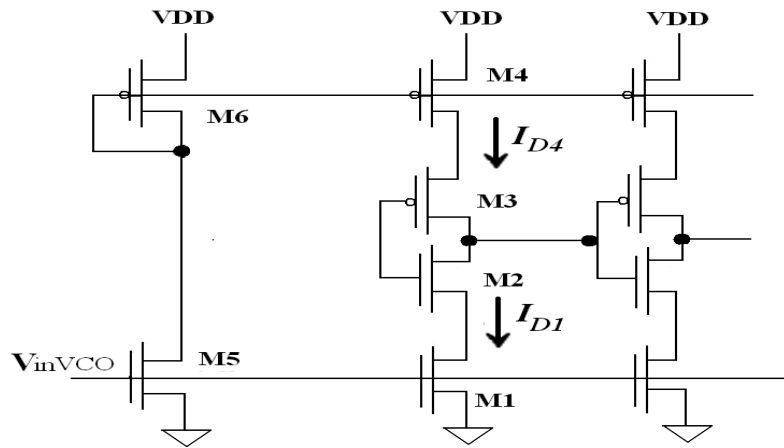


Figure1.5 Simplified view of a current starved VCO

Transistors M2 and M3 operate as an inverter while M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for current.

2.2.4 Frequency Divider

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. A simple D flip flop (DFF) acts as a frequency divider circuit. The schematic of a simple DFF based divide by 2 frequency divider circuit is shown in the Figure 1.6.

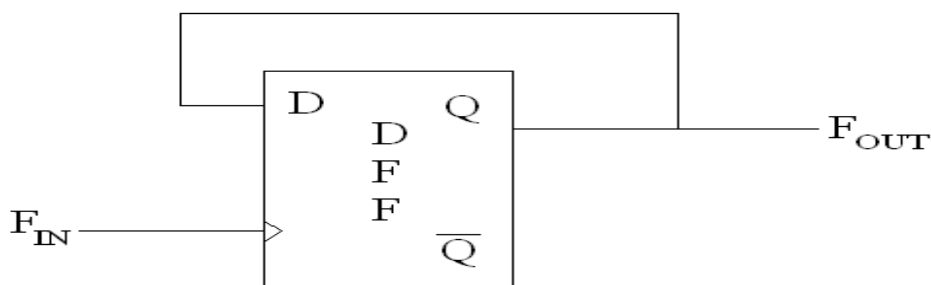


Figure1.6 Schematic of a simple DFF based divide by 2 frequency divider circuit

2.4 Terms in PLL

2.4.1 Lock in Range

Once the PLL is in lock state what is the range of frequencies for which it can keep itself locked is called as lock in range. This is also called as tracking range or holding range.

2.4.2 Capture Range

When the PLL is initially not in lock, what frequency range can make PLL lock is called as capture range. This is also known as acquisition range. This is directly proportional to the LPF bandwidth. Reduction in the loop filter bandwidth thus improves the rejection of the out of band signals, but at the same time the capture range decreases, pull in time becomes larger and phase margin becomes poor.

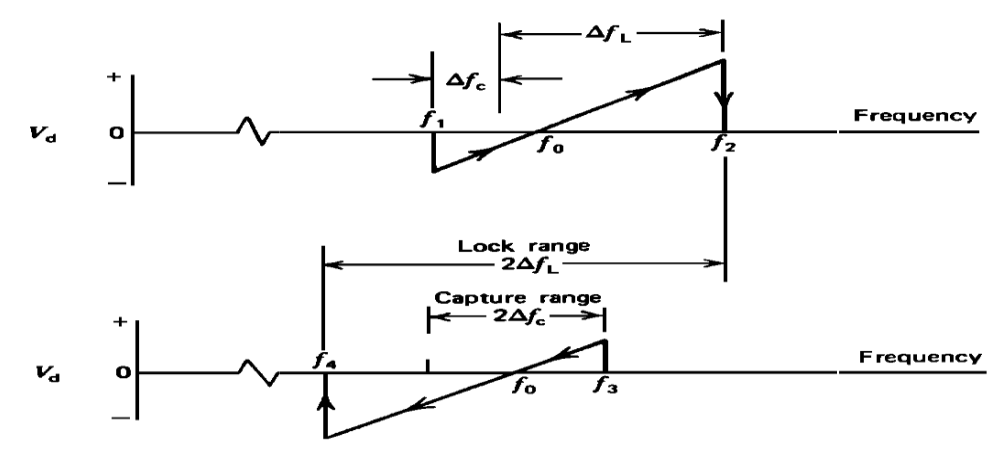


Figure1.7 Illustration of lock and capture range

2.4.3 Pull in Time

The total time taken by the PLL to capture the signal (or to establish the lock) is called as Pull in Time of PLL. It is also called as Acquisition Time of PLL.

2.4.4 Bandwidth of PLL

Bandwidth is the frequency at which the PLL begins to lose the lock with reference.

2.5 Noises in PLL

The output of the practical system deviates from the desired response. This is because of the imperfections and noises in the system. The supply noise also affects the output noise of the PLL system [12]. There are mainly 4 types of noises. They are explained below.

2.5.1 Phase Noise

The phase fluctuation due to the random frequency variation of a signal is called as phase noise. This is mostly affected by oscillator's frequency stability. The main sources of the phase noise in PLL are oscillator noise [12-15], PFD and frequency divider circuit. The main components of the phase noise are thermal and flicker noise.

2.5.2 Jitter

A jitter is the short term-term variations of a signal with respect to its ideal position in time [16]. This problem negatively impacts the data transmission quality. Jitter and phase noise are closely related and can be computed one from another. Deviation from the ideal position can occur on either leading edge or trailing edge of signal. Jitter may be induced and coupled onto a clock signal from several different sources and is not uniform over all frequencies. Excessive jitter can increase bit error rate (BER) of communication signal. In digital system Jitter leads to violation in time margins, causing circuits to behave improperly.

2.5.3 Spur

Non-desired frequency content not related to the frequency of oscillation and its harmonics is called as "Spur". There are mainly two types of spur. They are reference spur and fractional spur. Reference spur comes into picture in an integer PLL while fractional spur plays a major role in fractional PLL. When the PLL is in lock state the phase and frequency inputs to the PFD are essentially equal. There should not be any error

output from the PFD. Since this can create problem, so the PFD is designed such that, in the locked state the current pulses from the CP will have a very narrow width as shown in the Figure 1.8. Because of this the input control voltage of the VCO is modulated by the reference signal and thus produces “Reference Spur”.

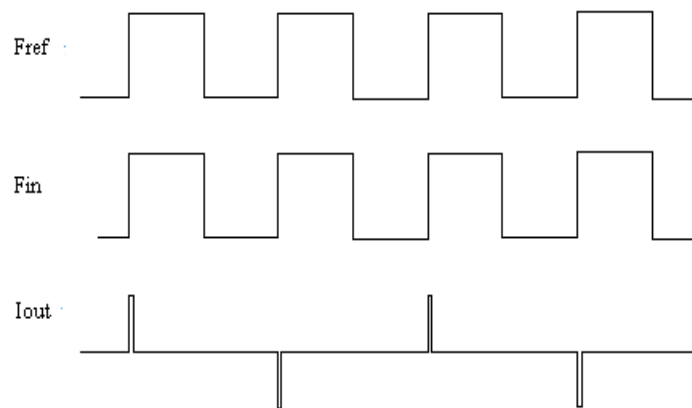


Figure 1.8 Output current pulses from charge pump in the lock state

2.5.4 Charge Pump Leakage Current

When the CP output from the synthesizer is programmed to the high impedance state, in practice there should not be any current flow. But in practical some leakage current flows in the circuit and this is known as “charge pump leakage current”.

II. Literature Survey

[1] S. M. Shahruz, “Novel phase-locked loops with enhanced locking capabilities,” *Journal of Sound and Vibration*, Vol. 241, Issue 3, 29 March 2001

The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high performance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range. Hence there is a necessity of a PLL which must operate in the GHz range with less lock time. PLL is a mixed signal circuit as its architecture involves both digital and analog signal processing units. The present work focuses on the redesign of a PLL system using the 90 nm process technology (GPDK090 library) in CADENCE Virtuoso Analog Design Environment. Here a current starved ring oscillator has been considered for its superior performance in form of its low chip area, low power consumption and wide tuneable frequency range. The layout structure of the PLL is drawn in CADENCE VirtuosoXL Layout editor. Different types of simulations are carried out in the Spectre simulator. The pre and post layout simulation results of PLL are reported in this work. It is found that the designed PLL consumes 11.68mW power from a 1.8V D.C. supply and have a lock time 280.6 ns. As the voltage controlled oscillator (VCO) is the heart of the PLL, so the optimization of the VCO circuit is also carried out using the convex optimization technique. The results of the VCO designed using the convex optimization method is compared with traditional method.

[2] H. Janardhan, and M.F. Wagdy “Design of a 1GHz Digital PLL Using 0.18 μm CMOS Technology,” *IEEE Proc. of the Third International Conference on Information Technology*, 2006

This paper focuses on the analysis and design of 1GHz basic Phase Lock Loop (PLL). The PLL circuit is designed and simulated in GPDK 180nm CMOS Technology. Its frequency range from 450MHz to 1GHz and average power consumption is 1.0494mW. The Voltage Controlled Oscillator is tuned for 400MHz to 1.2GHz

frequency and 49% to 51% duty cycle. The lock time for 450MHz is 25.39ns and for 1GHz is 42.68ns. The supply voltage VDD is 1.8V.

[3] A. Arakali, S. Gondi, and P. K. Hanumolu, "Analysis and Design Techniques for Supply-Noise Mitigation in Phase-Locked Loops", *IEEE Transactions on Circuits and Systems—I: Regular Papers*, Vol. 57, No. 11, Nov. 2010

Supply noise affects the jitter performance of ring oscillator-based phase-locked loops (PLLs) significantly. While the focus of much of the prior art is on supply noise in oscillators, this paper illustrates that supply noise in other building blocks also contribute significantly to PLL output jitter. Analytical expressions for supply-noise sensitivities are derived for each of the circuit blocks used in the PLL and insight into the mechanism through which supply noise appears at the PLL output is provided. Efficient supply-regulation schemes that combine a split-tuned PLL architecture with an optimized low-dropout regulator to achieve better than -22 dB of worst case supply-noise sensitivity for the whole PLL are presented. Fabricated in a 0.18 μm digital CMOS process, the prototype PLL occupies an area of 0.18 μm^2 and operates from a 1.8 V supply. At 1.5 GHz, the total power consumption is 3.3 mW, of which 0.54 mW is consumed in the regulators. The measured output peak-to-peak jitter is 33 ps and 41 ps with no supply noise and with a 100-mV amplitude supply noise tone injected at the worst case noise frequency.

[4] B. Razavi "A Study of Phase Noise in CMOS Oscillators", *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 3, March 1996

This paper presents a study of phase noise in two inductorless CMOS oscillators. First-order analysis of a linear oscillatory system leads to a noise shaping function and a new definition of Q. A linear model of CMOS ring oscillators is used to calculate their phase noise, and three phase noise phenomena, namely, additive noise, high-frequency multiplicative noise, and low-frequency multiplicative noise, are identified and formulated. Based on the same concepts, a CMOS relaxation oscillator is also analyzed. Issues and techniques related to simulation of noise in the time domain are described, and two prototypes fabricated in a 0.5- μm CMOS technology are used to investigate the accuracy of the theoretical predictions. Compared with the measured results, the calculated phase noise values of a 2-GHz ring oscillator and a 900-MHz relaxation oscillator at 5 MHz offset have an error of approximately 4 dB.

III. Problem Formulation

Global optimization methods such as branch and bound and simulated annealing are also used in analog circuit design. These methods are guaranteed to find the global optimal design solution. The global optimal design is determined by the branch and bound methods unambiguously. In each iteration, a suboptimal feasible design and also a lower bound on the achievable performance is maintained by this method. This enables the algorithm to terminate non-heuristically, i.e., with complete confidence that the global design has been found within a given tolerance. The branch and bound method is extremely slow, with computation growing exponentially with problem size. The trapping in a locally optimal design can be avoided by using simulated annealing (SA). This method can compute the global optimal solution but not guaranteed. Since there is no real-time lower bound is available, so termination is heuristic. This method can also handle a wide variety of performance indices and objects. The main advantage of SA is that it handles the continuous variables and discrete variables problems efficiently and reduces the chances of getting a non-globally optimal design. The only problem with this method is that it is very slow and cannot guarantee a global optimal solution

IV. Proposed Methodology

1. In this work a PLL with a better lock time is presented. The lock time of the PLL is found to be 280.6 ns.
2. The PLL circuit consumes a power of 11.9 mW from a 1.8 V D.C. supply
3. The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values a better lock time can be achieved.
4. The centre frequency of oscillation of the VCO depends upon the sizing of the transistors. The frequency deviation from the desired value can be reduced by properly choosing the transistor sizes.
5. By applying the convex optimization technique with frequency of oscillation as the main objective function, the deviation of oscillation frequency is minimized to 0.00457% from 1.2%.
6. Here the convex technique is used to find out the transistor sizing to meet only the desired frequency specification. The other constraints like area, power and phase noise can also be applied.

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