Phase-Locked Loop

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Introduction:

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock CK_{ref} to produce a high-frequency clock CK_{out} this is known as clock synthesis.

A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

Phase-Locked Loop Operation

The basic components of a phase-locked loop (PLL) are a stable reference oscillator, a phase detector, a frequency divider, a voltage-controlled oscillator (VCO), amplifiers, and filters. The following figure shows a simplified PLL block diagram.

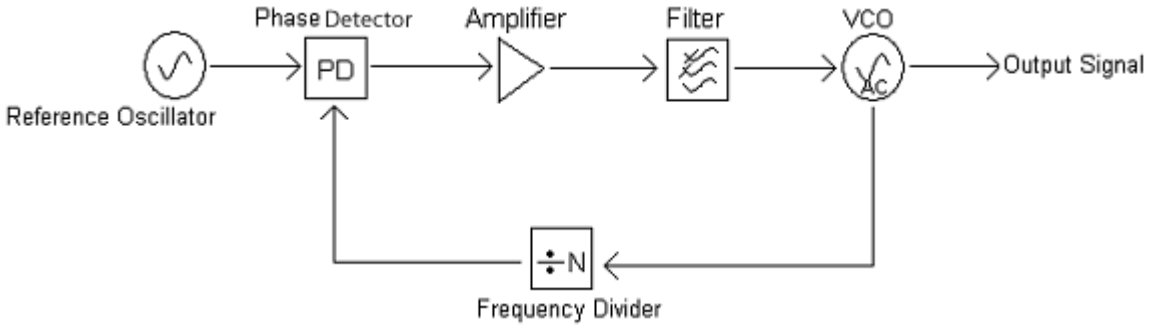

Figure 1. PLL Block Diagram

PLLs work by comparing the generated signal phase to the reference oscillator signal phase and then using the difference to adjust the generated signal. To compare the two waves, both signals must be of the same frequency. The frequency divider is used to divide down the generated signal. Because the frequency divider can divide down only an integer number of times, the generated signal must be an integer multiple of the reference oscillator signal. The phase detector returns a voltage depending on the phase difference between the two waves. This voltage is amplified, filtered, and then fed into the VCO. The VCO adjusts the signal it outputs based on this voltage.

Types of PLL

There are mainly 4 types of PLL are available. They are

1. Liner PLL
2. Digital PLL
3. All Digital PLL
4. Soft PLL

The basic block diagram of the PLL is shown in the Figure 1.1. In general a PLL consists of five main blocks:

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
3. Low Pass Filter (LPF)
4. Voltage Controlled Oscillator (VCO)
5. Divide by N Counter

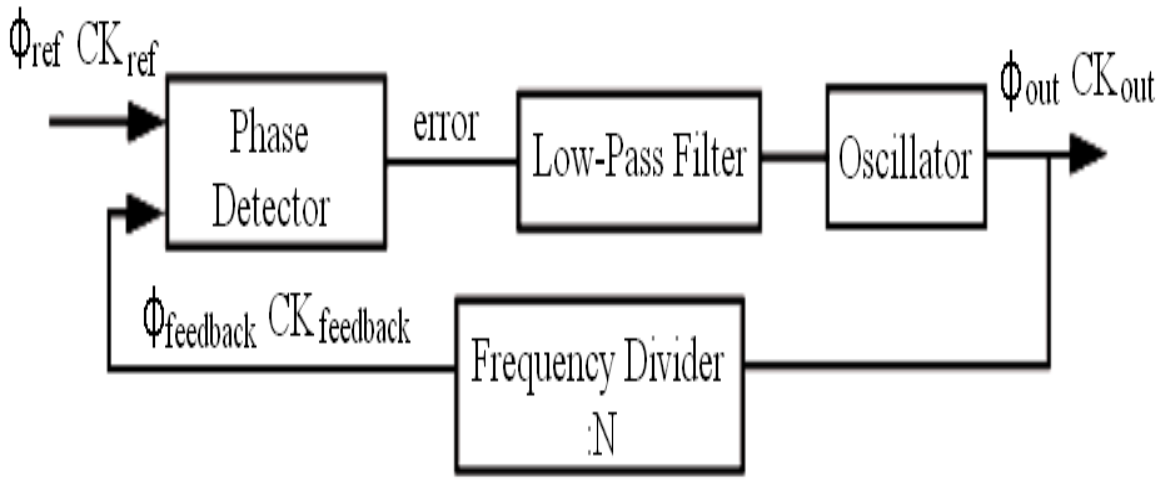

Figure1.1 Basic block diagram of a PLL

The "Phase frequency Detector" (PFD) is one of the main parts in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals "UP" and "DOWN". The "Charge Pump" (CP) circuit is used in the PLL to combine both the outputs of the PFD and give a single output. The output of the CP circuit is fed to a "Low Pass Filter" (LPF) to generate a DC control voltage. The phase and frequency of the "Voltage Controlled Oscillator" (VCO) output depends on the generated DC control voltage. If the PFD generates an "UP" signal, the error voltage at the output of LPF increases which in turn increase the VCO output signal frequency. On the contrary, if a "DOWN" signal is generated, the VCO output signal frequency decreases. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, and then we can create closed loop frequency control system.

2.2 PLL Architecture

The architecture of a charge-pump PLL is shown in Figure 1.2. A PLL comprises of several components. They are (1) phase or phase frequency detector, (2) charge pump, (3) loop filter, (4) voltage-controlled oscillator, and (5) frequency divider. The functioning of each block is briefly explained below.

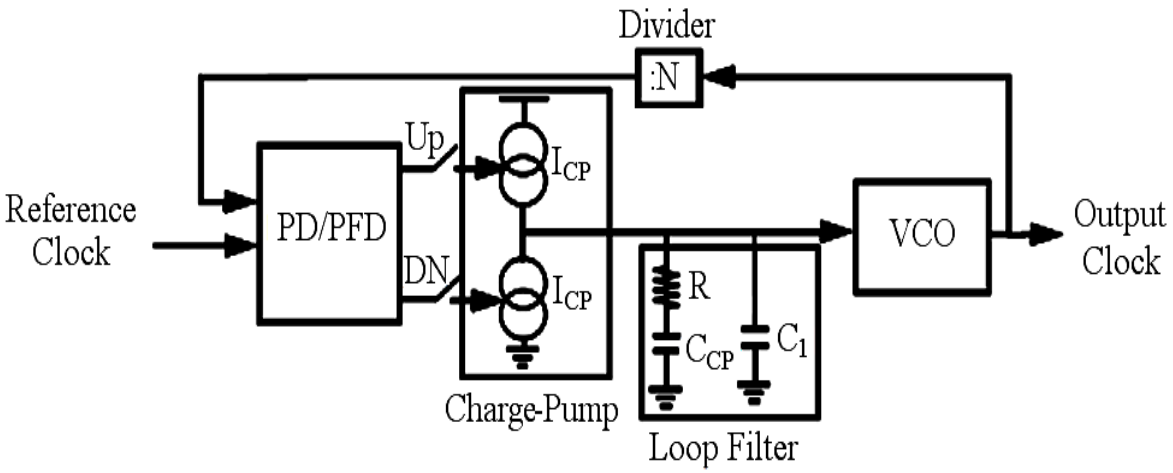

Figure1.2 Architecture of a PLL

2.2.1 Phase Frequency Detector

The "Phase frequency Detector" (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock.Depending upon the phase and frequency deviation, it generates two output signals "UP" and "DOWN" . Figure 1.3 shows traditional PFD circuit.

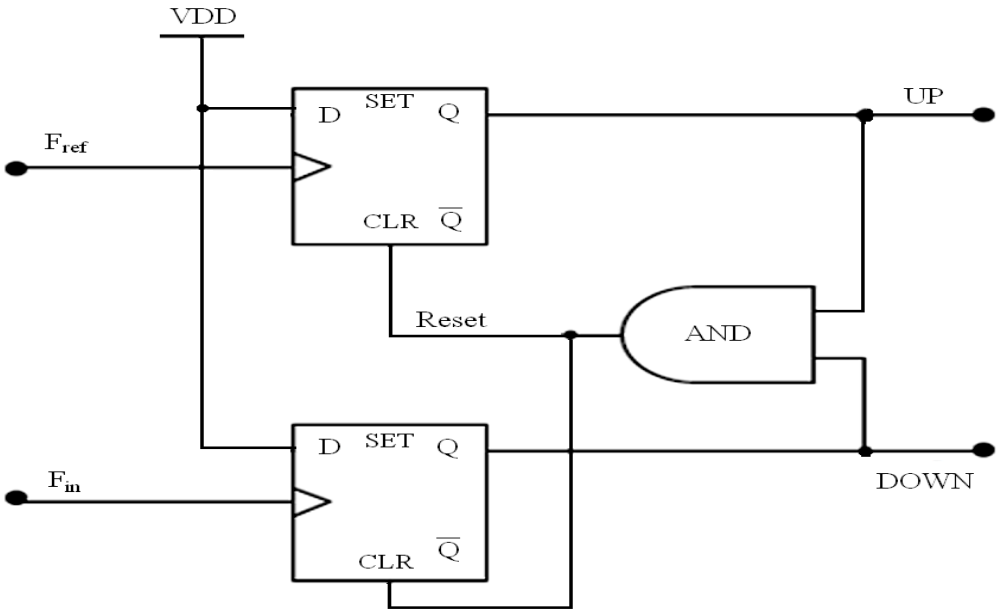

Figure1.3 Block diagram of a traditional PFD circuit

2.2.2 Charge Pump and Loop Filter

Charge pump circuit is an important block of the whole PLL system. It converts the phase or frequency difference information into a voltage, used to tune the VCO. Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. Charge pump circuit gives a constant current of value I_{PDI} which should be insensitive to the supply voltage variation [8].

The amplitude of the current always remains same but thepolarity changes which depend on the value of the "UP" and"DOWN" signal. The schematic diagram of the charge pump circuit with loop filter is shown in the Figure 1.4.

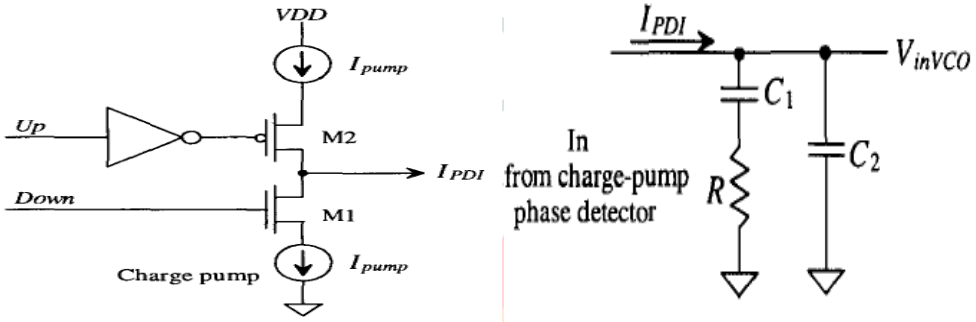

Figure1.4 Schematic diagram of the charge pump circuit with loop filter

2.2.3 Voltage Controlled Oscillator

An oscillator is an autonomous system which generates a periodic output without any input.The most popular type of the VCO circuit is the current starved voltage controlled oscillator (CSVCO). Here the number of inverter stages is fixed with 5. The simplified view of a single stage current starved oscillator is shown in the Figure 1.5.

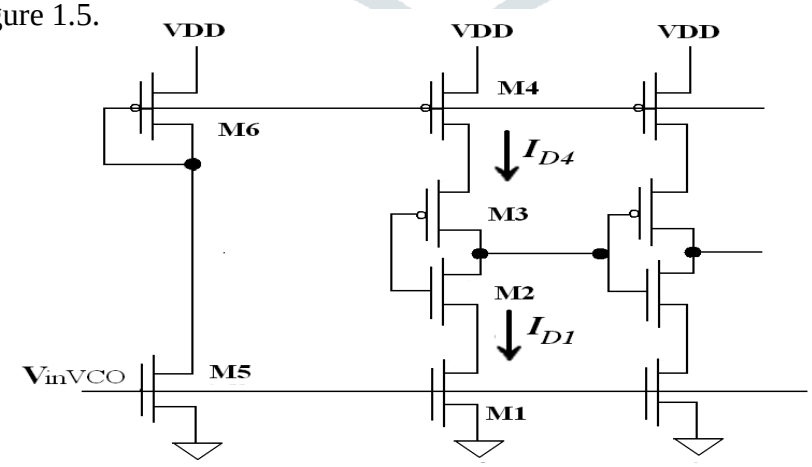

Figure1.5 Simplified view of a current starved VCO

Transistors M2 and M3 operate as an inverter while M1 and M4 operate as current sources. The current sources, Ml and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for current.

2.2.4 Frequency Divider

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. A simple D flip flop (DFF) acts as a frequency divider circuit. The schematic of a simple DFF based divide by 2 frequency divider circuit is shown in the Figure 1.6.

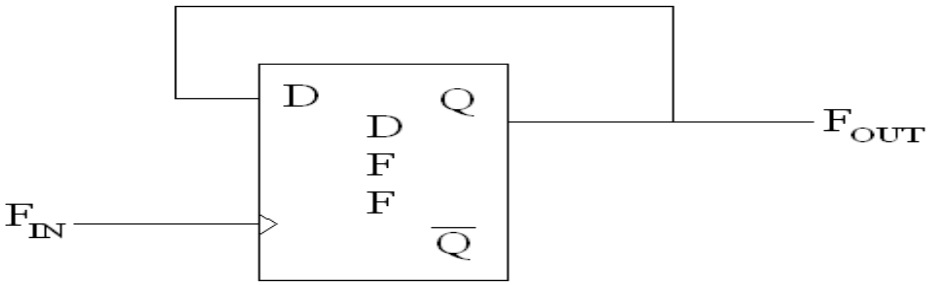

Figure1.6 Schematic of a simple DFF based divide by 2 frequency divider circuit

2.4 Terms in PLL

2.4.1 Lock in Range

Once the PLL is in lock state what is the range of frequencies for which it can keep itself locked is called as lock in range. This is also called as tracking range or holding range.

2.4.2 Capture Range

When the PLL is initially not in lock, what frequency range can make PLL lock is called as capture range. This is also known as acquisition range. This is directly proportional to the LPF bandwidth. Reduction in the loop filter bandwidth thus improves the rejection of the out of band signals, but at the same time the capture range decreases, pull in time becomes larger and phase margin becomes poor.

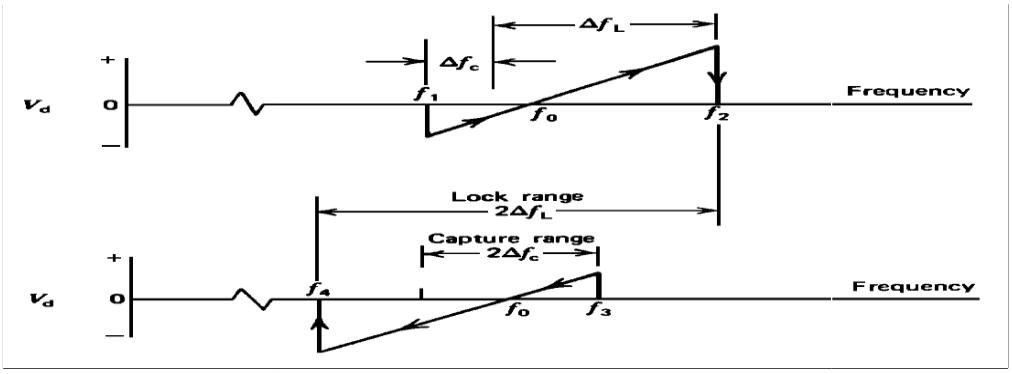

Figure1.7 Illustration of lock and capture range

2.4.3 Pull in Time

The total time taken by the PLL to capture the signal (or to establish the lock) is called as Pull in Time of PLL. It is also called as Acquisition Time of PLL.

2.4.4 Bandwidth of PLL

Bandwidth is the frequency at which the PLL begins to lose the lock with reference.

2.5 Noises in PLL

The output of the practical system deviates from the desired response. This is because of the imperfections and noises in the system. The supply noise also affects the output noise of the PLL system [12]. There are mainly 4 types of noises. They are explained below.

2.5.1 Phase Noise

The phase fluctuation due to the random frequency variation of a signal is called as phase noise. This is mostly affected by oscillator' s frequency stability. The main sources of the phase noise in PLL are oscillator noise [12-15], PFD and frequency divider circuit. The main components of the phase noise are thermal and flicker noise.

2.5.2 Jitter

A jitter is the short term-term variations of a signal with respect to its ideal position in time [16]. This problem negatively impacts the data transmission quality. Jitter and phase noiseare closely related and can be computed one from another. Deviation from the ideal position can occur on either leading edge or trailing edge of signal. Jitter may be induced and coupled onto a clock signal from several different sources and is not uniform over all frequencies. Excessive jitter can increase bit error rate (BER) of communication signal . In digital system Jitter leads to violation in time margins, causing circuits to behave improperly.

2.5.3 Spur

Non-desired frequency content not related to the frequency of oscillation and its harmonics is called as "Spur". There are mainly two types of spur. They are reference spur and fractional spur Reference spur comes into picture in an integer PLL while fractional spur plays a major role in fractional PLL. When the PLL is in lock state the phase and frequency inputs to the PFD are essentially equal. There should not be any error output from the PFD. Since this can create problem, so the PFD is designed such that, in the locked state the current pulses from the CP will have a very narrow width as shown in the Figure 1.8. Because of this the input control voltage of the VCO is modulated by the reference signal and thus produces "Reference Spur" .

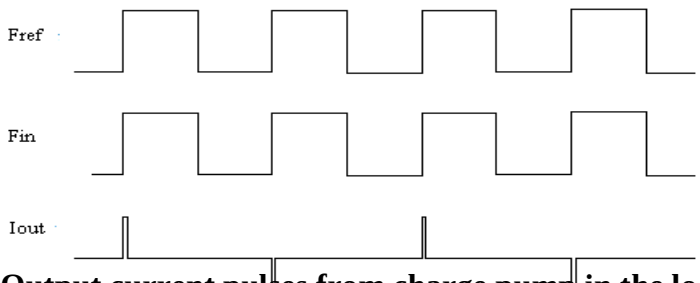

Figure1.8 Output current pulses from charge pump in the lock state

2.5.4 Charge Pump Leakage Current

When the CP output from the synthesizer is programmed to the high impedance state, in practice there should not be any current flow. But in practical some leakage current flows in the circuit and this is known as "charge pump leakage current"

Conclusion

A phase-locked loop (PLL) is a feedback control circuit that synchronizes the phase of a generated signal with that of a reference signal. It is important to keep in mind that a PLL can generate signals that are only integer multiples of the reference signal.

Phase-locked loops play a vital part in many modern-day circuits. They are used to demodulate amplitude and frequency modulated signals, synchronize clocks, recover small signals from noise, and they are used in devices such as dual-tone multiple frequency decoders and modems.