FPGA implementation of the fractional frequency synthesizers

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Abstract

The proposed work presented implementation of fractional frequency synthesizer on FPGA. The various parameters have been analyzed and comparison has been presented of the proposed design. The results of the proposed synthesizer has been simulated and synthesized by Xilinx and same results have been implemented on FPGA. In future, hybrid synthesizer may be designed on the same platform.

Keywords: PLL, DCO, Filter, FPGA, Xilinx.

I. INTRODUCTION

The Conventional PLL consists of 3 parts, PF-Detector, Loop Filter and TC Oscillator to resolve these restrictions, and few ADPLL architectures. A locked phase loop is a locked loop control system used to synchronize the frequency and phase of an input signal. In TV, radio, pager, servo motor control, telephony and many other areas analog PLL are common. Advances in telecommunications, wireless and wireless lines and smart network concepts in modern communication systems have increased demand for PLL design. Faster and more efficient operation of the PLLs is very desirable. The versatility of the locked loops phase has become all-round. Phase locked loop is an oscillator feedback system that is used to synchronize the phase with input signal frequency.

It is used widely for the demodulation and modulation of frequencies, clock recovery and communication device frequency controls. The analog approaches are traditionally used to design the PLLs. But these PLLs are affected by higher switching and time lock. The circuit complexity nature expanded too besides the analog PLLs is delicate to process parameter and ought to be updated for each new innovation. In contrast to analog PLLs, all of these issues could be resolved by ADPLL. Due to their scalability, quicker time lock and easy replacement with process changes ADPLLs have become lucrative.

Phase locked loop

A PLL is a device that locks the signal output phase in the reference signal input phase. Interesting signals may be any regular waveform, but they are usually sinusoid or digital clock.

All digital blocks are available in the ADPLL. A divider-n counter is added in the ADPLL and these are connected to feedback path for the function of a frequency synthesis. Single or parallel digital signals can be used as a signal. One popular option today for ADPLL is to install the largest number of digital circuitry. This concentrates on FPGA-based all digital PLLs that do not implement the DCO chip on the FPGA. We will focus in particular on DCOs, which can be controlled directly via a line to line interface[1-10]. Silicon Labs provides multiple I2Crystal oscillators for FPGA-based ADPLL applications (e.g. si514, si570, and si598).

Building Blocks in an ADPLL

In the ADPLL there are mainly three building blocks are available. These building blocks are digital controlled oscillator, phase detector and loop filter. These blocks are providing phase locking for operation of ADPLL. This section investigates the mostly used methods of implementing the building blocks
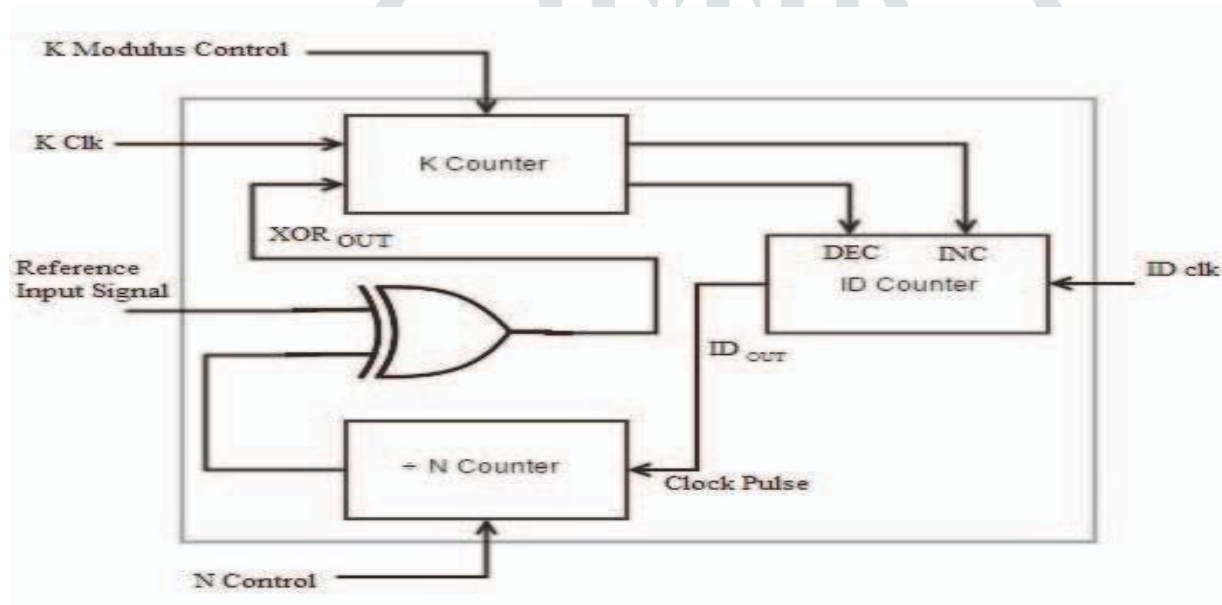
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Figure 1:-All Digital PLL circuit diagram

In Figure 1 the circuit ADPLL is shown as digital phase detector (DPD) for Ex-OR, K counter is shown as Digital Loop Filter is made by the arrangement of ID counter & N counter. The phase detector is supported by the E-XOR gate in this ADPLL design. EXOR offers simple but reliable phase detection

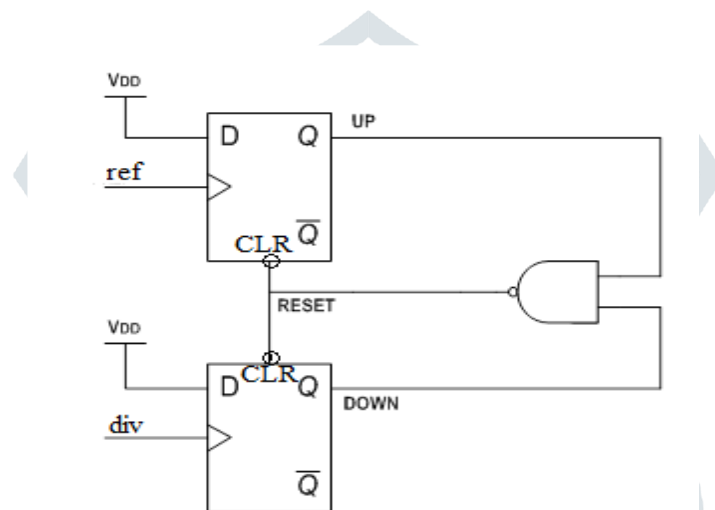**Phase frequency detector**

Two broad categories of phase detector are:

➢ Multiplier circuits

➢ Sequential circuits.

Multiplier means the average generation of products. Input signal waveform product and local waveform of the oscillator will be generated and the DC error signal will be obtained. With multiple noise signals, a properly designed multiplier system can operate on an input signal.

The sequential phase detector operation depends on the signal zero crossing. Sequential phase detector (PD) produced output voltage that is functions of a time interval between two signals zero crossing

A simple but reliable phase detection method is provided by the EXOR mechanism. The lack of sensitivity to the edges is a major issue of this mechanism. This is a flat mechanism triggered. The triggered mechanism of the edge becomes apparent to eliminate that drawback. The most popular and effective mechanism is the D-Flip-Flop-Mechanism [12].

Figure 2:-PF-Detector

Loop filter

The high phase frequency error signals are removed by loop filters. The counter 'k' is used for the loop filter. The phase-detector always works. Phase detector output is supplied to the k counter. The K counter clock is M times center frequency multiple times. M is usually 32, 16 and 8.

The most used Loop Filters are as below:
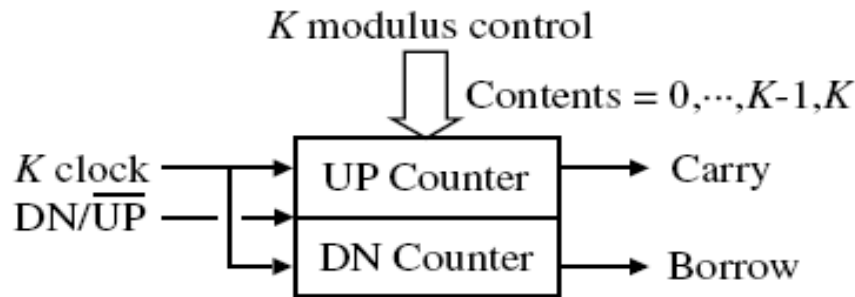
i. UP/DN counter

ii. K counter

Figure 3:-Block representation of the loop filter

In Figure 3, the loop filter block diagram is presented. There are two separate counters. The first one is known up counter and the second one is known as down counter. Both the counters count upwards in practice. The k is counter modulus. In this the range of counters is from 0 and K-1.

Digital control oscillators

DCO's are nothing more than simple modified oscillator. Their frequency is altered depending on the output value of the loop filter. It consists of a basic T-FF (toggle flip flop) and it has one output pin and three input pins. The first is the ID-clk. The second is the carry I/P (input) from the section of the loop filter, and when the input (I/P) signal leads the output (O/P) of the DCO then these signals goes high.

II. LITERATURE REVIEW

The phase locking loop literature survey reflects the fact that many investigators have used various techniques, such as digital and analog simulation, to design the Phase locked loop (PLL) by using mathematical / logical relations. Investigators have developed and attempted to identify unknown parameters and analyze the PLL by different systems, processes or phenomena on worked by ChaitaliP.Charjan and Asso.Prof.AtulS.Joshi et.al.[13-16]. Since VLSI / CMOS are very popular in real life today, it has been shown that very few researchers have been involved in the design of PLL using CMOS / VLSI technology. High-knee gate oxide, metal gate and very low-knee dielectric interconnection are the main innovations of 45 nm technology.

In this article Ms. Ujwala A. Belorkar and Dr. S.A.Ladhake et.al [24]presented Power has become one of the key design convergence paradigms in multi-Gigahertz systems like optical data connections and wireless products and the design of micro processing devices and ASIC / SOCs. The use of POWER has become a microprocessor bottleneck. The microprocessor is having the largest density of power to store data. The power supply voltage can be reduced, reducing dynamic and static power consumption, in an effort to reduce circuit power consumption. However, decreasing the delivery voltage also reduces the circuit performance, which is normally inacceptable. In some fields it is necessary in order to maintain the same throughput to replicate the circuit block with reduced delivery voltage. The paper presents the design aspects for locked loop with low power phases with use of VLSI technology. This phase locked loop is designed with the latest process

technology parameters of 45 nm, which in turn provides high speed performance at low power. High-k gate oxide, the metal-gate and very low interconnect dielectric have been the most important innovation of the 45 nm technique. VLSI technology encompasses process design, trends, chip manufacture, real circuit parameters, circuit design, electrical characteristics, building block configuration, cycle circuitry, silicone translation, CAD, practice layout design experience[17-19].

III. SIMULATION RESULT

The simulation results of the proposed architecture have been presented in fig. 4. The parameters of the architecture simulated and synthesized using Xilinx tool.
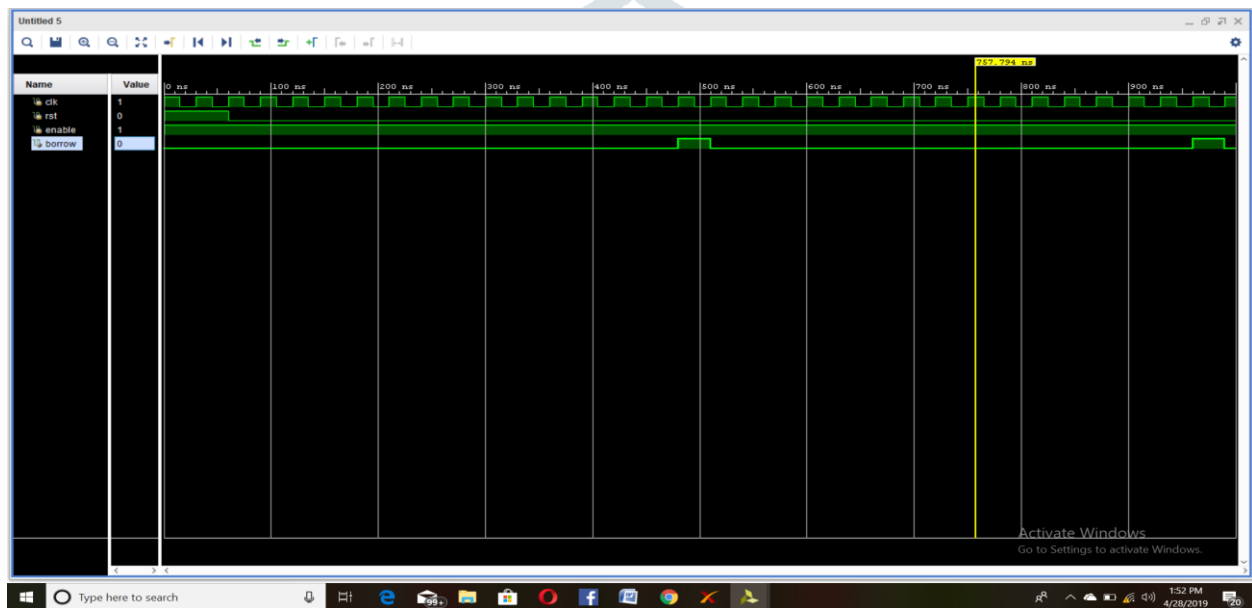

Figure 4:- Simulation result of the proposed architecture

The comparisons of the results have been presented in the table 1. It showed improvement in the proposed architecture.

Table 1:- Comparison of results of proposed architecture

Parameters	Ref.[10]	Ref.[20	Ref.[7]	Proposed work
Area	61	59	59	57
Power	339mW	340mW	338mW	337mW
Time	6.693ns	6.410ns	6.795ns	5.677ns

IV CONCLUSION

The proposed architecture of the synthesizer has been simulated and implemented using Xilinx Vivado and FPGA. The parameters power, area and delay of the synthesizer have been analyzed. The results showed improved performance of the proposed design.

The work has been simulated and implemented on FPGA. The parameters like; Area, Power and Time have been analyzed using Xilinx tool. The results show the improvement in the parameter which is shown in the table.

REFERENCES

1. Tin-Yam yau, and Tri Caohuu, ―An Efficient All-Digital Phase-Locked Loop with Input Fault Detection‖, Proceedings of IEEE International Conference on Information Science and Applications (ICISA), 26-29 April 2011, pp. 1-7.

2. J. Zhao and Y. Kim, ―A Novel All-Digital Phase-Locked Loop with Ultra-Fast frequency and Phase Acquisition,‖ 2009 IEEE International Midwest Symposium on Circuits and Systems, pp. 487-490, August 2009.

3. Q. Zhang, ―Research and application of all digital phase locked loop,‖ in Proc. of the Second International Conference on Intelligent Networks and Intelligent Systems, USA, pp. 122 – 125, 2009.

4. Tadipaneni Jhansi Rani,Jallisuneetha, "A Novel Design of All Digital Phase Locked Loop for VLSI Applications", in International Journal of Electrical, Electronics and Computer Systems (IJEECS) 2014.

5. Gayathri M G, "Design of All Digital Phase Locked Loop in VHDL" in International Journal of Engineering Research and Applications, Vol. 3, Issue 4, Jul-Aug 2013.

6. Ullas M and Krishnakumar D N, "Design and Simulation of Power efficient All Digital Phase Locked Loops (ADPLL)" in International Research Journal of Engineering and Technology (IRJET), Volume: 04 Issue: 05 | May -2017.

7. KusumLata and Manoj Kumar, "ADPLL Design and Implementation on FPGA" in International Conference on Intelligent Systems and Signal Processing (ISSP), 2013.

8. VáclavValenta and Roman Maršálek, "dual mode hybrid pll based frequency synthesizer for cognitive multi-radio applications" in The 12th International Symposium on Wireless Personal Multimedia Communications,

9. Aniruddha Chandra, ―Phase Locked Loop‖, ECE Department, NIT Durgapur, Winter School on VLSI Systems Design, WB, Jan24, 2009.

10. YoungGunPu, AnSoo Park, Joon-Sung Park and Kang-Yoon Lee, ―Low-Power, All Digital Phase-Locked loop with a Wide-Range, High Resolution TDC,‖ ETRI Journal, vol. 33, no.3, pp.366-373, June, 2011.

11. P. Hanumolu, M. Brownlee, K. Mayaram, and U. Moon, "Analysis of charge-pump phase-locked loops," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 51, no. 9, pp. 1665–1674, Sep. 2004

12. Fernando Rangel De Sousa, "A reconfigurable high frequency phase-locked loop" IEEE transactions on instrumentation & measurement Vol. 53 No. 4 Aug. 2004

13. M. Brownlee, P. Hanumolu, K. Mayaram, and U. Moon, "A 0.5 to 2.5 GHz PLL with fully differential supply regulated tuning," IEEE ISSCC Dig. Tech. Papers, pp. 588–589, Feb. 2006.

14. NavidAzizi, Student Member, IEEE, Muhammad M. Khellah, Member, IEEE, Vivek K. De, Senior Member, IEEE, and Farid N. Najm, Fellow, IEEE, "Variations-Aware Low-Power Design And Block Clustering With Voltage Scaling," IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS Vol. 15 No.7, July 2007.

15. J. Tusch, "On Frequency Sweeping in Phase-Locked Loops", IEEE Transactions on Communications (Volume: 32 , Issue: 8 , Aug 1984) .

16. D. Sahu , "A completely integrated low jitter CMOS PLL for analog front ends in system on chip environment", Proceedings of ASP-DAC/VLSI Design 2002. 7th Asia and South Pacific Design Automation Conference and 15h International Conference on VLSI Design Jan 2002.

17. S. Dosho , N. Yanagisawa, "A background optimization method for PLL by measuring phase jitter performance",2004 Symposium on VLSI Circuits. Digest of Technical Papers June 2004.

18. Hun Hee Lee ; Won Hwi Park , "High speed digital hybrid PLL frequency synthesizer", 2005 Asia-Pacific Microwave Conference Proceedings Dec 2005.

19. M. Houdebine and s. Dedieu, "a new fractional frequency synthesizer architecture with stability and robustness analysis" in elsevier 2005.