A Seventeen Level Inverter Topology for Induction Motor Drives by reduced Switch Count to twelve switches per phase

N. Soujanya[1] , Asst. professor
A. Padma[2], Asst. professor
R. Babu [3] Assoc. professor

Department of Electrical and Electronic Engineering
VITS Karimnagar, India
Email: n.sowjanya08024@gmail.com*
Email: anthagiri.padma@gmail.com*
Email: baburondi@gmail.com*

Abstract**—** *This paper shows a seventeen level inverter topology for open end acceptance engine drives requiring just twelve switches per stage. One three-level inverter and one seven-level inverter with DC interface voltages in 3:1 proportion are associated with the two closures of the stator twisting of the enlistment engine to create a seventeen level space vector structure. A level moved transporter based plan is utilized to regulate the inverter, which requires just momentary stage voltage references. Determination of exchanging states is utilized to guarantee that the two inverters supply genuine energy to the engine the over whole regulation range, forestalling cheating of the DC transport. The topology was tried for relentless state operation over the whole regulation range, and exploratory outcomes are discussed*

.

I. INTRODUTION
II.

Multilevel inverters are the favored decision for most medium voltage high power modern applications. Key favorable circumstances of multilevel inverters more than two-level inverters incorporate decreased dV/dt bring down electromagnetic obstruction and lower gadget evaluations. The enhanced symphonious execution results in smoother swell free torque in engine drive applications and dispenses with the requirement for cumbersome line channels. Effectiveness is additionally enhanced because of lower successful exchanging frequencies. The Cascaded H-Bridge (CHB), Neutral Point Clamped (NPC) and Flying Capacitor (FC) topologies are among the most punctual multilevel inverter topologies. CHB topologies require confined power supplies in each stage for creating multilevel yields. NPC topologies require a solitary DC supply yet require extra cinching diodes to brace the inverter posts to the DC transport midpoint. At the point when more levels are wanted, the quantity of bracing diodes required can be restrictive. Extraordinary strategies are utilized to avoid unbalance in the DC transport midpoint. FC topologies utilize various drifting capacitors to create multilevel yields from a solitary DC supply. Subordinate and half and half topologies have likewise been developed. Multilevel operation is additionally conceivable with acceptance engines (IMs) in the open end arrangement. Where two 3-inverters are associated with the two finishes of the machine stator winding.

II. METHODOLOGY

The inverters should be fueled by disconnected power supplies to anticipate regular mode streams through the engine. As power levels rise, constrains on consonant substance require the utilization of inverters with more number of levels. For huge number of levels, CHB topologies can produce 2m + 1 levels with m fell cells per stage. Despite the fact that this approach offers expanded seclusion, the aggregate segment tally can turn out to be high. For a seventeen level yield, eight CHB cells (32 switches and eight secluded power supplies) would be required per stage. A mixture seventeen-level topology with a solitary DC interface has been proposed. Requiring sixteen switches and four capacitors for every stage

The seventeen level inverter topology introduced in this paper requires just 12 switches and two capacitors for every stage, with two secluded DC supplies. Voltages of every single drifting capacitor are adjusted at exchanging recurrence utilizing a hysteresis controller .At startup the capacitors can be charged utilizing the stage streams, wiping out the requirement for pre-charging hardware. A tweak conspire in light of the level moved transporter (LSC) PWM approach [13] is likewise exhibited, trailed by experimental approval

III. POWER CIRCUIT

The proposed topology consists of two three-phase inverters driving an induction motor in the open end configuration (fig. 1). Inverter-1 is connected to the start terminals (A, B, and C) of the phase windings while inverter-2 is connected to the end terminals (A', B', and C'). The inverters are powered by unequal DC sources of magnitude $6V_{DC}$ /8 and $2V_{DC}$ /8 respectively. Electrical isolation of the DC sources ensures that common mode current does not flow through the motor windings [9].

Inverter-1 is a three-level flying capacitor inverter with four switches and one capacitor per phase. The A-phase switches consist of two complementary pairs: SA0 and SA0', and SA1 and SA1'. The floating capacitor C1A is maintained at a nominal voltage of $3V_{DC}/8$. As a result, the pole voltage (V_{AO}) can have one of three values: 0, $3V_{DC}/8$ or $6V_{DC}/8$. The B- and C- phases are identical, with four switches and one capacitor each. All switches of inverter-1 are rated for a nominal blocking voltage of $3V_{DC}/8$.

Inverter-2 has a hybrid topology formed by cascading H-Bridges to the three phases of a three-level flying capacitor inverter The flying capacitor (FC) stage consists of two complementary switch pairs, e.g. SA2, SA2', SA3, and SA3' for A-phase. DC power comes from a source of magnitude

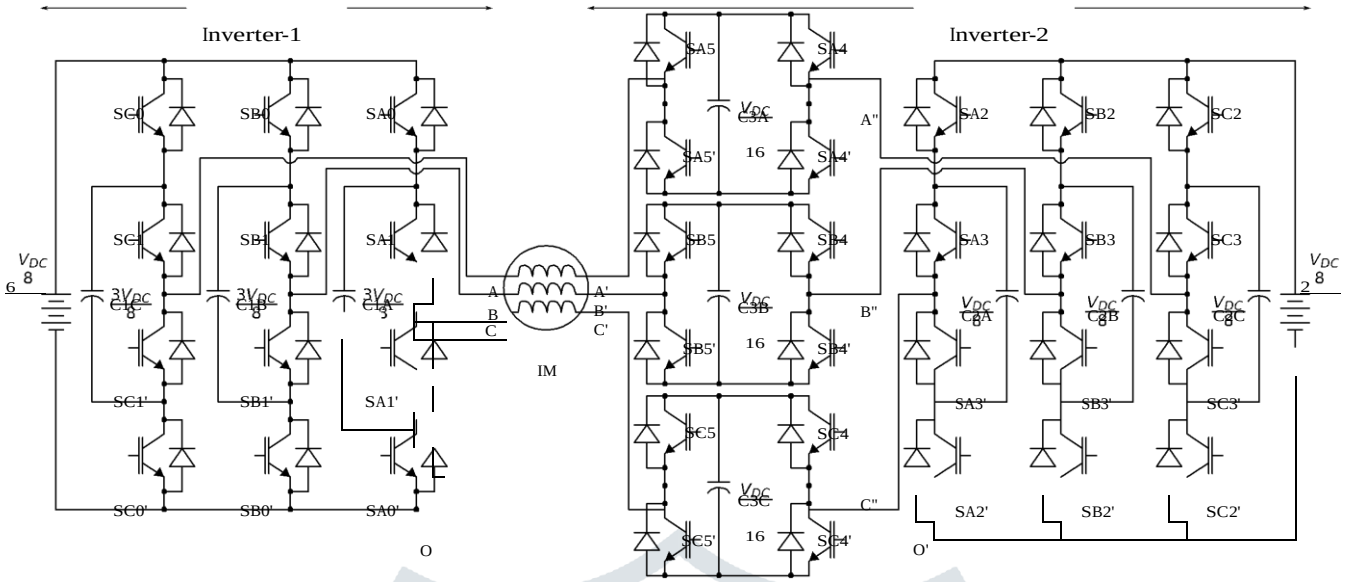


Figure 1. Proposed seventeen level inverter topology with twelve switches and two floating capacitors per phase powered by two isolated DC supplies.

$2V_{DC}/8$, and the floating capacitors (C2A, C2B, and C2C) are maintained at a nominal voltage of $V_{DC}/8$. The output voltage of this stage ($V_{A"O'}$, $V_{B"O'}$, and $V_{C"O'}$) can take one three levels: 0, $V_{DC}/8$ and $2V_{DC}/8$. These switches need a lower nominal DC blocking rating of just $V_{DC}/8$.

A floating H-bridge is connected to the each phase of the FC stage of inverter-2. The H-bridge for A-phase consists of one capacitor (C3A) and four switches (SA4, SA4', SA5, and SA5'). The nominal voltage across capacitor C3A is maintained at $V_{DC}/16$. As a result the switches of the H-bridge need a nominal voltage blocking rating of only be $V_{DC}/16$. The output voltage ($V_{A"A'}$) can take one of three levels: ($-V_{DC}/16$), 0 or ($+V_{DC}/16$). The voltage $V_{A'O'}$ can thus have one of seven possible instantaneous levels: $-V_{DC}/16$, 0, $V_{DC}/16$, $2V_{DC}/16$, $3V_{DC}/16$, $4V_{DC}/16$, or $5V_{DC}/16$.

A. Flying capacitor voltage balancing

The pole voltage $V_{AO}=3V_{DC}/8$ can be obtained in two ways (fig. 2). If SA0 and SA1' are turned on, the capacitor C1A is connected to the DC bus positive. With the current direction as indicated, this causes C1A to charge (fig. 2a). If, however, SA0' and SA1 are turned on, C1A is connected to the DC bus negative and will discharge (fig. 2b). If the current is reversed the switching states have the opposite effect – turning on SA0 and SA1' discharges C1A and turning on SA0' and SA1 charges C1A. For pole voltages of $V_{AO}=6V_{DC}/8$ or $V_{AO}=0$, capacitor C1A is completely bypassed and its voltage remains unaffected. The capacitor of each phase can thus be controlled independently, for any load power factor or modulation index, simply by choosing the appropriate switching state based on the current direction of that phase. For inverter-2, C2A, C2B and C2C can be balanced in the same way.

B. H-Bridge capacitor voltage balancing

The floating capacitors in the cascaded H-bridges C3A, C3B and C3C also require voltage balancing. The output $V_{A'A"}=V_{DC}/16$ can only be generated by turning on SA5 and SA4' (fig. 3a and fig. 3c). With current as shown, C3A will charge. Similarly, $V_{A'A"}=-V_{DC}/16$ can only be generated by turning on SA5' and SA4 (fig. 3b and fig. 3d), and C3A will discharge. Consider the pole voltage $V_{A'O'}=3V_{DC}/16$, which can be obtained in two ways. With inverter-2 FC stage generating $V_{A"O'}=2V_{DC}/16$, the CHB adds $V_{DC}/16$ (fig. 3a) and C3A is charged. Alternatively, with inverter-2 FC stage generating $V_{A"O'}=4V_{DC}/16$, the CHB subtracts $V_{DC}/16$ (fig. 3b) and C3A is discharged. Similarly, $V_{A'O'}=V_{DC}/16$ can be generated with $V_{A"O'}=2V_{DC}/16$ and $V_{A'A"}=V_{DC}/16$ or with $V_{A"O'}=0$ and $V_{A'A"}=-V_{DC}/16$. For $V_{A'O'}=0$, $V_{A'O'}=2V_{DC}/16$, and $V_{A'O'}=4V_{DC}/16$, the H-bridge capacitor is bypassed and its voltage is unaffected. For pole voltages $V_{A'O'}=5V_{DC}/16$ and $V_{A'O'}=-V_{DC}/16$. The pole voltage $V_{A'O'}=5V_{DC}/16$ can be generated in exactly one way, with $V_{A"O'}=4V_{DC}/16$ and $V_{A'A"}=V_{DC}/16$ (fig. 3c). With phase current as shown, C3A will only discharge. This switching state can be used when C3A needs to be discharged, and cannot be applied indefinitely. Similarly, $V_{A'O'}=-V_{DC}/16$ can be generated only with $V_{A"O'}=0$ and $V_{A'A"}=-V_{DC}/16$ (fig. 3d), causing C3A to charge. As a result this switching state can be when C3A needs to be charged.

C. Pole voltage levels

The voltage across the motor phase windings can be expressed in terms of the inverter pole voltages (1).

$$\begin{aligned} V_{AA'} &= V_{AO} - V_{A'O'} + V_{OO'} \\ V_{BB'} &= V_{BO} - V_{B'O'} + V_{OO'} \\ V_{CC'} &= V_{CO} - V_{C'O'} + V_{OO'} \end{aligned} \quad (1)$$

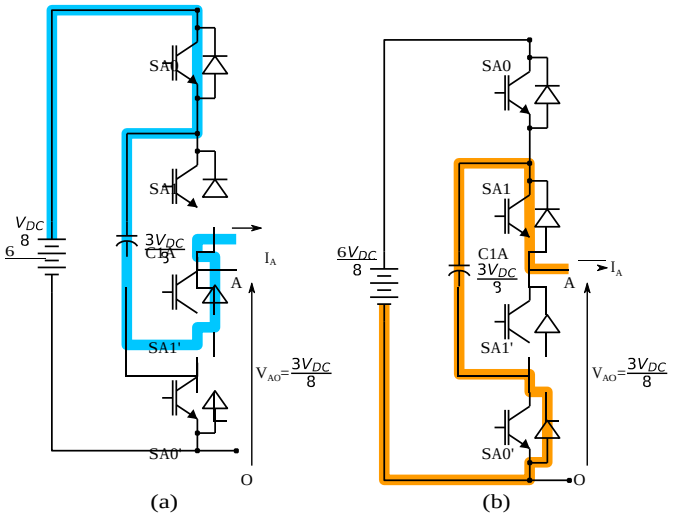


Figure 2. Switching states of inverter-1 A-phase for $V_{AO}=3V_{DC}/8$: (a)C1A charging (b) C1A discharging

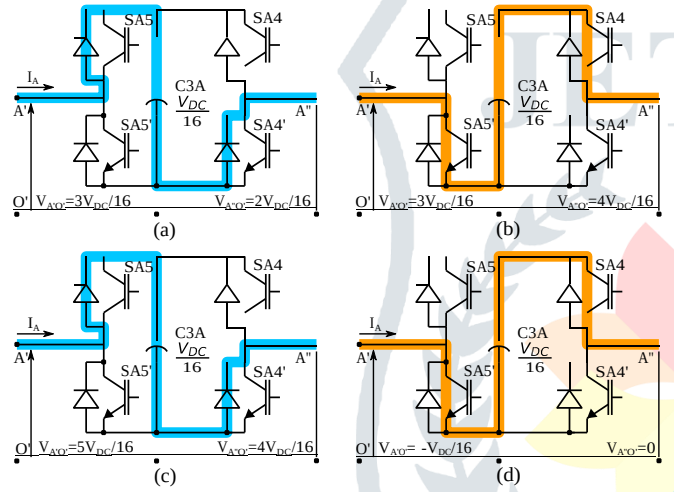


Figure 3. Switching states of inverter-2 A-phase H-Bridge: (a,c) $V_{A'A''}=V_{DC}/16$, C3A discharging (b,d) $V_{A'A''}=-V_{DC}/16$, C3A charging

Here, $V_{OO'}$ consititutes a common mode voltage and does not affect the phase currents. Only the differential mode voltages (V_{AO}-$V_{A'O'}$, V_{BO}-$V_{B'O'}$, and V_{CO}-$V_{C'O'}$) affect the phase currents [12]. All the possible instantaneous values of (V_{AO}-$V_{A'O'}$) are assigned numeric levels (-1) through 17 as listed in table I. The voltage levels V_{AO}-$V_{A'O'}=V_{DC}/16$ (Level 5) and V_{AO}-$V_{A'O'}=7V_{DC}/16$ (Level 11) can be obtained in two ways. The choice is used to balance the H-bridge capacitor as described earlier. The two extreme levels (level −1 with $V_{AA'}=-V_{DC}/16$ and level 17 with $V_{AA'} = 13V_{DC}/16$) cannot be used since there is no provision for controlling the CHB capacitors. This leaves seventeen usable phase voltage levels from $-4V_{DC}/16$ to $12V_{DC}/16$ in steps of $V_{DC}/16$.

III. Space Vector Structure

The space vector structure of the proposed topology is shown in fig. 4. The output of inverter-1 is represented as

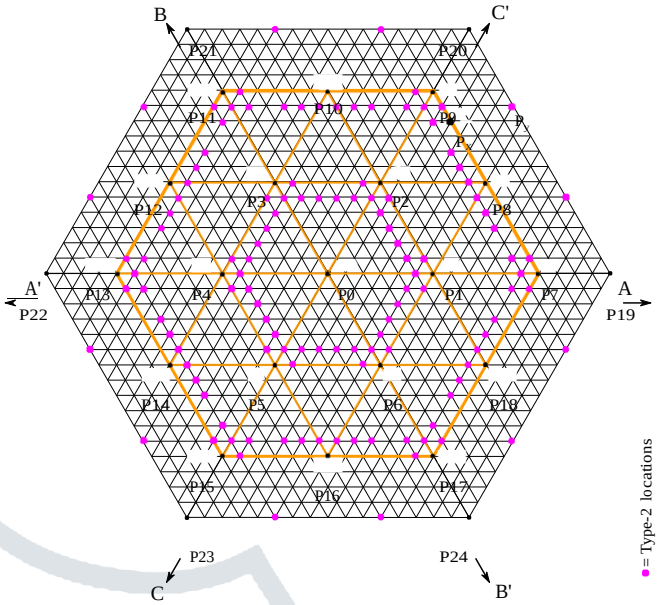


Figure 4. Space vector structure of proposed topology: The outer most hexagon (P19-P24) has a radius of V_{DC}. Locations P1-P18 can be generated by inverter-1 alone. Type-2 locations are highlighted.

a voltage space vector using (2).

$$\vec{V}_1 = V_{AO} + V_{BO}\angle -120^\circ + V_{CO}\angle -120^\circ \qquad (2)$$

With the origin at point P0, inverter-1 can generate voltage space vectors corresponding to the locations P1 through P18. The hexagon with vertices P1 through P6 has a radius of $3V_{DC}/8$. The hexagon bound by points P7 through P18 has a radius of $6V_{DC}/8$. The pole voltages applied by inverter-2 directly oppose those applied by inverter-1. (Thus the A', B', and C' axes are opposite the A, B, and C axes.) The voltage space vector applied by inverter-2 is given by (3).

$$\vec{V}_2 = -V_{A'O'} + V_{B'O'}\angle -60^\circ + V_{C'O'}\angle 60^\circ \qquad (3)$$

The effective voltage space vector seen by the motor is the sum of the two space vectors ($\vec{V} = \vec{V}_1 + \vec{V}_2$) [12]. The boundary of the space vector structure (the hexagon P19-P24) thus has a radius of V_{DC}. The structure is symmetric and can be subdivided into equilateral triangles of each side $V_{DC}/16$. Most space vector locations (SVLs) can be obtained without any phase generating levels 5 ($V_{DC}/16$) or 11 ($7V_{DC}/16$), and are called type-1 SVLs. The remaining locations are called type-2 SVLs, and are marked in fig. 4.

To generate a desired space vector, it is necessary to first determine the vectors $\vec{V}_1$ and $\vec{V}_2$ that must be applied by the two inverters. For most SVLs, multiple combinations of $\vec{V}_1$ and $\vec{V}_2$ are possible. As an example, the SVL P_x can be generated in two ways (fig. 5). If inverter-1 applies the vector $\vec{V}_1$ (corresponding to the location P9), inverter-2 must apply the vector $\vec{V}_2$ to generating the net space vector $\vec{V}_{eff}$. The component of $\vec{V}_2$ along $\vec{V}_{eff}$ is negative, which indicates that inverter-2 receives power from inverter-1. This reverse power flow can cause uncontrolled overcharging of the DC bus, resulting in pole voltage distortion.

Level	V_{AO}-$V_{A'O'}$	V_{AO}	$V_{A'O'}$	Level	V_{AO}-$V_{A'O'}$	V_{AO}	$V_{A'O'}$	Level	V_{AO}-$V_{A'O'}$	V_{AO}	$V_{A'O'}$
-1	$-5V_{DC}/16$	0	$5V_{DC}/16$	5	$V_{DC}/16$	$6V_{DC}/16$	$5V_{DC}/16$	11	$7V_{DC}/16$	$12V_{DC}/16$	$5V_{DC}/16$
0	$-4V_{DC}/16$	0	$4V_{DC}/16$	6	$2V_{DC}/16$	$6V_{DC}/16$	$4V_{DC}/16$	12	$8V_{DC}/16$	$12V_{DC}/16$	$4V_{DC}/16$
1	$-3V_{DC}/16$	0	$3V_{DC}/16$	7	$3V_{DC}/16$	$6V_{DC}/16$	$3V_{DC}/16$	13	$9V_{DC}/16$	$12V_{DC}/16$	$3V_{DC}/16$
2	$-2V_{DC}/16$	0	$2V_{DC}/16$	8	$4V_{DC}/16$	$6V_{DC}/16$	$2V_{DC}/16$	14	$10V_{DC}/16$	$12V_{DC}/16$	$2V_{DC}/16$
3	$-1V_{DC}/16$	0	$V_{DC}/16$	9	$5V_{DC}/16$	$6V_{DC}/16$	$V_{DC}/16$	15	$11V_{DC}/16$	$12V_{DC}/16$	$V_{DC}/16$
4	0	0	0	10	$6V_{DC}/16$	$6V_{DC}/16$	0	16	$12V_{DC}/16$	$12V_{DC}/16$	0
5	$V_{DC}/16$	0	$-V_{DC}/16$	11	$7V_{DC}/16$	$6V_{DC}/16$	$-V_{DC}/16$	17	$13V_{DC}/16$	$12V_{DC}/16$	$-V_{DC}/16$

Table I. A-phase voltage levels for all combinations of inverter pole voltages.

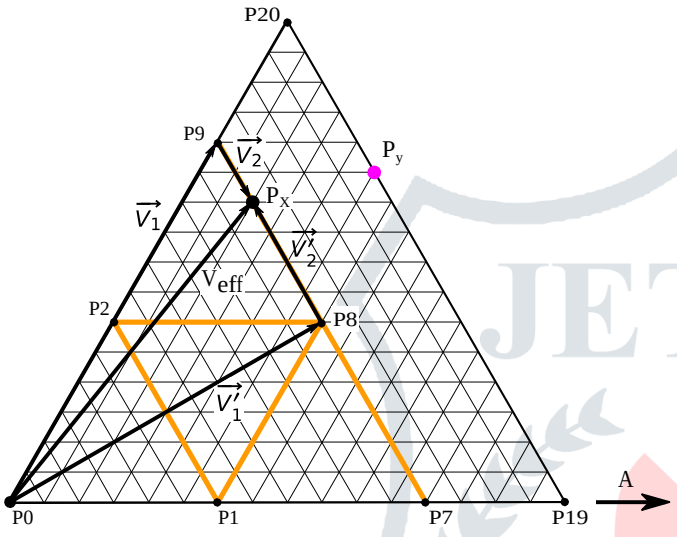


Figure 5. Vector combinations for generation of space vector $\hat{\bar{V}}_{eff}$ corresponding to location P_x

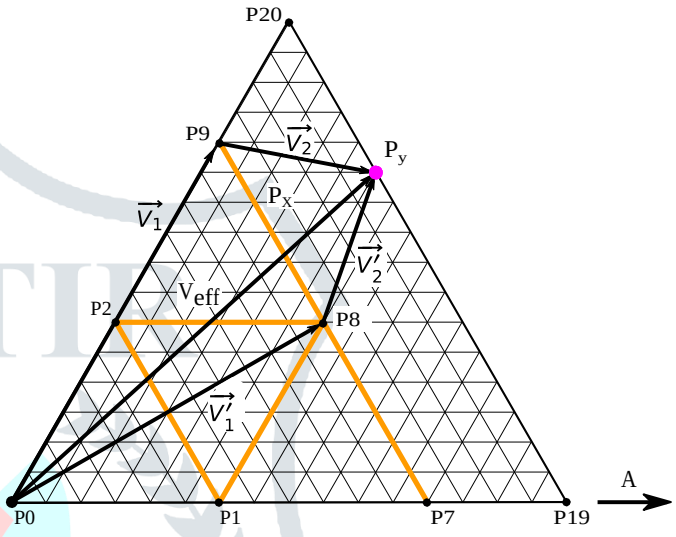


Figure 6. Vector combinations for generation of space vector $\hat{\bar{V}}_{eff}$ corresponding to type-2 location P_y

This can be avoided if the other vector combination is used – inverter-1 applies the space vector $\hat{\bar{V}}_1'$ (corresponding to the location P8) while inverter-2 applies $\hat{\bar{V}}_2$ (fig. 5). Here the components of $\hat{\bar{V}}_1$ and $\hat{\bar{V}}_2$ along the effective vector $\hat{\bar{V}}_{eff}$ are positive, and as a result both inverters deliver power to the load. This choice of vectors for each location can be precomputed and looked up at run time.

Type-2 SVLs have one more constraint: the vectors $\hat{\bar{V}}_1$ and $\hat{\bar{V}}_2$ must be selected based on the state of the H-bridge capacitors. One such location, P_y shown in fig. 6, can be obtained by two vector combinations: $\hat{\bar{V}}_1$ and $\hat{\bar{V}}_2$; or $\hat{\bar{V}}_1'$ and $\hat{\bar{V}}_2'$. Inverter-2 supplies power in both cases, so both can be used. The vector $\hat{\bar{V}}_2$ can in turn be generated with two pole voltage combinations: $V_{A'O'}=-V_{DC}/16$, $V_{B'O'}=4V_{DC}/16$, and $V_{C'O'}=3V_{DC}/16$ or $V_{A'O'}=0$, $V_{B'O'}=5V_{DC}/16$, and $V_{C'O'}=4V_{DC}/16$. Similarly, the vector $\hat{\bar{V}}_2'$ can be generated with two pole voltage combinations: $V_{A'O'}=0$, $V_{B'O'}=-V_{DC}/16$, and $V_{C'O'}=4V_{DC}/16$ or $V_{A'O'}=V_{DC}/16$, $V_{B'O'}=0$, and $V_{C'O'}=5V_{DC}/16$. Based on the directions of phase currents and voltages of the H-bridge capacitors, the appropriate combination is chosen to balance the H-bridge capacitors.

IV. Modulation Scheme

A level-shifted carrier (LSC) based pulse-width modulation (PWM) scheme [13] is used for the proposed topology. This approach requires only the instantaneous three phase voltage references, which allows use of scalar or vector control.

The reference voltage for a phase (V_{ph}^*) has a range of 0 to V_{DC}. This is first scaled to generate a scaled reference signal V_{ref} with range [0,16] using (4).

$$V_{ref} = V_{ph}^* \times \frac{16}{V_{DC}} \tag{4}$$

This range corresponds to the available levels (0 to 16) listed in table I. Then, V_{ref} is expressed as a sum of an integer and a fraction using (5).

$$V_{ref} = V_{int} + V_{frac} \tag{5}$$

Here, V_{int} is the greatest integer less than or equal to V_{ref} and consequently $0 \leq V_{frac} \leq 1$. The fractional component is passed to a dual slope PWM generation module to generate the PWM signal, with the duty cycle being equal to V_{frac}. The integer component together with the PWM signal are used to determine the phase voltage level to be applied at any instant. For example, if the reference signal V_{ref} has a value of 7.2, voltage level 7 ($3V_{DC}/16$) must be applied for 80%

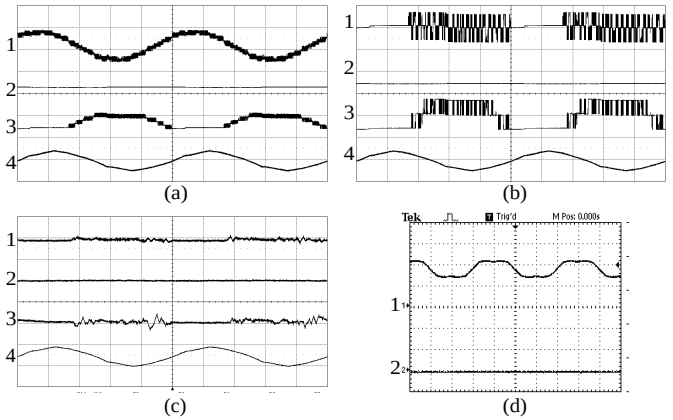


Figure 7. Experimental results for 10Hz operation
(a) Voltage and current waveforms. X-Axis: 20ms/div. (1) A-phase voltage $V_{AA'}$ (Y-axis: 50 V/div). (2) Inverter-1 pole voltage V_{AO} (Y-axis: 200 V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y-axis: 100 V/div). (4) A-Phase current (Y-axis: 1A/div)
(b) Voltage and current waveforms. X-Axis: 20ms/div. (1) Inverter-2 CHB stage voltage $V_{A'A''}$ (Y-axis: 25 V/div). (2) Inverter-1 pole voltage V_{AO} (Y-axis: 200 V/div). (3) Inverter-2 FC stage output $V_{A''O'}$ (Y-axis: 50 V/div). (4) A-Phase current (Y-axis: 1A/div)
(c) Capacitor voltage waveforms. X-Axis: 20ms/div. (1) Ripple in flying capacitor C3A, (AC coupled) (Y-axis: 2mV/div). (2) Ripple in flying capacitor C1A, (AC coupled) (Y-axis: 1V/div). (3) Ripple in flying capacitor C2A, (AC coupled) (Y-axis: 1V/div). (4) A-Phase current (Y-axis: 1A/div)
(d) Controller outputs. X-Axis: 25ms/div. (1) Phase voltage reference (Y-axis: 1V/div) (2) Type-2 Space vector location traversal (Y-axis: 1.8V/div)

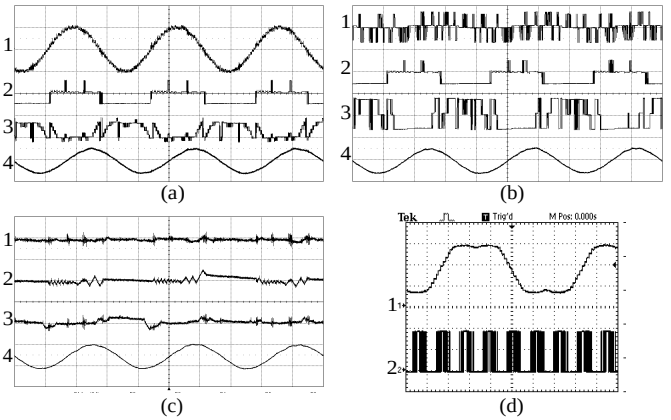
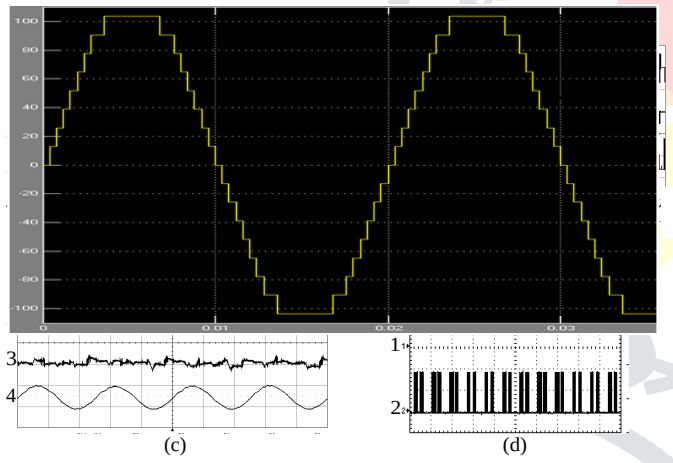
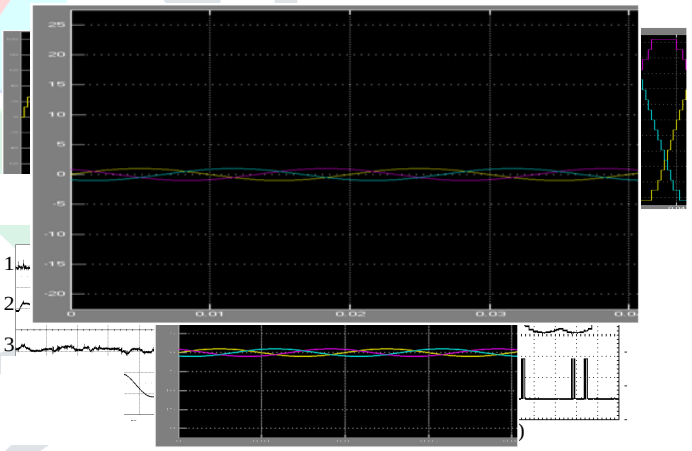


Figure 9. Experimental results for 30Hz operation
(a) Voltage and current waveforms. X-Axis: 10ms/div. (1) A-phase voltage $V_{AA'}$ (Y-axis: 100 V/div). (2) Inverter-1 pole voltage V_{AO} (Y-axis: 200 V/div). (3) Inverter-2 pole voltage $V_{A'O'}$ (Y-axis: 100 V/div). (4) A-Phase current (Y-axis: 1A/div)
(b) Voltage and current waveforms. X-Axis: 10ms/div. (1) Inverter-2 CHB stage voltage $V_{A'A''}$ (Y-axis: 25 V/div). (2) Inverter-1 pole voltage V_{AO} (Y-axis: 200 V/div). (3) Inverter-2 FC stage output $V_{A''O'}$ (Y-axis: 50 V/div). (4) A-Phase current (Y-axis: 1A/div)
(c) Capacitor voltage waveforms. X-Axis: 10ms/div. (1) Ripple in flying capacitor C3A, (AC coupled) (Y-axis: 2mV/div). (2) Ripple in flying capacitor C1A, (AC coupled) (Y-axis: 1V/div). (3) Ripple in flying capacitor C2A, (AC coupled) (Y-axis: 1V/div). (4) A-Phase current (Y-axis: 1A/div)
(d) Controller outputs. X-Axis: 5ms/div. (1) Phase voltage reference (Y-axis: 1V/div) (2) Type-2 Space vector location traversal (Y-axis: 1.8V/div)





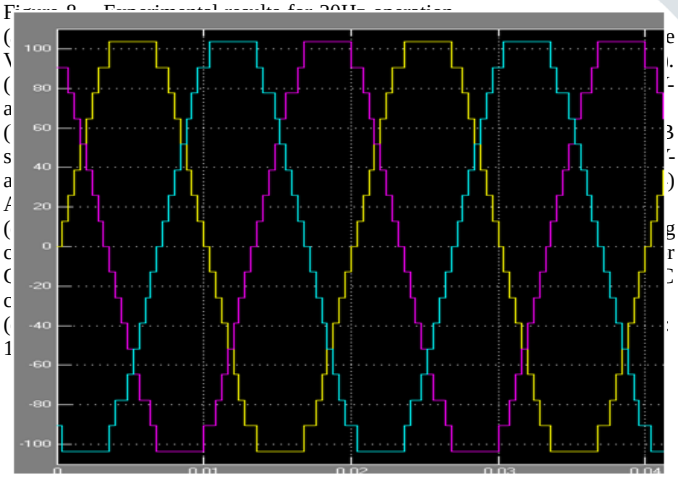
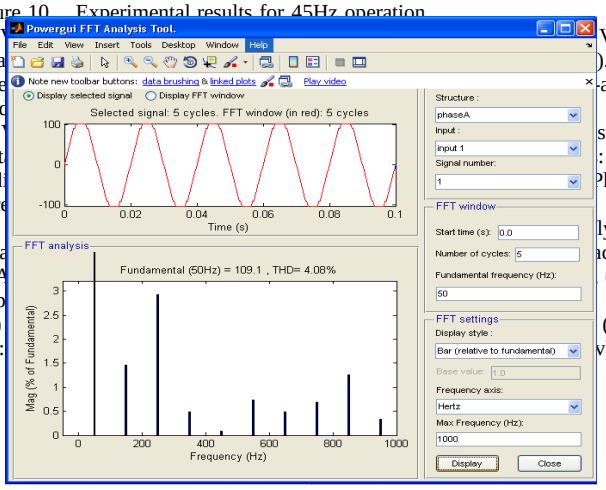


Figure 10. Experimental results for 45Hz operation



of the switching period, and voltage level 8 ($4V_{DC}/16$) for the remaining 20%. This is done independently for all three phases. Three phase voltage references are scaled to generate three PWM signals.

At any given instant, the voltage levels of the three phase uniquely identify the space vector to be applied ($\vec{V}_{eff}$). A lookup table is first used to determine the voltage vectors ($\vec{V}_1$ and $\vec{V}_2$) to be applied by the two inverters. Next, a second lookup table is used to determine the pole voltages for the two inverters. Finally, the switching state is determined and gate signals are generated for all switches.

V. Experimental Results

The proposed topology was validated experimentally with a 3φ, 440 Volt, 1.5 HP induction motor. The motor was operated at steady state over the entire linear modulation range with a V/f controller. A digital signal processor (DSP) (TMS320F28335) was used to implement the V/f controller and level shifted carrier PWM. The DSP was programmed to generate PWM signals for all three phases. Synchronous PWM was used over the entire modulation range to eliminate sub-harmonics from the phase voltage. The three phase currents, voltages of all nine floating capacitors, and DC link voltages were sensed using hall effect sensors and were sampled at the start of every switching cycle. This data was transmitted to a Field Programmable Gate Array (FPGA) (Spartan 3E XC3S200). The FPGA was programmed with the lookup tables required to determine the switching states based on the PWM signals, capacitor voltage states and phase currents. Dead time was implemented within the FPGA logic, enabling the FPGA to drive the insulated gate bipolar transistor (IGBT) gate drivers directly. Both inverters were powered by isolated rectifier power supplies.

The motor was run at no load at constant speed over the entire modulation range. The phase voltage $V_{AA'}$, three pole voltages V_{AO}, $V_{A''O'}$ and $V_{A'O'}$ were recorded along with the phase current I_A at each operating frequency. The ripple in voltages of capacitors C1A, C2A, and C3A was also recorded. Two controller outputs were also logged - the phase voltage reference and a binary signal digital to indicate whenever type-2 states were used.

For low modulation indices, inverter-1 does not switch at all (fig. 7). Inverter-1 begins to switch at slightly higher modulation index (fig. 8), although only in two level mode. Three-level operation of inverter-1 when the modulation index rises further (fig. 9). Finally, for operation at 45Hz, at the end of the linear modulation range, inverter-1 operates in three-level stepped mode, while the contribution of inverter-2 generates sinusoidal phase voltage. It can be seen that all capacitor voltages are well balanced to within a few volts over the entire operating range, even when the type-2 SVLs are traversed.

VI. Conclusion

A seventeen-level inverter topology is presented here for open end induction motor drives with just twelve switches per phase. The resulting space vector structure is hexagonal and consists of identical equilateral triangles. An efficient modulation scheme is also presented, requiring only instantaneous phase voltage references. By proper selection of switch states, all floating capacitor voltages can be kept well balanced over the entire modulation range, while also ensuring that neither inverter experiences DC bus overcharging due to reverse power flow. Experimental results show the effectiveness of the proposed topology and its suitability for applications such as industrial drives and electric traction.

References

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, and J. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug 2010.

[2] R. Teodorescu, F. Blaabjerg, J. Pedersen, E. Cengelci, and P. Enjeti, "Multilevel inverter by cascading industrial VSI," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 832–838, Aug 2002.

[3] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Perez, "A survey on cascaded multilevel inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, July 2010.

[4] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sept 1981.

[5] Y. Jiao, F. Lee, and S. Lu, "Space vector modulation for three-level NPC converter with neutral point voltage balance and switching loss reduction," IEEE Trans. Power Electron., vol. 29, no. 10, pp. 5579–5591, Oct 2014.

[6] T. Chaudhuri, A. Rufer, and P. Steimer, "The common cross-connected stage for the 5L ANPC medium voltage multilevel inverter," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2279–2286, July 2010.

[7] R. Sudharshan Kaarthik, K. Gopakumar, J. Mathew, and T. Undeland, "Medium-voltage drive for induction machine with multilevel dodecagonal voltage space vectors with symmetric triangles," IEEE Trans. Ind. Electron., vol. 62, no. 1, pp. 79–87, Jan 2015.

[8] G. Grandi, C. Rossi, A. Lega, and D. Casadei, "Multilevel operation of a dual two-level inverter with power balancing capability," in Conference Record of the 41st Industry Applications Conference,. 41st IAS Annual Meeting., vol. 2, Oct 2006, pp. 603–610.

[9] D. Casadei, G. Grandi, A. Lega, and C. Rossi, "Multilevel operation and input power balancing for a dual two-level inverter with insulated DC sources," IEEE Trans. Ind. Appl., vol. 44, no. 6, pp. 1815–1824, Nov 2008.

[10] K. Thakre and K. Mohanty, "Comparative analysis of THD for symmetrical and asymmetrical 17 level cascaded H-bridge inverter using carrier based PWM techniques," in Industrial Instrumentation and Control (ICIC), 2015 International Conference on, May 2015, pp. 306–310.

[11] P. Kumar, R. Kaarthik, K. Gopakumar, J. Leon, and L. Franquelo, "Seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-Bridges," IEEE Trans. Power Electron., vol. 30, no. 7, pp. 3471–3478, July 2015.

[12] J. Mathew, P. Rajeevan, K. Mathew, N. Azeez, and K. Gopakumar, "A multilevel inverter scheme with dodecagonal voltage space vectors based on flying capacitor topology for induction motor drives," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 516–525, Jan 2013.

[13] R. Kanchan, M. Baiju, K. Mohapatra, P. Ouseph, and K. Gopakumar, "Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages," IEE Proceedings on Electric Power Applications, vol. 152, no. 2, pp. 297–309, March 2005.