Design and Implementation of Floating-point Vedic multiplier

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Abstract— Critical role of any digital system is played by the multiplier. In mathematics, Veda provides one line, fastest processor along with fast cross-checking method. It is most important to implement faster multiplier occupying less area and consuming less power. VEDIC Mathematics is mathematical detail of 'Sixteen Simple Mathematical formula from the Vedas' as release by Sri Bharati Krishna Tirtha. The implementation of the Floating-point multiplier is done by using Vedic multiplication methods. For mantissa multiplication we are using Urdhvatriyakbhyam formula. The cases of underflow and overflow would be solved. The multiplier's input in 32bit IEEE 754 outlay. We implement these multipliers using VHDL. For simulation of our work Xilinx ISE tool i.e. amenable for synthesis tool is used and Modalism 10.2a is also used.

Keywords: Mathematics of Vedic, a formula of UrdhvaTriyakbhyam, Floating-Point multiplier, precision.

I. INTRODUCTION

This Floating-point operation is very important for computation involves huge dynamic areas, but they are demand especially more estate the whole numbers operation. The speedy promoted in area programmable gate array (FPGA) technic made like device progressively absorbing for implementing arithmetic of floating-point. This multiplier has moderate working in both speed and field. The basic function of binary floating-point numbers application applied in digital signal processing (DSP) application. IEEE 754 norm confers of outlay for characterization of Binary Floating-point numbers in computers.

The Binary Floating-Point is into two formats i.e.

i) Single-Precision

ii) Double Precision

Single Precision Representation -(32 bit) Double Precision Representation- (64 bit)

Fig No. :1 Binary floating points format

II. RELATED WORK

The format of the IEEE floating-point was a norm layout used in the whole technology essence since Binary floating-point numbers. Multiplication is a general gathering used in digital signal processing (DSP) petition. The floating-point multiplier's VHDL implementation using ancient Vedic. Urdhva Tiryakbhyam formula (system) was elected for execution so this is valid to whole matters of multiplication mathematics is offered. The representation of floating-point numbers in a binary sequence. The idea for tracing of multiplier unit is conditioned from the old Indian mathematics ".Urdhva Tiryakbhyam formula (system) was elected for execution since this is eligible for whole cases of multiplication. Two number's multiplication by using Urdhva Tiryakbhyam formula is worked by vertically and crosswise, crosswise appliance diagonal multiplication, and vertically appliance outright above multiplication and taking their sums. A multiplier is one of the execution hardware in most digital signal processing method better execution of any digital signal manipulation stop upon the better execution of the multiplier. The high-performance digital signal processor is the design of multiplier. It is also known as mathematical tools. The post floating pint is derivative from the meaning there is no switched number and digital after and before the decimal point that is decimal point can floating. There was representation

too in which the digital number before and after the decimal point is a grouped called switched point representation generally floating-point representation is slow and short actual then switch point representation but they can maintain the larger range's number. The floating-point number as display as a fractional portion. Modified of the Booth algorithm is one of the major plausible algorithms. Rounding the resulted number confer a calibration number's multiplication by manners IEEE rounding system.

III. LITERATURE REVIEW

Sushma S. Mahakalkar et al, they operated on the primeval and the cores of whole the DSPs are its multipliers and the DSPs speed is mainly composed by the fast of its multiplier. The IEEE floating-point format was a norm outlay applied in whole processing elements so Binary floating-point numbers multiplication is one of the general gatherings applied in DSP petition. In that work VHDL execution of Floating-Point Multiplier applying old Vedic mathematics is presented. The designing of the multiplier system is adoptive from ancient Indian mathematics "Vedas". The Urdhva Tiryakbhyam formula (system) is elected for execution so this is eligible to the whole concern of multiplication. Two no's multiplication using Urdhva Tiryakbhyam formula is operated by vertically and crosswise, crosswise means diagonal multiplication and vertically appliance outright above multiplication and taking their addition. A trait is any multi-bit multiplication can be diminished down to single bit multiplication and sum applying this system. On account of these methods, the carry propagation from LSB to MSB is less due to one step descent of fractional product [1].

They get that the effective application of the Vedic multiplication technique to produce two floating-point numbers. This function represents the execution of a floating-point multiplier that helps the IEEE 754-2008 binary interchange outlay. The discussion-based made above it is clear that a multiplier is a most crucial element in any processor design and a processor past satiety amount of time in functioning multiplication and simply the most field reducing. Therefore, improving the fast and field of the multiplier is a large outlay design mark. A reform in multiplication fast by using a recent method can greatly reform system working. This project can be forwarded for the reconfigurable tectonics [1].

Aritra Mitra et al proposed a Vedic Multiplication technique that applied to the executive Floating-point multiplier. The Urdhvatriyakbhyam formula will be applied as a multiplication of Mantissa. The overflow and underflow matters would be handled. The multiplier's input in 32bit format. The multiplier is constructed in VHDL or VERILOG and simulated using Modalism.

They reduce that the multiplier system has been constructed. The design of the project in the forward stage would be constructed using VHDL or VERILOG and will be perceptible using Modalism Simulator. The construction would be synthesized applying Xilinx ISE 12.1 tool. A bench of the test would be used to produce the stimulus and the multiplier gathering is to be tested. Over-flow and milder flow flags are to incorporate in the construction to display the overflow and underflow concern. This theory said that the effective use of the Vedic multiplication technique to multiply two floating-point numbers. That hardware needed is shattered, thereby shattering the power decrease. The power decrease upon shattering effectively may not deal with a delay so much [3].

BHAGYASHREE HARDIYA et al operated on floating-point number's multiplication stated in IEEE 754 single-precision recognized. The floating-point multiplier is done by applying VHDL. Implementation in VHDL (VHSIC Hardware Description Language) is applied because it free of making apparent execution on the hardware while in other languages they have to change them into HDL then only can be implementation on the hardware. In floating-point multiplication, two number's adding is done with the need for different types of adders but for production with some advance shifting is needed. This floating-point multiplication solved different situations such as underflow normalization, overflow, rounding. In this function, they use the IEEE rounding technique for the execution of the rounding of the resulted number. This work scrutiny the execution of an IEEE 754 single-precision floating-point multiplier solved with the help of a lot of investigations. Finally they have viewed that the multipliers play a crucial preface in today's DSP and different other petition. With promoted in technique, a lot of investigations have tried and slapping to design multipliers which offer either of the following creation targets – fast speed, consumption of less power, layout regularity and hence low field or even conjunction of them in one multiplier thus making them appropriate for different fast speed, less power and firm VLSI execution. By applying serial to parallel Booth multiplier they view that in parallel multipliers partial product number to be added is the chief parameter that judges multiplier performs. To reduce partial product numbers to be added, the Modified of the Booth algorithm is one of the majority of plausible algorithms. Resulted in rounding number confers calibration production numbers by applying the IEEE rounding technique [4].

Remadevi proposed an algorithm for multiplying floating-point numbers which were a delicate need for DSP petition including a huge dynamic range. This work focuses only on single accuracy normalized binary interchange outlay targeted for Xilinx Spartan-3 FPGA based on VHDL. The multiplier was tested against Xilinx floating-point multiplier core. It maintains underflow and overflow cases. Rounding is not execution give more calibrated when using the multiplier in a Multiply and Accumulate (MAC) ace. They receive that the current function design and simulation of a floating-point multiplier that adherence the IEEE 754-2008 binary interchange sequence, proposed of multiplier doesn't execution rounding and extant the significant multiplication result like is (48 bits), this gives better accurate if all 48 bits are used of in another ace; i.e. With a floating-point adder to aspect a MAC unit. But the generated of floating-point multiplier core by Xilinx core generator doesn't imply the entire 48 bits of mantissa proper to rounding and is not beneficial in DSP application case of big dynamic particularly when using it in another high calibrated floating-point units such as Multiply and Accumulate (MAC) unit[6].

Dinesh Kumar et al operated on floating-point numbers they are successive used for numerical computation in a reputing method for better calibrate, but floating-point functions are complicated and hard to design on FPGAs. This work tries to create like -the architecture of hardware for single-precision calibration floating-point multiplication that is simply implementable with advanced efficiency. The multiplier unit is optimal on the old Vedic mathematics system. The introduced design is developed using VHDL which is seeming using Modalism SE 5.7f and especially using ISE Xilinx 10.1i on FPGA device Vertex -XC4VSX25-12FF668. Logic use shows that the use of slices is 1% and of 4-input LUTs is 21%. Also logic divided hint that many occupied portions are 2358 which are completely respective e[7].

They execution single precision floating point multiplier is formation using the old Vedic mathematics system. The algorithm is executed using ISE Xilinx 10.1i on FPGA device Vertex -XC4VSX25-12FF668 and pretense are entire by using Modalism SE 5.7f. The agglutination results present that number of portions applied is 154 out of 20480 with the use of 1%. Logic divided present occupied utilization portion is 23% and the overall number of 4inpur LUTs applied is 4470 out of 20480. The timing essence implies overall time contracted for the procedure is 32.730 ns (11.651ns for calculation, and 21.079 ns for communication) and several components applied are also present. The double calibration multiplier must be formed as an explication of this work. Also they can apply the Nikhlam formula (another method of Vedic mathematics) and weigh the results. They could also creation matrix multiplier and weigh speed and operations area [7]. decimal floating-point sequence. Execution results are associated with a broad spectrum of manipulation, presenting promise that our approach is practicable for a petition that needs decimal floating-point calculations. This work fills sooner publicity [19].

They incidental few mathematical talent and algorithms used in the first execution in the software of the IEEE 754R decimal arithmetic of floating-point rooted on the BID encoding. These concentrated on the issue of rounding properly decimal values that are contained in binary sequence while using binary manipulation effectively and also shown briefly other important or interesting algorithms applied in the library implementation. Finally, these handy a broad performance's sample numbers that demonstrate that the eventual exacerbation of hardware execution over software may not be as salutatory as beforehand ejective. The execution was condescending via testing against context magnificence implemented freely, which applied, in little concern, existing multiprocessing arithmetic magnificence. As they aspect by the future, they need ahead reformation in execution via algorithm and code optimizations, like good as increased functionality, for example, via the addition of transcendental execution help. Furthermore, they presume that hardware help can be added incrementally to renovate decimal floating-point execution as a request for its increase.

IV. PROBLEM FORMULATION

IEEE 754 task confer the sequence for characterization of Binary Floating point. The represented binary floating-point number in Single and Double sequences. Single has 32 bits and double has 64 bits. They are sequences &3 fields composed: Exponent, Sign, and Mantissa presenting the fabrication of Single and Double sequences of the IEEE 754 task. In the content of Single, the represented of Mantissa is in 23 bits and MSB added 1-bit standardization, represented of an exponent is in 8 bits which are inclined to 127, in fact the Exponent is represented in spare 127-bit sequences and MSB of Single is darn for the Sign bit. When sign bit is 1 that appliance the number is negative (-) and when the sign bit is 0 that appliance the number is positive (+). In 64 bits sequence the represented of Mantissa is in 52 bits, represented of Exponent is 11 bits which are inclined to 1023 and Double MSB is contained for the sign bit.

V. OBJECTIVES

In this paper we worked on the sublimate speed deign Vedic Multiplier applying the method of old Indian Vedic Mathematics that has been improved for renovating execution. Vedic Multiplication method is applied to implement IEEE 754 Floating point multiplier for mantissa multiplication we are applying Urdhvatriyakbhyam formula for the over-flow and underflow regard are maintained. Inputs of multipliers are provided in IEEE 754, 32-bit sequences. Vedic Mathematics is the old system of mathematics technique that has a masterly method of enumeration rooted in 16 Sutras Urdhva Triyagbhya. This technique is a classical technique for solving of floating-point multiplier and objects the accurate value.

VI. METHODOLOGY

The mantissa performance calculation unit dominates all execution of the floating-point multiplier. Require of malformed multiplier for multiplication of 24*24 bit. The technique for multiplication of twos,3 Bit. This technique provides a hopeful result in speed terms and energy. This multiplier is structured in VHDL or VERILOG and simulated using Modellism. The techniques for multiplication of two, the number of 3 bits is represented figure 2.0 regard the number X and Y where X=a2a1a0, Y=b2b1bo. The A LSB is multiplied with LSB of

B; s0 =a0 b0;

The multiplied of a0 with b1 and multiplied of b0 with a1 and then result are added in concert a

c1 s1 =a1 b0+a0b1;

So carry is c1 and the sum is s1. Sum c1 is the next step with the multiplication a0 result with b2 with b2, a1 with b1 and a2 with b0.

C2 s2 = c1 + a2 b0 + a1 b1 + a0 b2;

Add c3 is the next step with the multiplication results of a1 with b2 and a2 with b1.

C3 s3 = c2 + a1 b2 +a2 b1;

Similarly last step

c4 s4 = c3 + a2 b2;

Now the multiplication final result of X &Y

is c4s4s3s2s1s0.

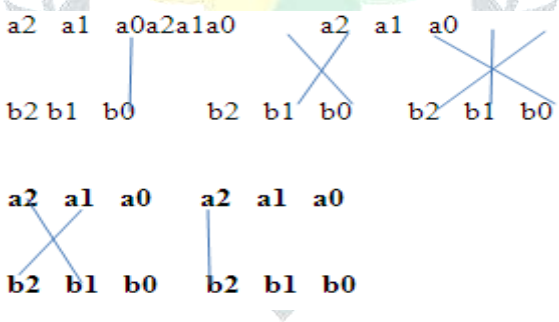

Fig. No.: 2 Implementation result

VII. CONCLUSION

Vedic' word is made from the word 'Veda' i.e. the store-house of the whole knowing. Mathematics, derivate from the Veda confers one line, mental and super-fast technique along with fast crosses checking technique. Mathematic of Vedic was rediscovered in the soon twentieth century from old Indian sculptures (Vedas). What we invoke VEDIC MATHEMATICS is a function of the mathematical spread of 'Sixteen Simple Mathematical sutras from the Vedas' as release by Sri Bharati Krishna Tirthaji. The Vedic Multiplication method would be applied to an appliance for a floating-point multiplier. To multiplication of mantissa, we are applying Urdhvatriyakbhyam formula. The overflow and underflow concern would be solved. Inputs to the multiplier is in the 32-bit IEEE 754 sequence.

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