R/W Operation & Performance Analysis of 4T & 6T SRAM

Rajkumar Sarma*

VLSI Design, SEEE, Lovely Professional University, Phagwara, Punjab,

rajkumar.16886@lpu.co.in

Abstract*: A detailed analysis on different approaches of designing sense amplifier is discussed in this paper. 4T & 6T SRAM cells are implemented in cadence virtuoso 90 nm CMOS technology along with differential and current mirror sense amplifiers. The result suggests that the Current Mirror Sense Amplifier (CMSA) is better option in terms area along with high speed although at the cost of 50 % more power consumption than Differential Sense Amplifier (DSA).

Keywords: Current Mirror, CMOS, SRAM, Cadence Virtuoso

I. INTRODUCTION

SRAM is a memory unit to store data. As its name indicates, it stores till the power supply is on [6]. Unlike DRAM does not require periodic refreshments and it uses two inverters to store data and a sense amplifier for the retrieval of data when it is necessary. Power consumption of SRAM depends upon many factors but the most important one is that "how many times the bit line is accessed in a cycle".

Each SRAM cell is made up of 4 transistors used to store data, which are basically two cross coupled inverter circuits. These inverter circuits have two stable states either '0' or '1'. Two more transistors are used to access the data during read and write operation. It has three modes of operation named as hold, read and write operations.

A. Pre-charge Circuit

The pre-charge circuit has only one use in SRAM. The function of SRAM circuit is to charge the BL and BLB to vdd=1.8 volts. With the help of pre-charge circuit SRAM keeps the BL and BLB all the times high except during read and write operation. The width used for PMOS is 2.4u and length used is equals 180n.

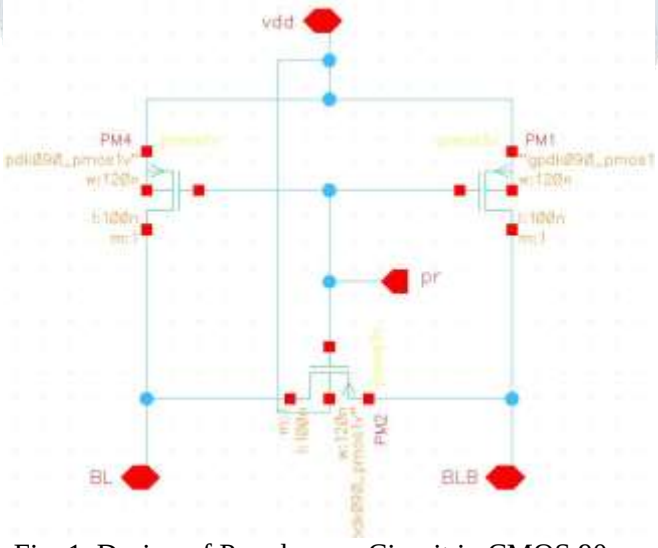

Fig. 1. Design of Pre-chanrge Circuit in CMOS 90nm

B. Write Driver Circuit

It starts with data to be written on bit lines. Suppose to write '0' then '0' must be applied to BL and its complement to BLB. In write operation two not gates are connected back to back whose output worked for controlling voltage of two NMOS transistors which further attached to two access transistors for write enable pin. When both the pins get high it performs the write operation.

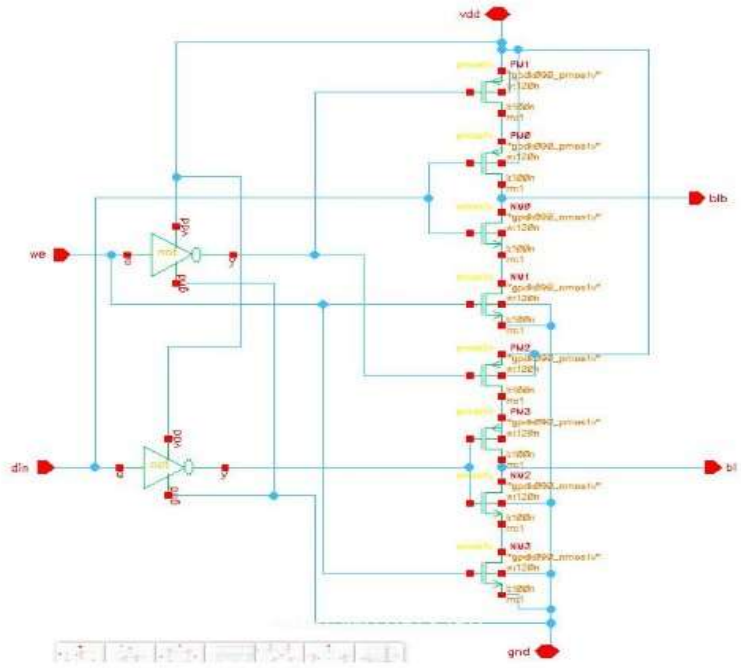

Fig. 2. Design of Write Driver Circuit in CMOS 90nm

C. Single Bit Memory Cell using 6T

It comprises of SRAM cell, pre-charge circuit, write driver circuit, sense amplifier and column select. The complete schematic is shown below. This schematic shows all the different peripherals circuit combined with SRAM cell, to form a complete SRAM read and write operation. The input signals are WE that allows the writing operation, SE that allows reading from SRAM cell & WL that allows to decide from which address data will be written or read & the signal data either 0 or 1 is to be stored or read from the cell.

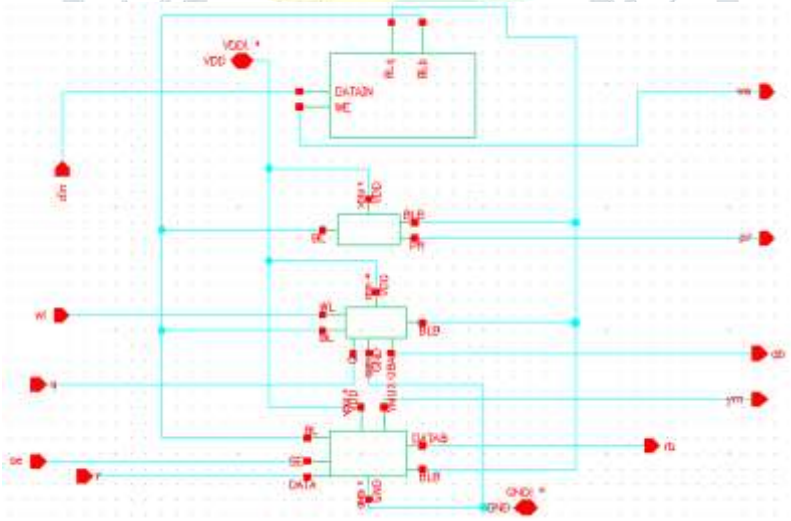

Fig. 3. Design of Single Bit Memory Cell using 6T in CMOS 90nm

II. POWER, DELAY & AREA ANALYSIS OF 4T & 6T SRAM CELLS

Using this 4T SRAM memory system area consumption is significantly reduced by an amount of 40% as compare to existing 6T SRAM as shown in table-I. Power dissipation is a component to think in 4T SRAM (as shown in table II & III) about since it dissipates 50% more power than conventional 6T.

Table- I: Area calculation of 6T & 4T

Serial	Type of SRAM	Area
1	4T Cell	94.14
2	6T Cell	154.17

Table- II: PDP calculation of 4T

Supply voltage	Delay (ns)		Power dissipation(µW)	PDP
	Read	Write		
0.5 V	25.11	0.34	1.23	0.031×10^{18}
1 V	20.30	0.193	19.56	0.400×10^{18}
1.5 V	20.01	0.183	65.15	1.315×10^{18}
2 V	19.90	0.113	145.5	2.911×10^{18}

Table- III: PDP calculation of 6T

Supply voltage	Delay (ns)		Power dissipation(µW)	PDP
	Read	Write		
0.5 V	5.082	0.173	0.215	1.12×10^{15}
1 V	0.335	0.162	3.13	1.53×10^{15}
1.5 V	0.210	0.151	11.71	4.22×10^{15}
2 V	0.145	0.133	142.1	39.5×10^{15}

Fewer transistors will always be welcomed in designing high density SRAM arrays. In 4T data and their compliment has been held on each node unlike in 6T where two coupled inverters are used to hold the single bit data. On the basis of above results one can clearly say that 4T saves around 40% area to perform the same operation but at cost of 60 % extra power dissipation.

III. PERFORMANCE ANALYSIS OF DIFFERENT SENSE AMPLIFIERS

Table- IV: Delay calculation of DSA & CMSA

V_{DD}	Delay (ns)	
	DSA	CMSA
0.5 V	3.22	0.68
1 V	0.361	0.064
1.2 V	0.316	0.084
1.5 V	0.257	0.027
1.8 V	0.226	0.013
2 V	0.116	0.010

Table- V: Power Calculation of DSA & CMSA

V_{DD}	Power Dissipation (µW)	
	DSA	CMSA
0.5 V	1.365	2.01
1 V	27.94	29.9
1.2 V	53.15	55.27
1.5 V	60.75	112.1
1.8 V	103.6	198.9
2 V	140.01	277.7

Table- VI: Area Calculation of DSA & CMSA

Serial no.	Type of Sense Amplifier	Area (mm^2)
1	DSA	187.42
2	CMSA	112.03

As it is visible from table-IV that as the power supply get increased the delay gets reduced and power dissipation increases. Now on the basis of the analysis it is clearly visible that at 1V supply voltage, CMSA delay is 0.064 ns while DSA delay is 3.22 ns. The delay of CMSA circuit is 82.3 % lesser than that of DSA circuit. That means CMSA has better speed than conventional DSA.
Table-V shows the power dissipation by both kind of sense amplifiers. Clearly DSA has less power dissipation than CMSA. For 2V supply voltage it consumes almost 50 % less power than CMSA. As per area regard CMSA saves almost 40 % area as compared to DSA (table-VI).

IV. CONCLUSION & FUTURE SCOPE

A detailed analysis on different approaches of designing sense amplifier is discussed in this paper. 4T & 6T SRAM cells are implemented in cadence virtuoso 90 nm CMOS technology along with differential and current mirror sense amplifiers. On the basis of these three important parameters it can be concluded that CMSA is better option in terms area along with high speed although at the cost of 50 % more power consumption.

In coming future there is a lot of work can be done in the field of SRAM in terms of designing SRAM cell with reduced number of transistors with ultralow power dissipation. The feasibility of 2T and single transistor SRAM cells can also be evaluated as it can highly improve the density of SRAM array which is a major problem in present day. Also, one can work on making fast sense amplifiers which contribute to less delay and speed up the performance of the SRAM system.

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