# Selective Harmonic Elimination based THD Minimization of a symmetric 9- Level Inverter using Ant Colony Optimization

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***Abstract***

A new topology of a symmetric single-phase multilevel inverter with the less number of semiconductor switches and optimized low-frequency control methods to optimize the Total Harmonic Distortion is proposed in this paper. A nine level single phase output is obtained by eight numbers of active semiconductor switches, four diodes and four capacitors from two symmetrical dc sources. The selected harmonic order in the output voltage is eliminated by the PWM (SHE-PWM) based on selective harmonic elimination. To optimize the switching angles, an ant colony optimization is applied. The proposed SHE-PWM and ant optimization are implemented and tested for THD on the SIMULINK platform. The proposed approach offers less THD and is best suited to high-power applications with medium voltage.

***Keywords:*** *THD, SHE-PWM, ACO, Multi- Level Inverter.*

## 1. Introduction

Inverter is a system that converts the DC to AC with acceptable voltage and output frequency. Inverters have some inherent issues of lower efficiency, high dv/dt, higher power losses and large THD [1]. A multi-level inverter is designed to solve these issues. With a three-level converter, the word Multilevel has begun, the cascaded multilevel inverter is currently in use [2]. The output of the multi-level inverter has lower harmonics than the normal output voltage of the bipolar inverter. Multilevel inverters are mainly known as a clamped diode, Flying condenser, and cascaded MLI [2- 3]. The control scheme of cascaded MLI is simple compared to other MLIs, since a clamping diode and a flying condenser are not needed [5]. For more than three decades, multi-level inverters are under research and development, and successful industrial applications have been discovered [4-5]. Nonetheless, this is still an emerging technology, and many fresh developments have been reported in recent years [6]–[8]. Multilevel inverters have drawn growing interest, with the key reasons being: increasing power levels, improved harmonic performance and reduced emissions of electromagnetic interference (EMI) that can be preserved with several dc stages synthesizing the output voltage waveform [7]. In systems like industrial variable-voltage drives, EVs and photovoltaic networks connected to the grid. The ongoing work offers an alternative to the design of an effective multi-level topology for high and medium-power applications.

Advanced Multi-level inverters now use fewer components and smaller carrier signals as compared with traditional multi-level inverters. A composite topology is presented in this paper having separate level generating part and polarity generating parts [8]. To increase the output of multilevel inverters in hybrid topology, first positive rates are produced with high-frequency switches and then the voltage portion is reversed with low-frequency switches. As a result, the control circuit complexity for higher levels is significantly reduced. Selective harmonic pulse width modulation (SHE-PWM) technique with Ant Colony optimization has been used to simulate a single phase 9-level hybrid inverter. The inverter performance is evaluated with regard to harmonic distortion (THD) [9-10]. The harmonic distortion generated by the proposed inverter is significantly lower, around 5% by the results obtained from simulation.

## 2. Proposed Symmetric Inverter Topology

The proposed inverter's schematic design is shown in figure (1), which consists of two modules, namely a module for level generation and a module for voltage reversal / polarity generation. Polarity generation module is an H-bridge that reverses the polarity of output for each half cycle of operation, where as the level generating module will generate higher levels from the dc sources that can extend up to ' n '

levels. Symmetric dc sources are used for the inverter input, where each source is divided into two equal parts by using similar condensers to increase the higher output level from less dc sources. A MOSFET is used for the circuit design and the diodes used in the circuit to prevent the short circuit of the sources.

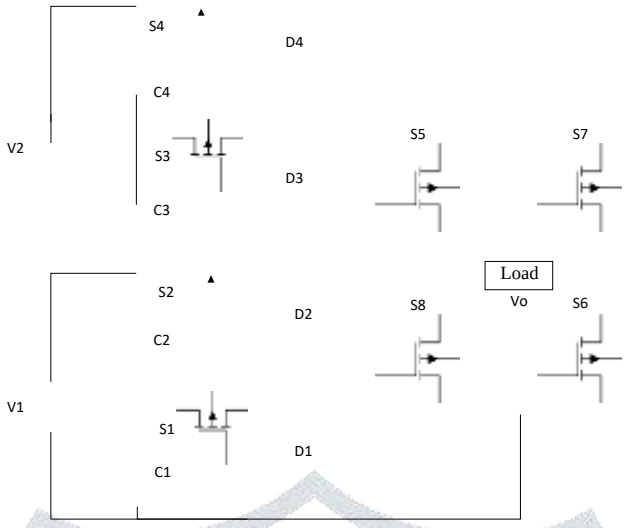


Figure (1): Proposed Symmetric 9-Level Inverter

Relation between the components used in the circuit design given as follows; No. of capacitors ($N_c$) = 2 $N_v$, Where $N_v$ = No. of voltage sources No. of Switches ($N_s$) = $N_c$ + 4

No. of diodes ($N_d$) = $N_c$

No. of levels ($N_{step}$) = 2$N_c$ + 1

There are nine modes of operation of this inverter to achieve the required 9-level output Vo; the first four modes of operation give the positive levels of voltages, V/2, V, 3V/2, 2V and next four modes of operation give the negative levels of voltages, -V/2, -V, -3V/2, -2V and ninth mode gives the output '0V'is obtained by switching sequence mentioned in table (I).

Table 1: Switching Sequence of the all modes of operations

| Mode | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | O/P Voltage |
|---|---|---|---|---|---|---|---|---|---|
| I | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | **V/2** |
| II | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | **V** |
| III | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | **(3/2)V** |
| IV | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | **2V** |
| V | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | **-V/2** |
| VI | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | **-V** |
| VII | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | **-(3/2)V** |
| VIII | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | **-2V** |
| IX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0** |

## 3. Selective Harmonic Elimination based control of proposed inverter

This paper proposed a SHE-PWM to reduce the dominant harmonics of lower order and the switching losses in the proposed hybrid multi level inverter [11]. A synthesized near sinusoidal output expected to obtain from the 9-level output is shown in fig. 2.

**(a) Selective Harmonic Elimination-PWM**

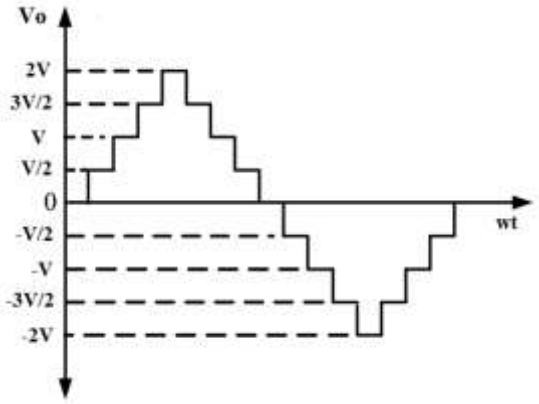


Figure 2: Proposed 9-Level synthesized near sinusoidal waveform

For the above 9- level wave form the four switching angles $\theta_1$ ,$\theta_2$ ,$\theta_3$ ,$\theta_4$ need to be generate. By considering the characteristics of the waveform, these switching angles are the function of Fourier series expression and expressed as (1)

$$V_0 = \sum_{k=1}^{\infty} \frac{4V_{dc}}{k\pi}(\cos k\theta + \cos k\theta_2 + + \cos k\theta_n)^* \sin k\omega t \qquad (1)$$

The necessary constraint the to be satisfied the switching angles from $\theta_1$ to $\theta_n$ is

$$0 \le \theta_1 < \theta_2 < \theta_3 < \theta_4 ..... < \theta_n \le \frac{\pi}{2} \qquad (2)$$

Thus with an inverter of nine levels with two DC outputs, the 5th, 7th, and 11th harmonics must be removed, and the transcendental equations to be satisfied are as follows.

$$V_1 = \cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \cos\theta_4 = MI$$
$$V_5 = \cos 5\theta_1 + \cos 5\theta_2 + \cos 5\theta_3 + \cos 5\theta_4 = 0$$
$$V_7 = \cos 7\theta_1 + \cos 7\theta_2 + \cos 7\theta_3 + \cos 7\theta_4 = 0$$
$$V_{11} = \cos 11\theta_1 + \cos 11\theta_2 + \cos 11\theta_3 + \cos 11\theta_4 = 0$$

For optimum switching angles, modulation index (MI) is;

$$MI = \frac{V_1}{\frac{16V_{dc}}{\pi}} \; for \; 0 \le MI \le 1 \qquad (3)$$

The magnitude of the harmonics depends on the angles of switching. To accomplish the above objectives the fitness function (FF) takes the form as follows:

$$FF = 100 * \frac{(V_{1d} - V_1)^4}{V_{1d}^4} + \left(\frac{50}{V_1}\right)^2 * \left(\frac{V_5^2}{5} + \frac{V_7^2}{7} + \frac{V_{11}^2}{11}\right) \qquad (4)$$

**(b) ANT Optimization of SHE-PWM**

Ant optimization (ACO) is the first to investigate an optimal path in an evo utionary-based on ant's behavior to find a path between their colony and food source. Flow chart shown in fig. 3 explains the step by step procedure to be followed to implement the Ant colony optimization algorithm [11-12]

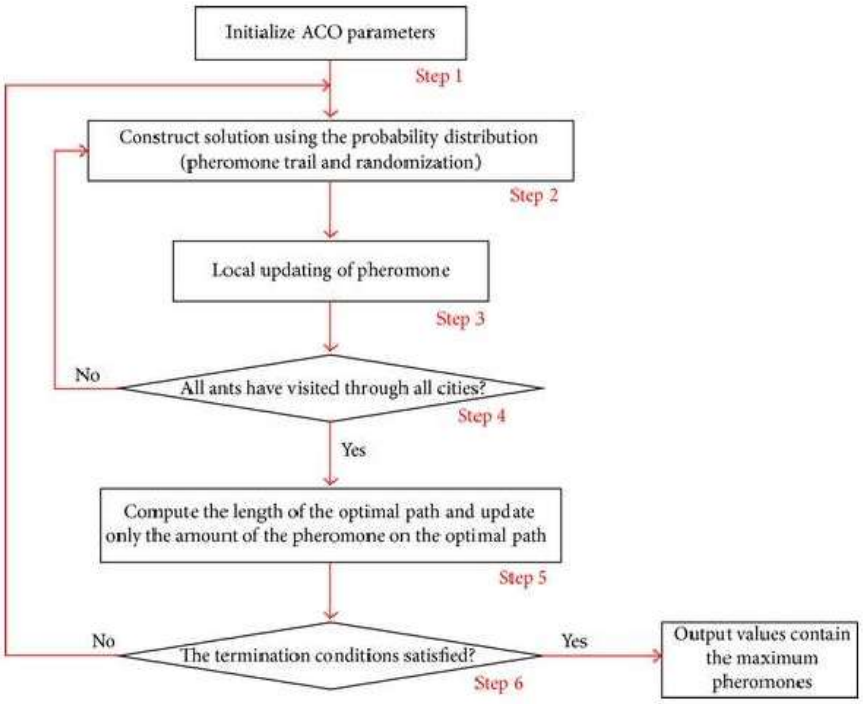


Figure 3: A flow chart for Ant colony optimization

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## 4. Results and Discussions:

The variance in the number of dc sources needed to model the proposed inverter for different output voltage levels is shown in the fig. 4.

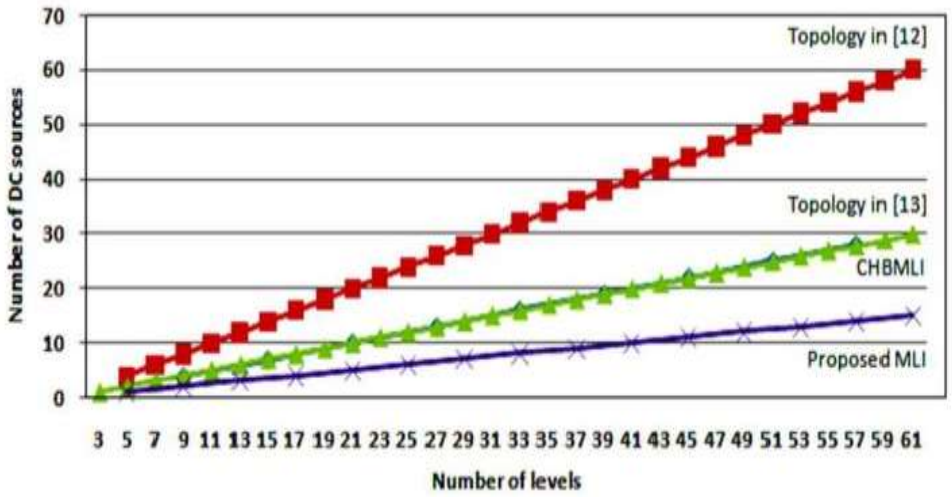


Figure 4: Comparison for number of DC sources

The Switching angles obtained from the Ant colony optimization algorithm. are $9.46^0$, $19.65^0$, $36.92^0$ and $59.45^0$ giving a THD of 5.60% The obtained voltage waveform is shown in fig 5.

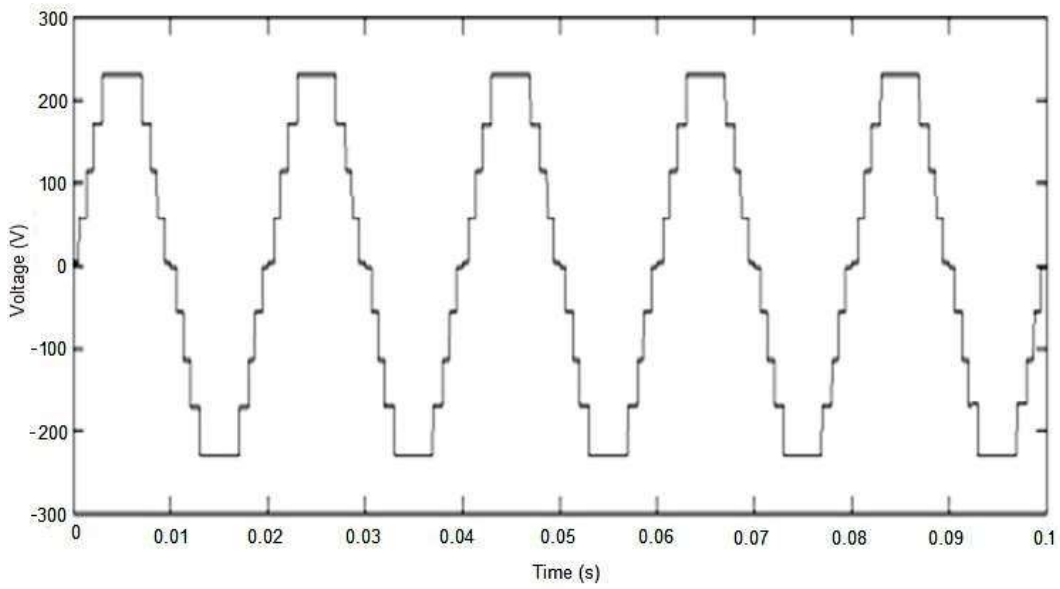


Figure 5: 9-Level load waveform of proposed inverter

## 4. Conclusions

This paper presented a novel symmetric inverter with reduced switches for a nine level inverter using MATLAB®SIMULINK. To optimize the switching angles of the multi-level inverter, a low frequency switching modulation called SHE-PWM is used to reduce switching losses and THD. In addition, less THD is achieved by adopting the Ant Colony Optimization technique. The output voltage obtained is approximately a sinusoidal wave. The inverter output voltage indicates lower THD. The suggested inverter is compliant with different single-phase applications.

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