

# Performance Analysis of XOR and XNOR Gates Using Different Logic Styles

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**Abstract**—Adder circuit is basic part of arithmetic circuits and also Application Specific Integrated Circuits (ASIC). Combination of unique logic styles are used to implement adder circuits. Performance analysis of these circuits is measured worst-case delay, power dissipation and Power Delay Product (PDP). Performance of these circuits is dependent on XOR and XNOR circuits. In this unit, XOR and XNOR implemented using PTL, CPL cross coupled and PTL cross coupled logic styles. The performance analysis of XOR and XNOR circuit is done using Mentor Graphics EDA tool at 130nm technology operating at 1.2V supply voltage and frequency of 1GHz. PTL cross coupled style is having lowest power of 3.42nW; The PTL circuit2 and CPL cross coupled has got lowest worst-case delay for XOR as 9.11ps and XNOR as 17.58ps, respectively and PTL circuit2 is lowest PDP of 0.07aJ.

**Keywords**—Pass Transistor Logic (PTL), Complementary Pass Transistor Logic (CPL), Complementary Metal Oxide Semiconductor (CMOS), Transmission Gate (TG), XOR-XNOR circuit.

## I. INTRODUCTION

Nowadays lightweight, battery related electronic devices are most popular such as mobile phones, laptops, notebook and smart watches. These types of electronic systems contain arithmetic circuits. The adder is a main building block of Arithmetic Logic Unit (ALU) which is part of processor. Adder circuits are designed using XOR and XNOR gates. XOR and XNOR can be designed using unique logic styles like CMOS, CPL, PTL and TG.

Complementary Metal Oxide Semiconductor (CMOS) logic style XOR circuit is designed with 12 (6 PMOS and 6 NMOS) transistors [17] as shown in Fig. 1. Add one extra inverter to XOR circuit to get the XNOR output. It contains pull up and pull-down networks are handled by input signals. Pull up network involves p-channel transistors and this network connected to supply voltage. The pull-down network involves n channel transistors and this is connected to ground. In the circuit either pulls up or pull-down network is ON. The main advantage of CMOS logic style is full output voltage and good noise margin.

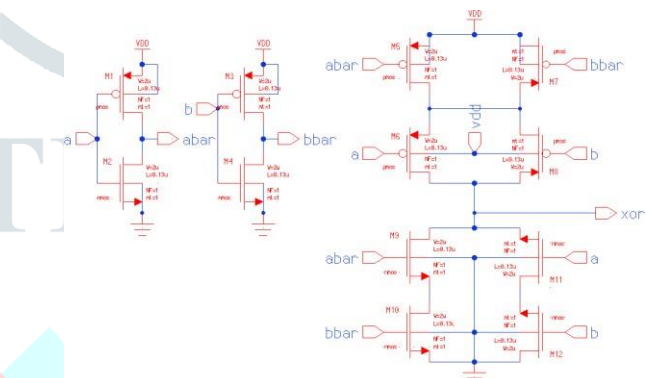


Fig. 1. CMOS based XOR circuit.

Complementary Pass Transistor Logic (CPL) is one of the new styles to implementing logic gates that uses transmission gates combines of both NMOS and PMOS pass transistors. CPL based XOR circuit is designed using 14 transistors, this logic is better than the CMOS logic design in terms of delay and power [17] as shown in Fig. 2. Add one extra inverter to XOR circuit to get the XNOR output. CPL logic is commonly used in multiplexers and latches. The main advantage of CPL is easy to design the circuit, it consumes less area and it requires less number of transistors compare to CMOS logic.

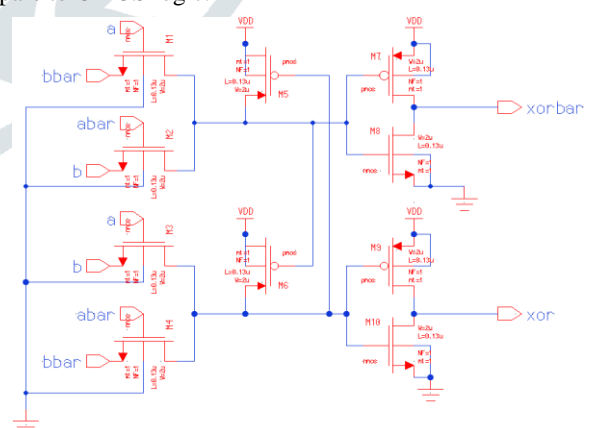


Fig. 2. CPL based XOR circuit.

Pass Transistor Logic (PTL) based XOR and XNOR circuit is designed with 6 transistors as shown in Fig. 3. PTL is mostly used in Integrated Circuit (IC) to decrease the more number of transistors are utilized to design unique logic gates [16]. PTL is used as a switch to pass the binary logic levels between nodes of a circuit. The main advantage is to reduce the area and it requires less number of transistors compare to CMOS logic. The main disadvantage of PTL is threshold voltage drop in transistor. It is one of the CMOS based switch, in which PMOS passes a strong 1 but poor 0, and NMOS passes strong 0 but poor 1.

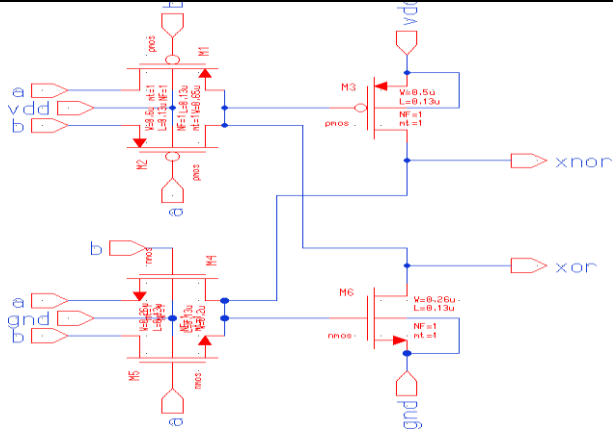


Fig. 3. PTL based XOR and XNOR circuit.

Transmission Gate (TG) is an electronic component and great non-mechanical relay built with CMOS innovation. It is bidirectional switch to conduct in both directions and block by a control signal with different voltage. It is made through parallel combination of NMOS and PMOS transistors and the drain and source terminals are connected together, TG based XOR circuit is designed with 8 transistors [1] as shown Fig. 4. Add one extra inverter to XOR circuit to get the XNOR output. The main advantage is to reduce the noise margin and also increase the chargeable resistance and power.

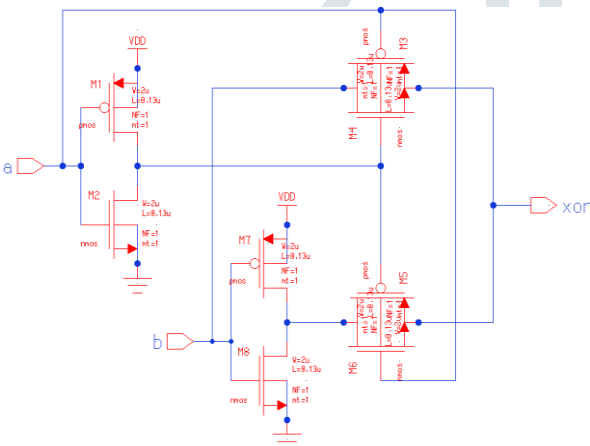


Fig. 4. TG based XOR circuit.

Several publishers have presented about the full adder with different type of logic styles. Multiplexer based one-bit full adder is designed using total 12-transistors, this circuit called as MBA-12T adder. This MBA-12T adder circuit analyzed with the complementary CMOS adder circuit i.e. 28-transistor at HSPICE [3]. Full adder circuit developed by split pre-charge data driven dynamic logic (sp-D3L) [7] and it is used to realizing high performance, power efficient full adder. Full adder using GDI (Gate-Diffusion Input) structure and hybrid CMOS logic style [8]. The main intent of this design is not only providing Low-Power dissipation and high speed but also full output voltage. One of the papers presents MOSFET-like CNFETs to develop 1-bit full adder cells [11]. Spin Hall Effect based 1-bit full adder [12] used to know the delay and power consumption of an n-bit SHE-based adder. The latest logic style used to design full adder is hybrid logic styles [5], [9-10], [13], [16].

## II. XOR AND XNOR CIRCUIT

### A. CPL cross coupled XOR and XNOR circuit

In this circuit, implemented using 10 transistors with CPL based cross coupled logic design [15] as shown in Fig. 5. Left hand side is the XOR circuit and right side is XNOR. At the XOR output side using 2 PMOS (M1 and M2) and 3 NMOS (M3, M4 and M5) transistors, M1 and M2 transistors are associated in parallel shape of PTL, also M3 and M4 are connected in series used as a restorer it gives a full output voltage of XOR and M5 is feedback transistor. At the XNOR output using 2 NMOS (M9 and M10) and 3 PMOS (M6, M7 and M8) transistors, M9 and M10 transistors are associated in parallel form of PTL, M7 and M8 are connected in series used as a restorer it gives a complete output voltage of the XNOR and M6 is feedback transistor.

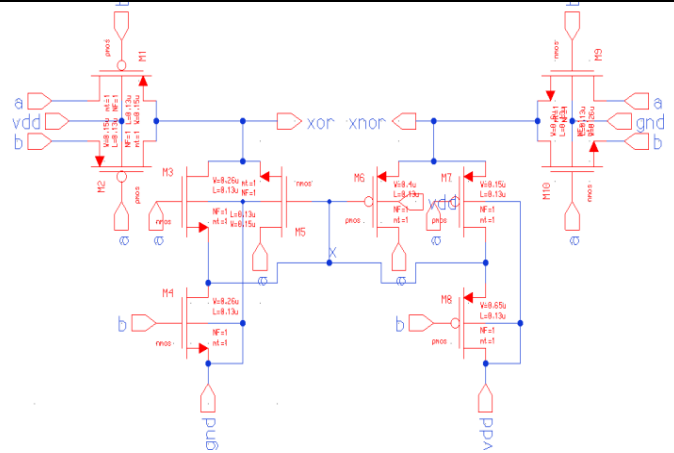


Fig. 5. CPL cross coupled XOR and XNOR circuit.

The input AB in 00 conditions, M1, M2, M7 and M8 transistors are turn ON. M1 and M2 transistors are passing low logic 0 because of negative PMOS threshold voltage (-Vthp) at XOR output, whereas M7 and M8 transistors are connected to Vdd passing high logic 1 at XNOR output and internal node X. The transistor M5 turns ON with respect to internal node X and it passes logic 0 at XOR output. Input AB in 01 condition, the transistors M2, M9 and M7 turns ON. Transistor M2 passes the logic 1 and M9 passes the logic 0 at XOR and XNOR output, and the transistor M7 passes logic 0 at node X to switch ON transistor M6 and it passes logic 0 (-Vthp) at XNOR output. For input AB in 10 conditions, transistors M1, M10 and M3 turn ON and transistors M1 and M10 are passes logic 1 and logic 0 at XOR and XNOR output, transistor M3 passes logic 1 at internal node X to switch ON transistor M5, which passes logic 1 (Vdd-Vthn) at XOR output. The input AB in 11 condition, transistors M9 and M10 passes logic 1 (Vdd-Vthn) at XNOR output. Similarly, XOR output thoroughly discharged via transistor M3 and M4 and passes logic 0 at internal node X to switch ON the M6 transistor and it passes logic 1 at XNOR output.

1) RC delay models of XOR and XNOR circuits: The delay of circuit can be reduced by varying Resistor and Capacitor (R and C). Resistor can be varied by varying the size of the transistor. RC delay models used to analyses the delay of the circuit. This delay models are created with respect to XOR and XNOR circuit, for unique input conditions as shown in Figure 6. In these models when input AB in 00 conditions, the XOR output will be discharge via path of transistors M1 and M2 both are associated in parallel as shown in Fig. 6(a) and transistor M5 are in linear region but discharging paths also these transistors. M3 and M4 transistors are cut off region or open circuits. The XOR output will be fully discharged when charging the node X path through turns ON the M5 transistor only, otherwise it will not be discharge completely. Therefore, for input AB in 00 conditions, the total delay of XOR in terms of R and C can be written in

$$TXOR00 = RM8 * CX + (RM1 \parallel RM2 \parallel RM5) CXOR. (1)$$

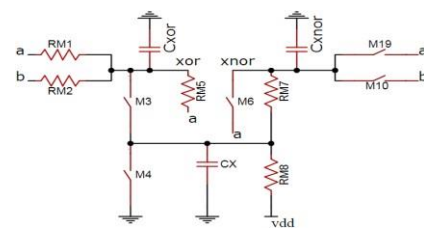


Fig. 6(a). AB in 00.

In the above equation (1) RM5 will be consider as a variable resistor because it will be depending on the charging of node X. Input AB in 01 condition, output can be charged through the transistor M2 only as shown in Fig. 6(b). In this condition, variable resistor is considered as M2 transistor. Delay for input AB in 01 condition can be given as

$$TXOR01 = RM2 * CXOR. (2)$$

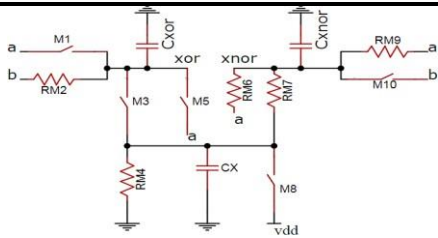


Fig. 6(b). AB in 01.

For input AB in 10 conditions, the output can be charged through transistor M1 but not fully charged through this transistor, it will be depending upon the node X is available through M3 transistor. And also, in this condition other charging paths are available through transistors M5 and M8, as shown in Fig. 6(c). Total delay for this condition can be given as

$$TXOR_{10} = (RM8 \parallel (RM1 + RM3)) CX + (RM1 \parallel (RM8 + RM3) \parallel RM5) CXOR. \quad (3)$$

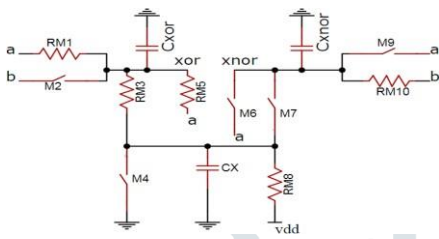


Fig. 6(c). AB in 10.

The last input conditions as AB in 11 outputs will be discharging through the transistor M3 and M4, also consider node X path as shown in Fig. 6(d). Total delay for this input condition is given as

$$TXOR_{11} = RM4CX + (RM4 + RM3) CXOR. \quad (4)$$

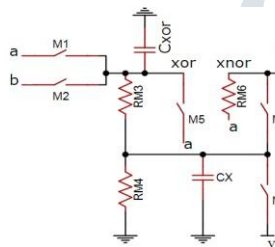


Fig. 6(d). AB in 11.

**B. PTL cross coupled XOR and XNOR circuit**

In this circuit implemented using only 6 transistors PTL based circuit [16] as shown in Fig. 3. In this circuit, represents two corresponding feedback transistors are utilized to restore the low logic in XOR and XNOR output side. This system gives good driving capable and full output voltage of XOR and XNOR. The PTL cross coupled circuit connected with parasitic capacitance to XOR and XNOR output sides. The upper part is PMOS network connected to Vdd and lower part is NMOS network connected to ground. For the input AB in 00 conditions, transistors M1, M2 and M3 turns ON. Transistor M1 and M2 passes logic 0 with switch ON the transistor M3 and it passes logic 1 than charge at the XNOR output. The input AB in 01 condition, transistors M2 and M4 turns ON. The XOR output will be charge through transistor M2 and XNOR output will be discharges through transistor M4 because transistor M2 and M4 passes logic 1 and logic 0 at each output. The input AB in 10 condition, transistors M1 and M5 turns ON. The XOR output will be charge through transistor M1 and XNOR output will be discharges through transistor M5 because transistor M1 and M5 passes logic 1 and logic 0 at each output. The input AB in 11 conditions, transistors M4, M5 and M6 turns ON. Transistor M4 and M5 passes logic 1 with switch ON transistor M6 and it passes logic 0 at XOR output. In this system provides less power dissipation, more delay.

**C. PTL based XOR and XNOR circuits**

1) *PTL circuit1*: It is also one of the improved designs of XOR and XNOR circuit1 is implemented using 12 transistors [14] as shown in Fig. 7. PTL circuit provides low power dissipation and better delay than alternative circuits, by Proper sizing of all transistors and full output voltage of XOR and XNOR. The input AB in 00 conditions, transistors M1, M2 and M3 turns ON or linear region and transistors M4 and M5 is in cut off region. Transistors M1 and M2 passes logic 0, respectively transistor M3 also passes logic 0 at the XOR output. Input AB in 01 condition, transistors M1, M3 and M4 turns ON. Transistors M1 and M3 passes logic 1 at XOR output and M4 is connected to ground but it doesn't connect to XOR output node because the transistor M4 in open switch or cut off region. Input AB in 10 condition, transistors M2 and M4 turns ON. XOR output is depending upon only the transistor M2 and it passes logic 1 at XOR output. Input AB in 11 condition, transistors M4 and M5 switch ON and passes logic 0 at XOR output. Similarly, in XNOR input AB in 00 condition, transistors M1 and M2 turns ON and passes logic 1 at XNOR output. Input AB in 01 condition, transistors M2 and M4 turns ON but only the transistor M2 passes logic 0 at output node. Input AB in 10 conditions, transistors M1, M3 and M5 turns ON. Transistors M3 and M5 are passes logic 0 at output node. Input AB in 11 conditions, transistors M3, M4 and M5 turns ON, and pass logic 1 at XNOR output.

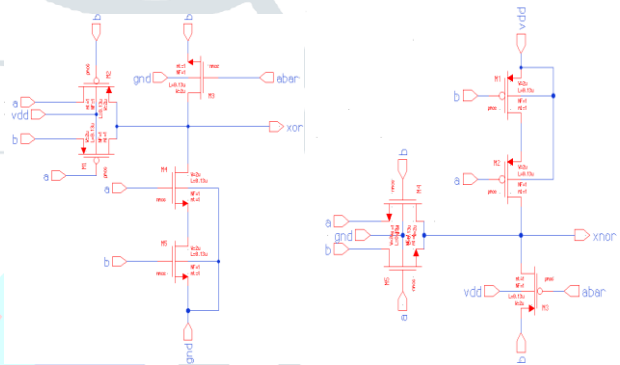


Fig. 7. PTL based XOR and XNOR circuit1.

2) *PTL circuit2*: It is also one of the PTL based circuit implemented by using 12 transistors [6] as shown in Fig. 8. In this system PMOS and NMOS transistors are connected in parallel. This design provides low power and good driving capability. For the input AB in 00 conditions, transistor M1 and M4 turns ON and passes logic 0 at XOR output. Input AB in 01 condition, transistors M2 and M4 turn ON and pass logic 1 at XOR output. Input AB in 10 condition, transistors M1 and M3 turn ON and pass logic 1 at output node. The input AB in 01 and 10 conditions, XOR will be charge. Final input AB in 11 conditions, XOR will be completely discharge through transistors M2 and M3. For XNOR part input AB in 00 conditions, transistors M3 and M4 turn ON and pass logic 1 at XNOR output. Input AB in 01 condition, transistors M2 and M3 switch ON and pass logic 0 at output node. Input AB in 10 condition, transistors M1 and M4 switch ON and pass logic 0 at output node. For input AB in 11 conditions, transistors M1 and M2 turn ON and pass logic 1 at XNOR output. The XNOR output will be charge at inputs are same (00 and 11) condition.

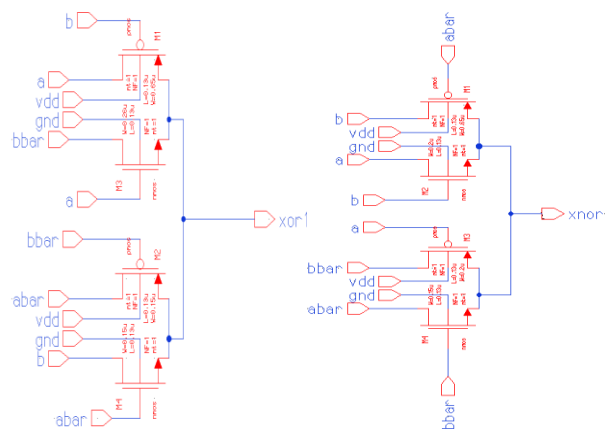


Fig. 8. PTL based XOR and XNOR circuit2.

III. SIMULATION RESULTS

All circuits are simulated using Mentor Graphics EDA tool at 130nm technology. The supply voltage is 1.2V and operating frequency of 1 GHz. In the waveform of CPL cross coupled XOR and XNOR circuit output can be seen for all the input conditions 00, 01, 10 and 11 as shown in Fig. 9. Table I shows the Performance analysis of XOR and XNOR circuits compared with others in terms of worst-case delay, power dissipation and PDP. The delay is calculated as 50% voltage level of input and output value for all rising and falling edge. Power dissipation is depending on supply voltage, capacitance, and frequency according to the equation 5.

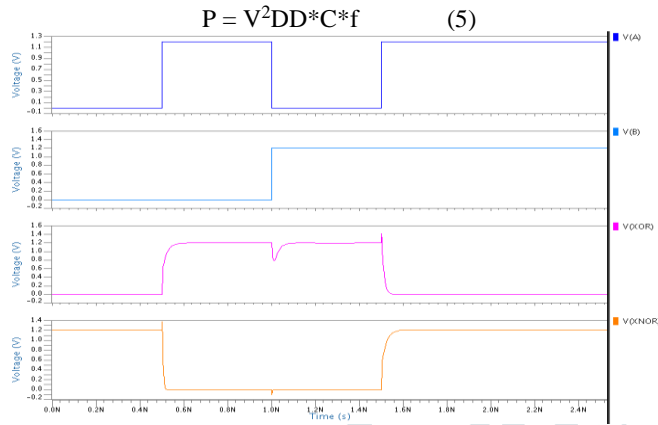


Fig. 9. Waveforms of CPL cross coupled XOR and XNOR circuit.

Performance analyses of XOR and XNOR circuit are compared with others in terms of worst-case delay, power dissipation and PDP are in Table I.

TABLE I. COMPARISON BETWEEN XOR AND XNOR CIRCUITS IN TERMS OF DELAY, POWER DISSIPATION AND PDP AT THE SUPPLY VOLTAGE OF 1.2V AND 1GHZ FOR OPERATING FREQUENCY

XOR-XNOR circuits	No. of transistors	Delay	Delay	Power (nW)	PDP (aJ)
		(ps) XOR	(ps) XNOR		
PTL cross coupled	6	45.41	65.93	3.42	0.22
CPL cross coupled	10	9.18	17.58	6.4	0.11
PTL circuit1	12	17.34	17.86	5.15	0.09
PTL circuit2	12	9.11	18.75	3.78	0.07

When all the circuits were simulated, it can be observed that power dissipation of PTL cross coupled is lowest that is 3.42 nW as shown in Fig. 10.

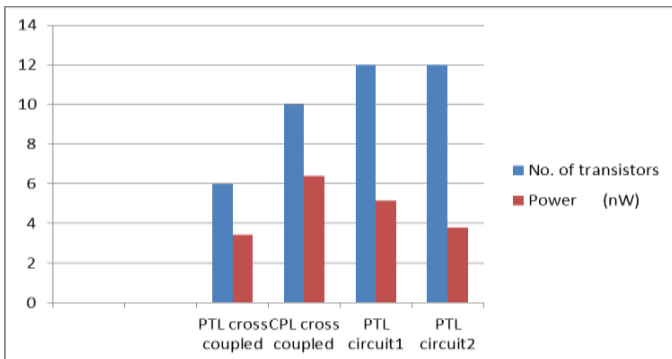


Fig. 10. Power dissipation bar chart for various circuits.

When all the circuits were simulated it can be observed that the PTL circuit2 and CPL cross coupled has got lowest worst case delay for XOR as 9.11ps and XNOR as 17.58ps, respectively as shown in Fig. 11.

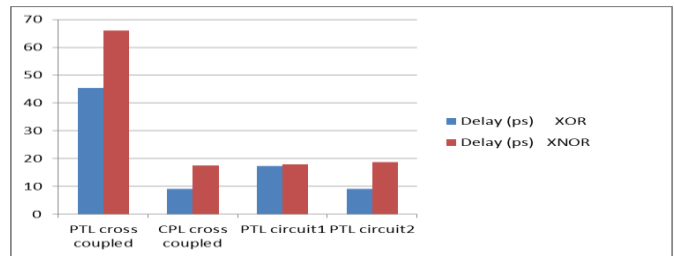


Fig. 11. Delay bar chart for various circuits.

When all the circuits were simulated, it can be observed that PDP of PTL circuit2 is lowest that is 0.07 aJ (10^-18) as shown in Fig. 12.

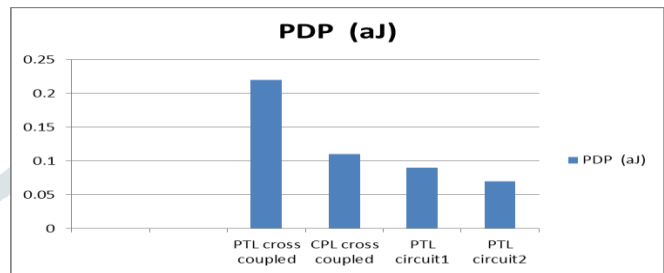


Fig. 12. PDP bar chart for various circuits.

The layout for the schematic explained in Fig. 5. is shown in Figure 13. Layout is done using pyxis and DRC is checked using calibre at 130nm technology.

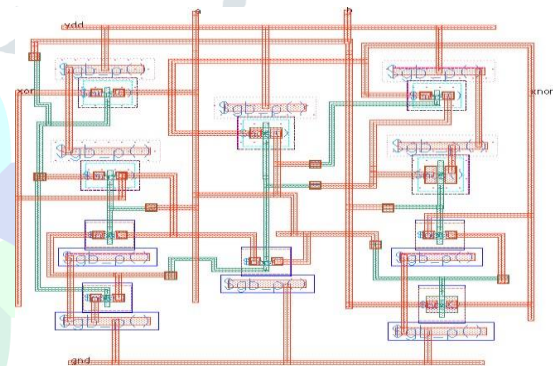


Fig. 13. Layout of CPL cross coupled XOR and XNOR circuit.

IV. CONCLUSION

Adder is important and basic component of ALU. The adder circuits are built using XOR and XNOR circuits. CPL, PTL, PTL circuit1, PTL circuit2 and CMOS, XOR-XNOR circuits were analyzed and simulated using Mentor Graphics EDA tool at 130nm technology. The performance analysis was done with respect to power, delay and PDP. The PTL cross coupled has got lowest power of 3.42 nW. The PTL circuit2 and CPL cross coupled has got lowest worst-case delay for XOR of 9.11ps and XNOR of 17.58ps, respectively. When PDP is considered PTL circuit2 has got lowest PDP of 0.07 aJ.

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