2:1 Multiplexers Using Various Styles of Design

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ABSTRACT: ***This article offers a comparative 2:1 multiplexer analysis of logic styles of three distinct technologies, 45nm and 32nm and 16nm (transmission door, transistor and CMOS logic). Synopsys HSPICE tool with 1V power supply is used to simulate. As a consequence, the 2:1 multiplexer used by TGL consumes the least power. The transistor logic consumes 99.7% less power than PTL and 99% more power than CMOS consumes. Since the PTL multiplexer uses minimal number of transistors, 2, the size of the efficient 2:1 MUX logic circuit is therefore low performance as its output is slightly distorted. Two key objectives for the 2:1 MUX design are being achieved in the comparative research. The first is that transistors are lower, and the second aim is that energy consumption is minimum. The investigation is performed with 1V energy supply from Synopsys HSPICE using three separate technologies: 45nm, 32nm and 16nm. As a result, TGL's 2:1 multiplexer is the least power consumption.***

KEYWORDS: ***2:1 Multiplexer, Circuits, CMOS logic, Design, Power Consumption, Transistors.***

1. INTRODUCTION

Very Large Scale Integration (VLSI) has been a crucial approach in recent years for the construction of built-in circuits (ICs) by placing millions of electrical components or transistors together on a single chip. That means that every electrical equipment reduces the silicone area, the delay and energy consumption [1]. The multiplexer is an essential element in the networking of communications. A combination circuit is a multiplexer which transforms serial data to parallel data. Multiplexer's major role is to integrate numerous users (or channels) into a single data transmission line to enhance this channel's efficiency. The 2:1 MUX has an output, two inputs and a line. The specific input is picked and sent to the output according to the binary value of the selected line. In this article 2:1 MUX design the gate logic, the transistor logic and the CMOS logic are used. A comparison is carried out between the number and power dissipation of transistors utilized to construct such circuits. The Synopsys HSPICE tool is used to model these circuits [2].

The development of an autonomous logic/circuit synthesizer accepts various Boolean functions as a system input and creates netlist output from a cell-based cell transistors library with 2-to-1 multiplexers and inverters. For these Boolean functions, the first synthesis technique builds efficient binary decision diagrams for both multi-function and minimal width. A 2-to-1 MUX (MUX) multiplexer of properly configured transistor logo is used to produce each of the nodes in the BDD trees. In order to increase speed and reduce the voltage problem, the inverters are installed along all the MUX lines. Several approaches are presented to decrease the latency in the crucial path for generating quicker circuits in the multiplexer chain. Our synthesizer offers higher speed and area performance in comparison to the newly suggested top-down, pass transistor-based architecture because of the reduced number of cascade inverters [3].

Multiplexer is a universal combination circuit for all logical gates. The multiplexer is a 2nd input, n' select and single output line digital switchover. The output is created by connecting to the selected data entry line in accordance with the binary combination of the selected lines. 2:1 MUX features two input data lines, one selected line and one output line. If the select line's binary value is logical '0,' the input D0 is transferred to the output line. The data line D1 is then linked and sent to the output line when the binary value for the select line is logic '1.' Block diagram 2:1 MUX and Boolean expression is as follows: Figure 1 shows Boolean expression and block diagram 2:1 MUX [4].

$$Y = D_0S^- + D_1S$$

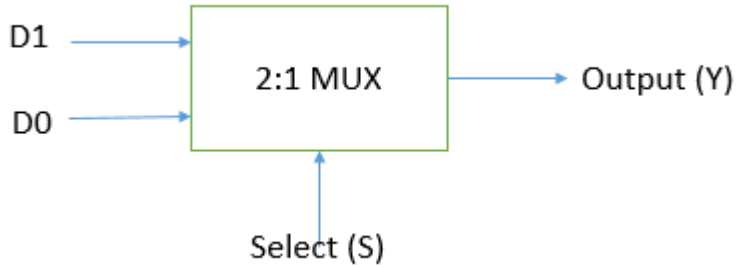

Figure 1: Basic 2:1 Multiplexer.

Figure 2 provides the following logic circuit of 2:1 MUX with the fundamental logic gates i.e. AND, OR and NOT gates:

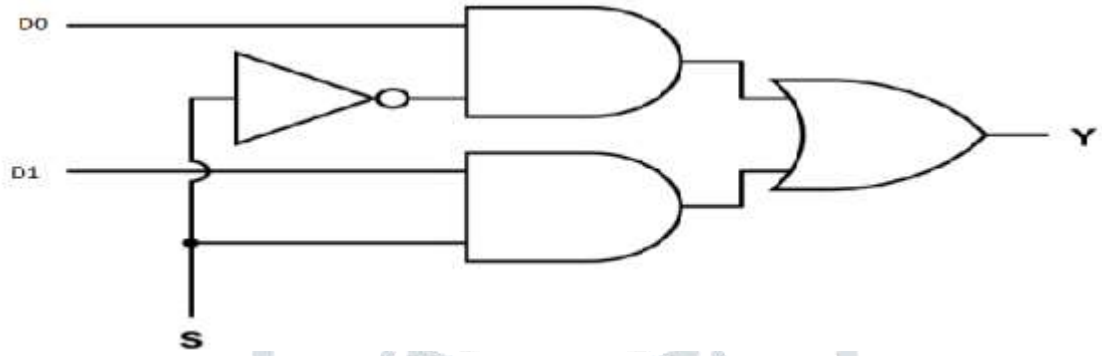

Figure 2: Logic Circuit of 2:1 MUX.

The table of truth as given in Table 1 shows below all conceivable combinations of the selected line and the data supplied. From the table it can be easily deduced that if the selected line is of low logic, output is the same as data entering D0 regardless of the values of other data entry. Likewise, whatever the value of the D1 data line may be, the resulting output will then show the same value as the D1 data input if the selected line is in high logic [5].

Table 1: Truth Table of 2:1 MUX.

S	D0	D1	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

1.1 Transmission Gate Logic Based 2:1 MUX:

A bilateral shutter consisting of a PMOS transistor and an NMOS transistor is a transmission door. On the basis of externally provided control signal it obstructs or sends a signal from the input to the output. The control signal applied to the gates in such a way that both transistors are activated or disabled at the same time. Figure 3 shows a 2:1 multiplexer constructed with gate logic. There are 4 transistors in the circuits. In accordance with the logic applies to the control input S the logic circuit chooses either the data line A or B.

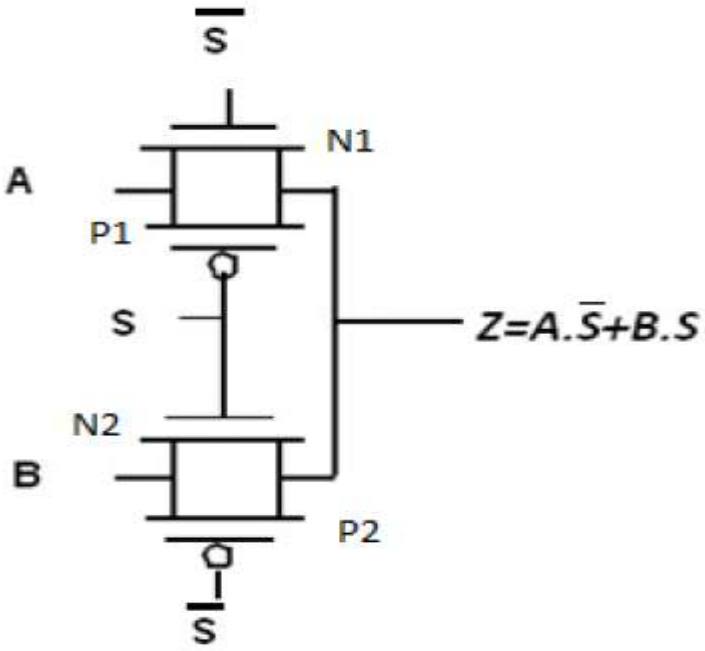

Figure 3: 2:1 MUX Using Transmission Gate Only.

The transistors N1 and P1 are turned on and act like short circuits when "S" is applied to the logical value '0,' while the transistors N2 and P2 are switched off and act as open circuits. Data A is therefore sent to the output. The N1 and P1 transistors are switched down and behave like open circuit when the control signal S is sent with the logic '1' while the N2 and P2 transistors are switched on and behave like short circuits. Only the path between data input B and output is therefore available. This circuit is simulated using HSPICE tool with a power supply of 45nm, 32nm and 16 nm with the desired output.

The following may be displayed as a bar graph with power consumption of 2:1 MUX utilizing 45nm, 32nm, and 16 nm technology with TGL.

1.2 2:1 MUX Using Pass Transistor Logic:

In accordance with the logic applied externally to the transistor gate, NMOS transistors are used to pass or block the electrical signal as the Pass Transistor Logic (PTL). It is used to minimize the number of transistors by sacrificing the logic circuit performance by removing superfluous transistors. Using the logic of Pass Transistor, only two NMOS transistors may construct a 2:1 multiplexer.

At the source of two pass transistors N1 and N2, two data inputs A and B are applied correspondingly. The transistor N1 is activated and portraits are switched off when the control signal S is given with a low logic. The output line is therefore provided with data input A. However, when a high logic control signal is provided, N1 is disabled, but N2 is a short circuit. Transistor N2 is disabled. Therefore, only a path between data input B and the output line is available and the output therefore follows input B. Waveforms of input and output produced after simulation are shown. The circuit is simulated in 45nm, 32nm and 16nm technologies and a bar graph shows the comparison of circuit power consumption at various technologies.

1.3 2:1 MUX Using CMOS Logic:

The CMOS logic uses a symmetrical number of both types of MOSFETs: PMOS and NMOS. The logic is complementary to metal oxide semiconductor. This means that any logic circuit is more efficient since NMOS is the high '0' device and PMOS is the strong one. Therefore, CMOS offers full '1' and full '0' logics without distortion at the output.

2:1 CMOS models with 10 transistors as seen in Figure 4.

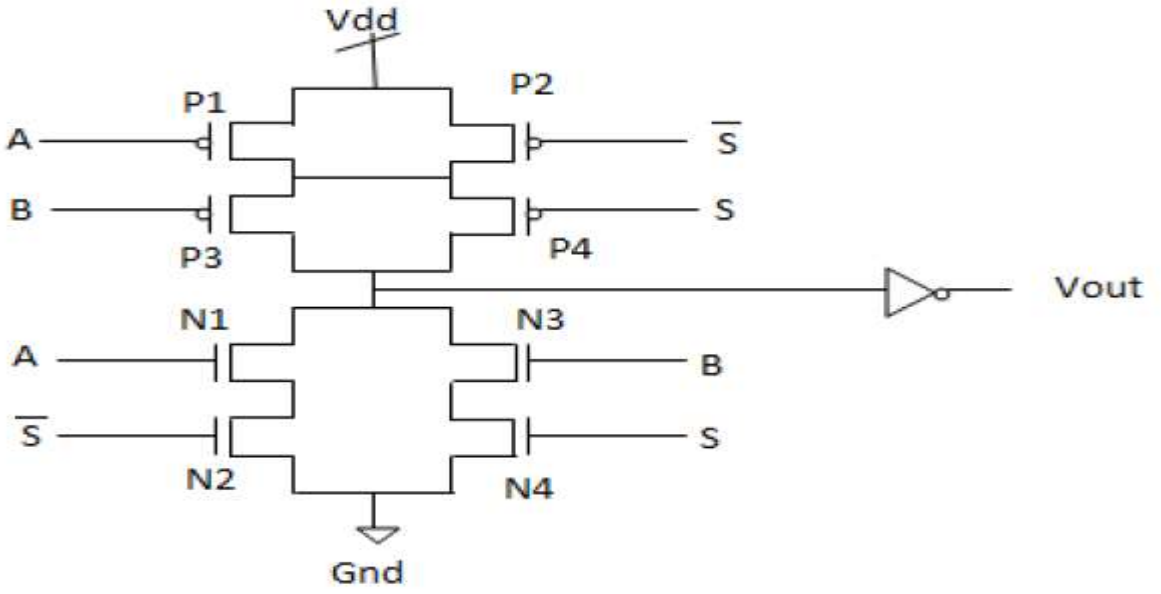

Figure 4: 2:1 MUX Using CMOS Logic Only.

The circuit is simulated using an HSPICE tool, CMOS multiplexer simulations are performed using technology 45nm, 32nm and 16nm. In the following bar graph depiction, the power consumption is compared by the circuit of these technologies. As technology decreases, energy consumption likewise decreases. It may be concluded.

2. LITERATURE SURVEY

R. V. Anugraha *et al.* presented in the article that as MUX is an essential part of the communication system, an efficient design of low-power MUX is needed to enhance data transmission efficiency, make use of the computer's large memory space, and convert data parallel to serial form in telecommunication networks. This study therefore uses a basic 2:1 MUX to determine the optimum logical family that is suited for the construction of higher MUJ levels, utilizing several CMOS logic families, such as Static CMOS logic, Pseudo NMOS logic, Domino Logic and Dual-Rail Domino Logic. VLSI technology implements its features such as tiny size, low cost, high speed and low power. VLSI's back-hand instrument is used for the efficiency study of the MUX with several CMOS logic families: SCHEMATIC CADENCE VIRTUOSO 6.1 at 180nm. The results reveal that the 2:1 MUX Domino based logic is the most efficient design, with the average power consumption 20.06 percent and the 20.1 percent of the PDP (Power Delay Product). However, tradeoffs between Domino logic and CMOS logic may be disregarded when the total performance is taken into account. Since Domino logic outperforms other logic families, this work indicated that any higher level MUX with low power delay, PDP and Domino logic may be accomplished [6].

M. Sumathi *et al.* presented in the article that in consumer electronics, low power and low power have now become a significant concern, and research has to be conducted on combination circuits. A multiplexer or data selector is an important device in digital circuits for the processing of several entries with one output. Multiplexers are currently a universal logical component required to construct any digital combination logic system in ICs, thus a multiplexer topology for low energy consumption and high speed has to be designed or revised. The present article analyses performance of several multiplexer architectures utilizing the CMOS (Metal Oxide Semiconductor) logic. Positive feedback (PFAL), cascade voltage switch logic (CVSL) and transmission gate based logic styles make the multiplexer architectures possible. The energy consumption, delays, voltage of supply and numbers of transistors are calculated and compared in the designs. The performance research is conducted utilizing CMOS technology of 0.18-µm. Detailed transistor levels simulation utilizing DSCH3 and Micro wind 3.1 CAD tools distinguish these distinct logic types [7].

M. Mishra *et al.* presented in the article that memory elements and structure for data management are made up of multiplexer as the main components of the Complementary Metal Oxide Semiconductor (CMOS). One of the most significant considerations in system design is low-power consumption. Various types have been created for low power use in high speed applications. In this work, a low power 4:1 multiplexer is developed using several logical types (MUX). For several 4:1 MUX logic types, the leakage current, power consumption, delays and count of

transistors is compared. Compared to other logic types, the transmission door multiplexer uses little power. Static MUX is compared to NMOS MUX with the larger number of transistors. The conclusion indicates that NMOS pass transistor logic multiplexer executes the task with least latency and minimum power consumption with less numbers of transistors. In 45 nm technology and 0.7 V supply voltage below 27°C, the designed circuit is built [8].

A. Morgenshtein *et al.* presented in the article that a novel low-power digital combinatorial circuit design approach to Gate diffusion input (GDI) is introduced. This approach enables energy use, propagation delays and the size of digital circuits to be reduced while retaining a low logical complexity. Comparison of performance with standard CMOS and other logical design processes is provided. Disposition area, device number, delay and power dissipation are the different techniques evaluated. Top-down Design, pre-computer synthesis and compatibility of the technology are discussed and the advantages and inconveniences of GDI in comparison to others are shown. In different design styles, various logic circuits were implemented. They discuss their characteristics, report simulation results and present test chip measurements [9].

K. Yano *et al.* presented in the article that for the first time, the cell-based transistor library and the tool for synthesizing is designed to elucidate the possibilities of the top-down transistor logic. LEAP is the whole plan (Lean Integration with Pass-Transistors). The multiplexer function and open-drain topology of an overhead transistor-based cell. This cell has the freedom of design and compatibility with standard cellular design on transistor-level circuits. Compared to a traditional CMOS library, which has more than 60 cells and the most up-to-date synthesis, there is an extremely simple cell library with only seven cells combined with a synthesis tool called circuit inventor. The results reveal that LEAP enhances the area, delay and power dissipation and that three factors increase the value for money ratio. This shows that LEAP is capable of making a quantum leap in LSI value while decreasing costs. Key difficulties to be resolved before transistor logic is passed are also highlighted as a general logic system replacing CMOS [10].

3. DISCUSSION

2:1 MUX is being developed utilizing TGL, Transistor Logic (PTL) and CMOS logic. All of these circuits are simulated with HSPICE tools with a power supply of 45nm, 32nm and 16nm, and the power consumption is evaluated in every case. Multiplexer power consumption, which has both transmission and CMOS design, is exceptionally low compared with Pass Transistor Logic power consumption. When all three circuits with various design approaches are compared, the minimum power is utilized by a 2:1 TGL multiplexer. While power required by TGL and CMOS circuits is comparable, the number of transistors used to develop these circuits does not differ greatly. The TGL method for designing 2:1 MUX employs the CMOS three times as many transistors. Since PTL's multiplexer uses minimal transistor numbers, i.e., 2 it is consequently an efficiently-fitted 2:1 MUX logic circuit, but its output is low since it is somewhat distorted. CMOS employs many components, but has a high performance and a minimal switching time hence has a minimum latency when compared with TGL and PTL.

4. CONCLUSION

The comparison study is carried out with two major aims to find the 2:1 MUX design. The first is to have fewer transistors and the second objective is to have minimal energy usage. The study is carried out using Synopsys HSPICE at 1V energy supply, utilizing three distinct technologies: 45nm, 32nm and 16nm. As a consequence, the 2:1 multiplexer used by TGL consumes the least power. The transistor logic consumes 99.7% less power than PTL and 99% more power than CMOS consumes. While power required by TGL and CMOS circuits is comparable, the number of transistors used to develop these circuits does not differ greatly. Since the PTL multiplexer uses minimal number of transistors, 2, the size of the efficient 2:1 MUX logic circuit is therefore low performance as its output is slightly distorted.

REFERENCES

[1] N. H.E.Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective (4th Edition)*. 2010.

[2] I. Gupta and N. Arora, “Design and Analysis of 2 : 1 Multiplexer for High Performance Digital Systems,” *IJECT VOL. 3, ISSUE 1, JAN. - MARCH 2012*, 2012.

[3] S. F. Hsiao, J. S. Yeh, and D. Y. Chen, “High-performance multiplexer-based logic synthesis using pass-transistor logic,” *VLSI Des.*, 2002, doi: 10.1080/1065514021000054736.

[4] A. Morgenshtein, A. Fish, and I. A. Wagner, “Gate-diffusion input (GDI) - A novel power efficient method for digital circuits: A design

methodology," 2001, doi: 10.1109/asic.2001.954670.

[5] P. K. Sharma and N. K. Singh, "Power comparison of single and dual rail 2:1 MUX designs at different levels of technology," 2014, doi: 10.1109/ICCICCT.2014.6993045.

[6] R. V. Anugraha, D. S. Durga, and R. Avudaiammam, "Design and performance analysis of 2:1 multiplexer using multiple logic families at 180 nm technology," 2017, doi: 10.1109/RTEICT.2017.8256918.

[7] M. Sumathi, K. H. Shakthimurugan, and K. Sumathi, "Performance study of 4:1 multiplexer CMOS logic structures," *Int. J. Control Theory Appl.*, 2016.

[8] M. Mishra and S. Akashe, "Multiple logic styles for low power 4:1 multiplexer in 45 nm technology," *Int. J. Signal Imaging Syst. Eng.*, 2015, doi: 10.1504/IJSISE.2015.070487.

[9] A. Morgenshtein, A. Fish, and I. A. Wagner, "Gate-diffusion input (GDI): A power-efficient method for digital combinatorial circuits," *IEEE Trans. Very Large Scale Integr. Syst.*, 2002, doi: 10.1109/TVLSI.2002.801578.

[10] K. Yano, Y. Sasaki, K. Rikino, and K. Seki, "Top-down pass-transistor logic design," *IEEE J. Solid-State Circuits*, 1996, doi: 10.1109/4.509865.