Multiplexer and De-Multiplexer Design Employing Various 90 Nm Technology Adiabatic Logic

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ABSTRACT: ***The design and assessment of 8:1 multiplexers utilizing various adiabatic logics was discussed in our research work. High power consumption in digital circuits is the major factor for Very Large Scale Integration (VLSI) design engineers. In this article, we will show the Complementary Metal Oxide Semiconductor (CMOS)-logical new design for a low power adiabatic 8:1 Multiplexer and De-Multiplexer using a 90 nm technology to match this trend. 2N-2N2P uses a transistor structured cross coupling structure for adiabatic operation and double sleep method, with the features of CMOS and the adiabatic logic family 2N2P. Adiabatic logic families usually employ clocks in several phases. Multi-phase clock accelerates the waste of power in your clock network. Due to the clock skew problems and excessive complexity of the clocks, several adiabatic logics are inadequate for high speed operational design. Thus we focus on recovery of energy with efficient energy clock use in this study work. The adiabatic logic circuit has shown to be of great relevance in the development of applications where energy conservation is a critical component for high efficiency, battery-powered handheld and portable electronics.***

KEYWORDS: ***Adiabatic Logic, CMOS, Energy Recovery, Logic Family, Multiplexer, Transistors.***

1. INTRODUCTION

For the design of VLSI circuits, energy recovery is a positive metric. Circuits for energy recovery reduce energy use by driving currents and storing energy across appliances slowly by charging and discharging through their capacitive loads. The circuit of this kind is known as boosted logic or adiabatic logic. Adiabatic circuits function at low operating frequencies very efficiently and cease at high frequencies. Adiabatic logic is the logic utilized for electrical low-power circuits. The second important advantage of adiabatic logic is that the inherent pipeline of the circuits may be achieved utilizing four phase trapezoidal power line clock In this study we describe the various adiabatic logic approaches using a de-multiplexer. Multiplexer is a circuit with several input lines and a single output line. Experts can locate the input to the output in the selected lines and you can also transmit data by a data selector or choose lines from input to output too serial. De-multiplexer is an input line circuit with numerous output lines. It is also used to transfer data concurrently via data selected from input to output [1], [2].

1.1. Overview of Adiabatic Logic Families:

This paper focus on power dissipation of the CMOS logic and other adiabatic logics are 2N2P logic, PAL logic and 2N2N2P logic [3].

1.1.1. MUX-DEMUX Using CMOS Logic Family:

CMOS is one of the most common styles of logic and is currently used for a few days. PMOS and NMOS are employed in this logic for the construction of a circuit. The phrase has a network pull up and a network draw down (see Fig. 1 (a) & (b)).

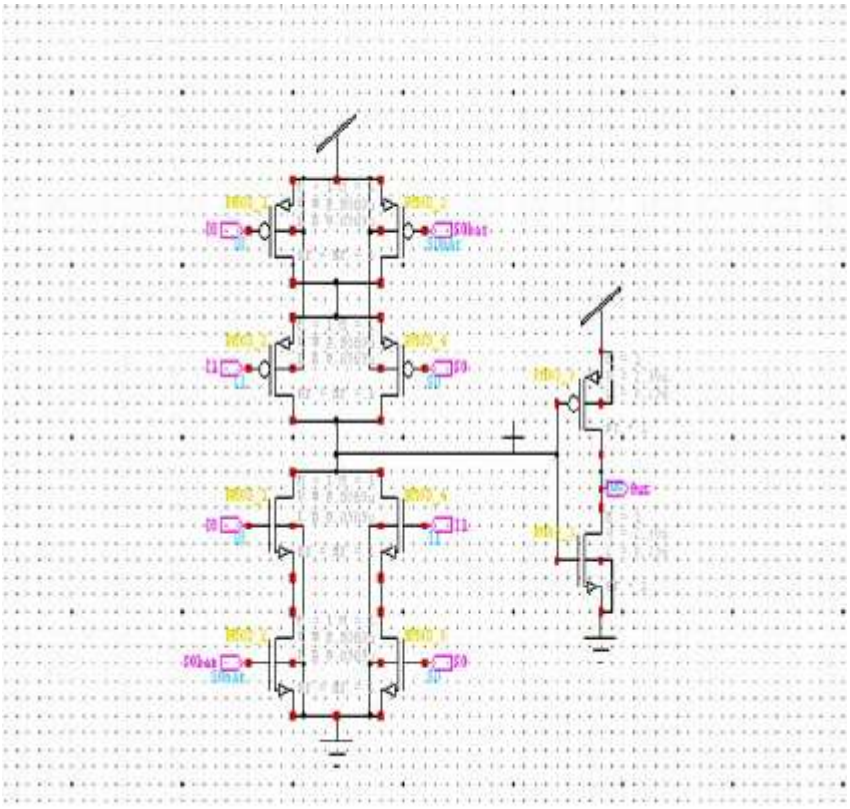

Fig. 1 (a): 2:1 MUX Using CMOS Logic

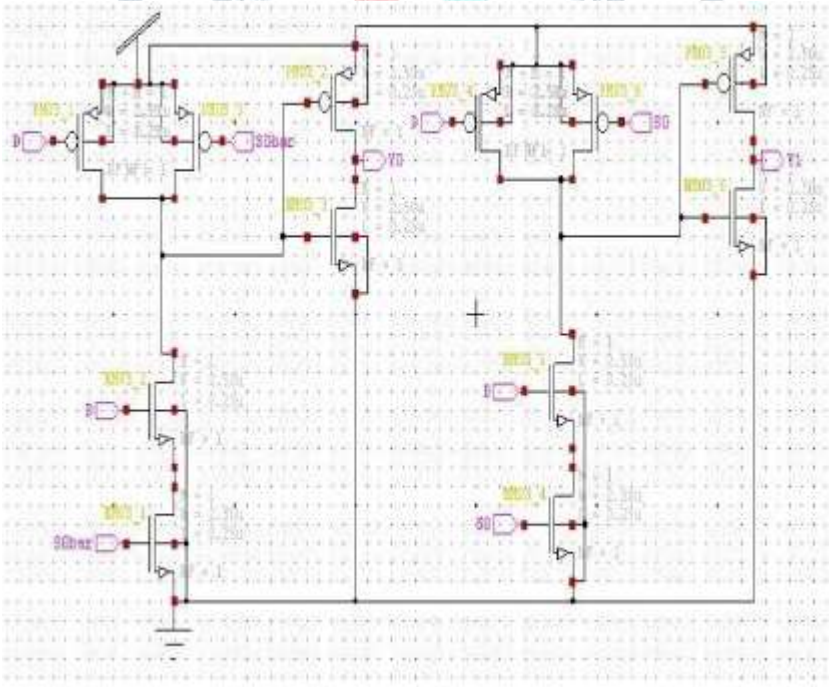

Fig. 1 (b): 2:1 DEMUX Using CMOS Logic

The pull-up network is equipped with PMOS transistors because PMOS transistors are good for V_{DD} output and all NMOS transistors are provided because the NMOS transistor is good for output transistors [4].

A multiplexer is a system that chooses and sends one of the data inputs to the output according to the control signals. The function F = A $\bar{S}$ + BS is implemented. When line S is low, the signal A at the output is selected. When line S is high, the signal B at the output is selected. The design of the 8:1 Multiplexer can be done by 2:1 Multiplexer [5].

1.1.2. MUX Using 2N2N2P Logic Family:

This family is a one-style adiabatic logic family with 2N2P logic family variant. For 2N2N2P, Latch is a combination of two p-MOSFETs and two n-MOSFETs and in parallel, the functional tree has been linked to the N-MOSFETs, which in this family implies the transistors with two n-MOSFETs are added in parallel (see Fig. 2). These n-MOSFETs are connected to the output which is not fluid. The advantage of the adiabatic logic family is that the output and output are provided simultaneously [6].

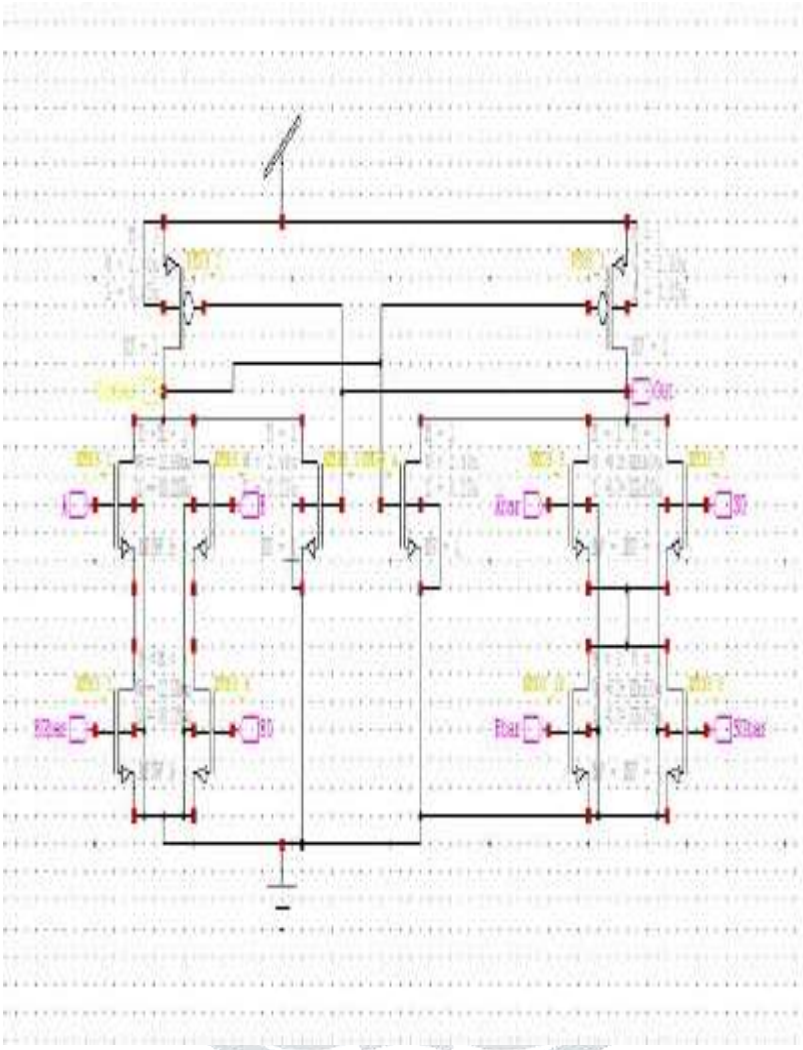

Fig. 2: 2:1 MUX using 2N2N2P logic.

1.1.3. DEMUX Using 2N2P Logic Family:

In order to accomplish adiabatic functions and calculate a logical function, this family of logic employs two n-MOSFET and two transistors with PMOSFET. A 4-phase trapezoidal reload and the 2n2p buffer are used for the family. The construction will now be investigated to cover the performance of the circuit (see Fig. 3). The gate is transferred to the drain on the adjacent PMOS transistors by every PMOS transistor.

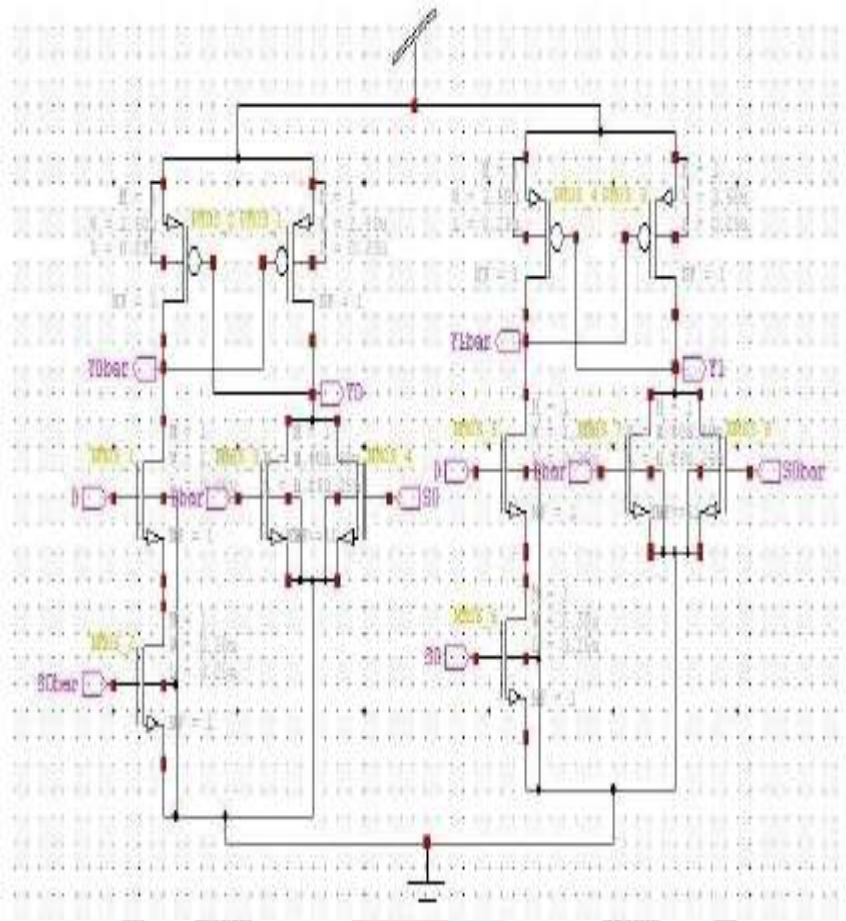

Fig. 3: 2:1 DEMUX Using 2N2P Logic

2. LITERATURE SURVEY

J. C. Kao *et al.* presented in the article that it contains a 14-tap 8-bit FIR (finite pulse response) tester, developed to accomplish a high speed and low-power operation by use of a new family of charging recovery software called the Enhanced Boost Logic (EBL). EBL has enhanced gate overdrive compared to earlier load recovery circuits and results in reduced overhead delay over the static CMOS architecture. The EBL-based FIR, based on post-layout simulations of both designs, was developed with just 1.5 delay cycles above its static CMOS equivalent and uses 21 percent lower energy each cycle. A test chip with a fully integrated 3 nH inductor was manufactured in a 0.13 $/mu$ m CMOS process. In the 365-600 MHz band, the correct function was confirmed. At 466 MHz the tester chip distributes 39,1 mW, with an output of 93,6 nW/MHz/Tap/InBit/CoeffBit, recovering 45% of the electricity per cycle provides [7].

C. S. A. Gong *et al.* presented in the article that this study discusses the design and experimental assessment of a novel type of irreversible energy recovery logic family (ERL) (CEPAL). Although it possesses the features of the quasi-static ERL (QSERL) family, it has enhanced driving capacity and track stability. Therefore, no feedback keeper is required to achieve substantial improvements in area and power overheads in comparison to its QSERL counterparts under the same operating circumstances. In addition, the performance of the QSERL is twice as great if its power clock frequencies (PCs) are the same. Results are presented on the effect of variance on CEPAL. A comparison is also made between CEPAL and other logics of low-power, especially the subthreshold logic, which achieve iso-performance. An 8-bit shift register, built in the suggested approaches, was manufactured in a TSMC 0.18 μm CMOS process to show the working ability of the newly developed circuit. Simulation and measurement data both demonstrate that the logic works, making it ideal for energy-conscious and high-performance (VLSI) circuitry integration [8].

Y. Ye *et al.* presented in the article that this study proposes a novel family of quasi-static energy recovery logics (QSERL) utilizing the adiabatic change concept. Most of the adiabatic logic types previously suggested are dynamic and need sophisticated timing systems. The suggested QSERL employs two syncs supply clocks and is like static CMOS behaviors. Therefore, switching is considerably lower than the logic of dynamics. QSERL

circuits can also be generated directly from static CMOS systems. In this work is also provided a high-performance circuitry that produces two QSERL-compatible sinusoidal complementary clocks. The adiabatic clock circuit locks clock signals frequency, which enables adiabatic modules to be integrated into a VLSI system. We have developed an eight to eight carry-save multiplier with QSERL logic and two sinusoidal phase clocks. SPICE simulation demonstrates that 34% more energy may be saved from the QSERL multiplier with 100 MHz through a static CMOS [9].

S. Vijayakumar *et al.* presented in the article that the most prevalent design, Multiplexer (MUX), is commonly known as a switch. It uses substantial power among the blocks of an ALU that is at the core, ranging from a big super computer to a very little device, of every digital design. There are several methods to optimizing the MUX through power, area and velocity. In this document you are presenting the comparison of the area between traditional MUX, the combination of the transmission gate and the static technique as hybrid style. The TGCSL MUX has a lower power consumption of about 20 percent than the two VDD styles (C2MOS, TGL), but it fails to create a complete swing. Although it works with less power than the other two logic types. This has a huge influence on the performance of a larger multiplexer with TGL MUX de-composed tree. Finally, the field comparison also concludes that the approach suggested is a superior choice [10].

3. DISCUSSION

This short presents a unique non-CMOS 4:1 multiplexer with a different logical approach. A heterogeneous logic architecture combines three fundamental logic types, for instance Dual Value Logic (DVL), gate logic and Simple Passport Logic (SPTL). There are just two transistors between the supply rails. The design utilizes only two stacking transistors in between the supply rails. In the suggested state-of-the-art architecture, just 16 transistors are needed for the actual logic function. A separate selection of DVL and TGL in the first phase according to the input combination reduces the number of transistors. The multiplexer will be built using the SPTL later stage. In order to limit the number of transistors, increase the speed and lower the average dissipation in power, a needed logic style is selected in the initial and second stages according to the input bit combination. The planned system is designed and simulated by means of the Pyxis schematic and Pyxis simulator with 22nm technology. A comparison of broad simulated design outcomes, CMOS tree multiplexer and CMOS NOR multiplexer at different power voltages and frequencies on the same technology node demonstrates improved speed and power-delivery performance of the proposed heterogeneous multiplexer. The multiplexer suggested reduces energy dissipation by 17.3 percent at the least feasible power voltage of 0.8V and a moderate frequency of 1GHz. In comparison with CMOS Tree Type and Multiplexers type CMOS NOR is the number of transistors including inverters also smaller. However, in comparison with CMOS, the solidity of mixed logic styles is enhanced.

Two transistors are used in double sleep (one NMOS and one PMOS). One is switched on in ON mode and one is switched on in OFF mode. In this method, we may use dual threshold voltage to decrease the dissipation of the leakage power. If sleep_n = 1 and PMOS is on state when sleep P =0, the NMOS transistor is on.

Various 8:1 multiplexer waveforms are displayed below in adiabatic logic, such that CMOS, 2N2P and 2N2N2P are used.

The waveform of the output is from volts to seconds. Three select lines are S_0, S_1 and S_2 with outputs for these output waveforms. In Table 1 comparison of energy recovery from different logical systems and different logical families is demonstrated for approaching techniques between MUX and DEMUX.

Table 1: Comparison of Energy Recovery from Various Logic Systems with Various Logical Families.

Approaching Techniques	Energy Recovery (MUX)	Energy Recovery (DEMUX)
CMOS Logic	11.0757nJ	16.9316nJ
2N2P Logic	12.1585nJ	17.4013nJ
2N2N2P Logic	17.3223nJ	27.7290nJ
Dual Sleep	1.9018mJ	18.3316nJ

4. CONCLUSION

In this research we explored the construction and evaluation of 8:1 multiplexers using different adiabatic logics. The main factor for VLSI is high electricity usage on digital circuits. The new logical design for a low power adiabatic 8:1 Multiplexer, a 90 nm technology for MOS will be shown in this article. 2N-2N2P employs a structured cross-connection structure with CMOS characteristics and the 2N2P adiabatic logic family for the adiabatic operation and double sleep methods. Clocks are typically used in adiabatic logic families for many stages. Multi-phase clock speeds your clock network power waste. Because of clock skew issues and excessive clock complexity, several adiabatic logics are insufficient for high-speed operating design. In this study we concentrate on energy recovery with efficient use of the energy clock. In developing applications, energy saving has been a crucial component of high efficiency, battery-powered portable electronics, and the adiabatic logic circuit was very significant.

Multiplexer has been developed and simulated using 90nm technology in several logic types using the Tanner tool. Static CMOS, 2N2P and 2N2N2P logic multiplexer designs are part of these logic types. In this paper, Multiplexer's energy recovery efficiency has been increased by 29% and 36% by 2N2N2P in comparison with 2N2N logic and CMOS logic. In comparison to previous techniques, double-sleep technique is nearly 10^5 times energy efficient. Dual sleep MUX is more energy efficient across all these logic types. In comparison with all adiabatic approaches, we employed dual sleep techniques that are more energy efficient. All findings are checked at different voltages of supply. In the design of applications where energy saving is a key element for high efficiency, battery-operated handheld and portable electronic devices, the adiabatic logic circuit has been shown to be of major importance.

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