Analysis and Design of MOS Differential Amplifier

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ABSTRACT: ***The initial phase of the operational amplifier is the differential amplifier. It merely amplifies the difference between the two signals and rejects any common signals. As the CMOS technology is extended to the nanoscale range, several important features must not be addressed and overcome if an analogue and physical systems are to be successfully designed. In the nanoscale age of the analogue CMOS concept, it is becoming increasingly vital to understand the physical variables which influence circuit reliability and performance and how they will be mitigated or overcome. The use of the modified MOS structure with pull-up and pull-down stacked transistors, the differences amplifier gain factor is enhanced to 5 dB compared to conventional differential amp circuits. This article discusses MOS differential amplifier structure and analysis and how it may be designed for a specific specification. An illustration of the design process and simulation with the NG Spice Tool is taken for an example. Design with the MAGIC VLSI tool is finally developed.***

KEYWORDS: ***Amplifier, Analogue, Circuit, CMOS, Common Mode, Differential Amplifier, Technology.***

1. INTRODUCTION

The initial phase of the operational amplifier is the differential amplifier. It merely amplifies the difference between the two signals and rejects any common signals. Figure 1 illustrates the typical MOS differential amplifier active load structure [1]. The MOSFET is by far the most widely used transistor in both digital and analog circuits, and it is the backbone of modern electronics. One of the most common uses of the MOSFET in analog circuits is the construction of differential amplifiers. The latter are used as input stages in op-amps, video amplifiers, high-speed comparators, and many other analog-based circuits. MOSFET differential amplifiers are used in integrated circuits, such as operational amplifiers, they provide a high input impedance for the input terminals. A properly designed differential amplifier with its current-mirror biasing stages is made from matched-pair devices to minimize imbalances from one side of the differential amplifier to the other.

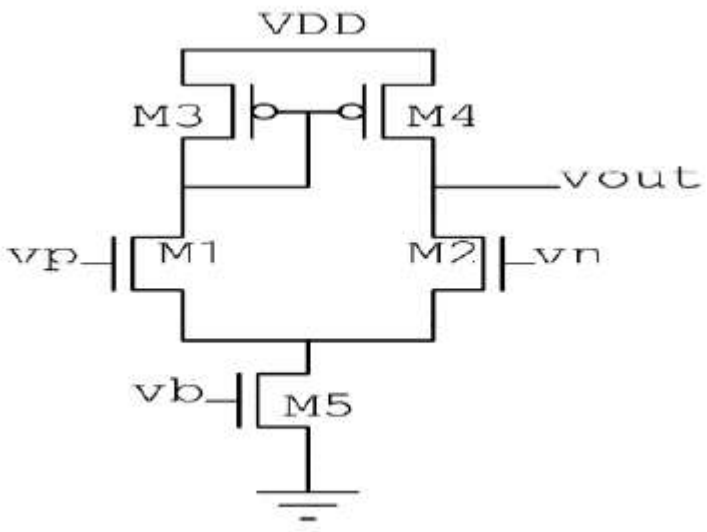

Figure 1: Typical Structure of Differential Amplifier Using Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS).

1.1.Differential amplifier:

We must treat differential inputs (V_d) and common mode inputs (V_{icm}) separately in the analysis of the differential amplifier. The tiny differential amplifier signal circuit for differential signals is shown in figure 2. The node with linked sources M1 and M2 is the basis for differential signals [2].

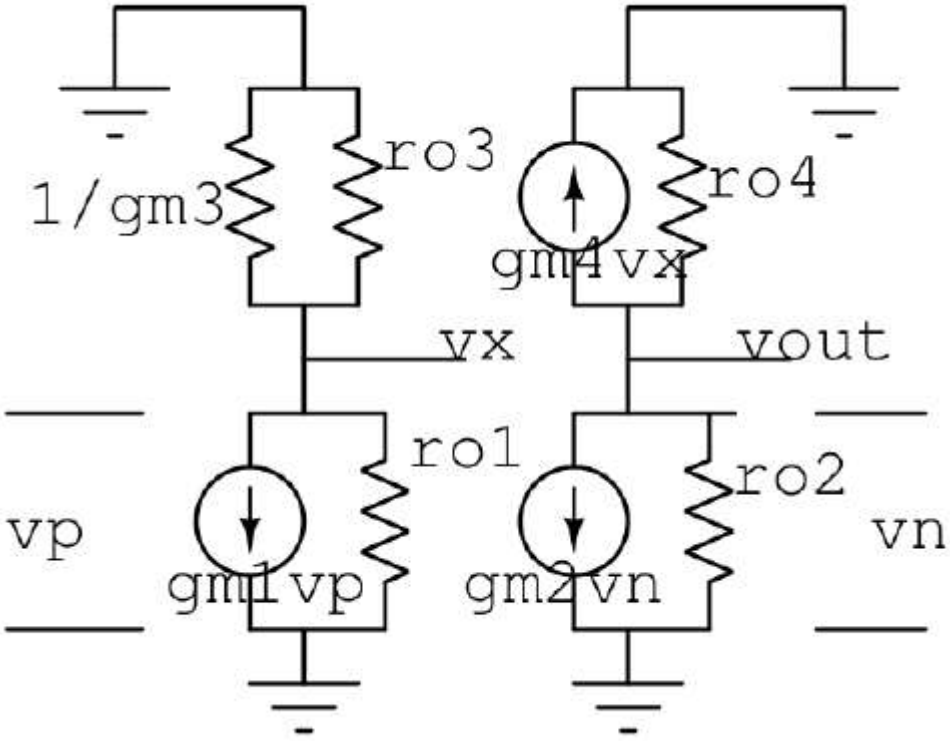

Figure 2: Small Signal Network of Differential Amplifier for Differential Signals.

1.1.1. Common Mode Gain:

The tiny differential amplifier signal network for the common mode signal is shown in Figure 3. The output strength of the current source transistor M5 is present. It is divided into two parallel resistors 2ro5 for analytical purposes [3].

1.1.2. CMRR:

The ratio differential profit to the common mode gain is the common mode rejection ratio (CMMR). The measurement of how efficiently a differential amplifier rejects the common mode signal as a key performance metric [4].

1.1.3. Frequency Response:

There are two C_m and C_L capacities in the simplified tiny differential amplifier signal circuit. C_m is produced mostly by C_{gs3} and C_{gs4}. C_{gd1}, C_{db1} and C_{db3} are also included.

1.1.4. Input Common Mode Range:

The ICMR is the input signal range for which all the transistors are located in saturation regions. The M5 and M1 overrunning voltages determine the minimum ICMR voltage and the M3 and M1 overrun voltage, the maximum ICMR voltage [5].

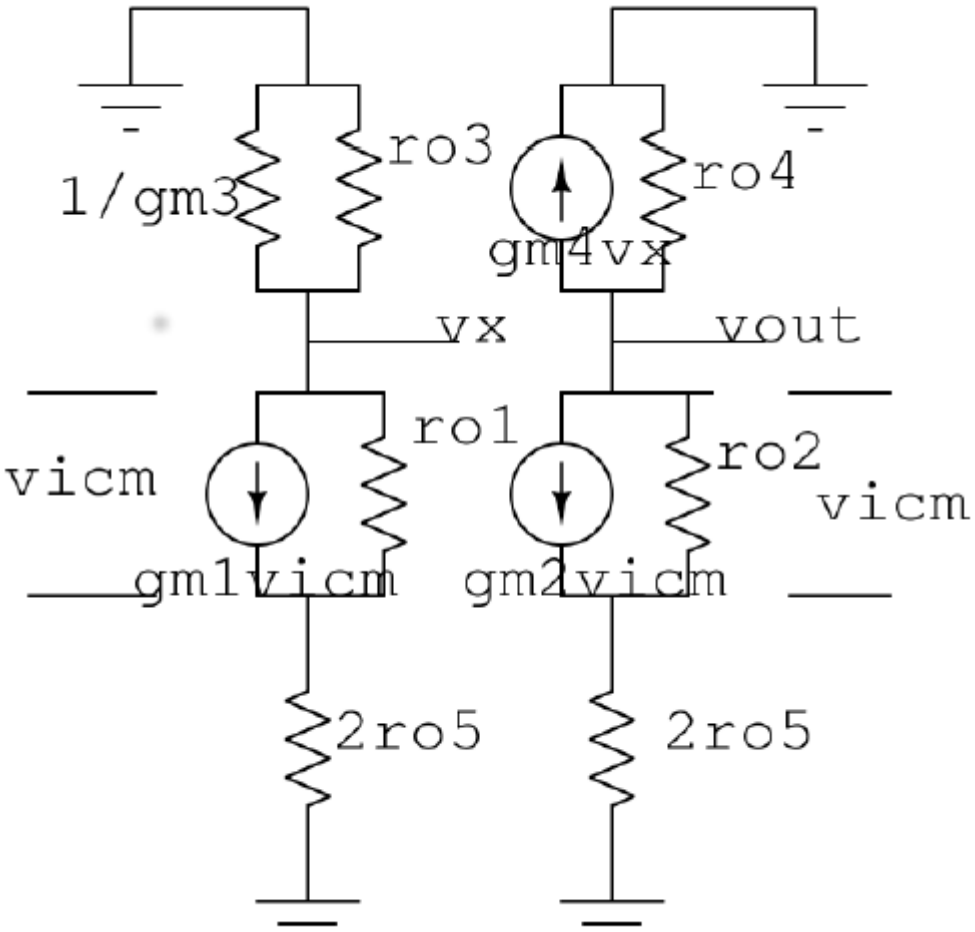

Figure 3: Small Signal Network of Differential Amplifier for Common Mode Signals.

1.1.5. Slew rate:

Depending on the tail current source and capacity, the slew rate of the differential amplifier relies on the output node. The quantity of electricity that can be supplied or sink into the output condenser is specified [6].

1.2.Design of Differential Amplifier:

The requirements for the differential amplifier may consist of:

- Small signal gain (A_v)
- Response frequency for the load capacitance provided (f_{-3dB})
- Common input range of mode
- The load capacitor speed is specified
- Disposal of power

The Differential Enhancer design is an iterative method and particular applications. However, in general, the following measures can be taken.

1. Choose I_5 depending on specified slew rate.
2. Calculate the necessary Ro to achieve the specified f_{-3dB} and amend I_5
3. To satisfy the higher ICMR, select (W/L) $_{3,4}$
4. To get the desired gain, select (W/L) $_{1,2}$
5. To fulfil the ICMR lower select (W/L) $_5$
6. If all design requirements are not satisfied, repeat the procedures above.

Design example:

Problem Statement: design for the following requirements of a difference amplifier in 800 nm technology (see Table 1).

Table 1: Design Specifications

Parameter	Value
A_V	40dB
SR	10V/µs
f_{-3dB}	200 kHz
$ICMR_{min}$	1.5V
$ICMR_{max}$	4V
P_{dis}	2mW
C_L	5pF

Initially, the DC operating point was discovered to verify the weather in all MOSFETs. A tiny signal was then applied to the non-inverting terminal in order to determine the frequency response. The differential amplifier gain and phase response were presented correspondingly. The f_{-3dB} was about 200 kHz and the anticipated gain was 40 dB. At the non-inverting input of 0V at 5V, the ICMR detected the voltage when the difference amplifier was configured in the voltage tracking system. The differential amplifier was in linear region for the input range from 0.7V to 4.4 V. It was far better than anticipated. This amplifier was developed for a 10V/µs slew rate and was achieved following simulation. A 2V pulse was used to evaluate the slew rate, with 1 µs transition time after 2 µs delay, in the voltage follow-up amplifier arrangement. Finally, the construction was designed using the MAGIC VLSI tool in 800 nm CMOS technology as illustrated (see Table 2).

Table 2: Gives The Technology Parameters Of 800 Nm CMOS Technology.

Parameter	Value
V_{DD}	5V
λ_P	$0.05V^{-1}$
λ_N	$0.04V^{-1}$
V_{tn}	0.7V
V_{tp}	-0.7V
K_N	$110\mu A/V^2$
K_P	$50\mu A/V^2$

2. LITERATURE REVIEW

L. L. Lewyn *et al.* presented in the article that as the CMOS technology is extended to the nanoscale range, several important features must not be addressed and overcome if an analogue and physical systems are to be successfully designed. In the technical literature the nature of these not idealities is extensively documented. These include hot-carrier injections and dielectric, time-dependent, failure effects, which limit the power supply, stress and lithographic effects, which limit the accuracy of the matching effects, electro-migration effect, driver life, leakage and mobility, and limit the performance of the equipment. A considerable effort has been made with the electrical design automation sector due to the absence of analogue design and simulation instruments accessible to solve these challenges. During the design process, post-layout simulation tools are of little benefit while computer-assisted design tools are slowness and are not used frequently by analogue circuit designers [7].

P. Jain et al. presented in the article that a new CMOS differential amplifier with little deformation and optimal power use is studied, competent, effortless, low-leakage A CMOS analogue front-end (AFE) circuit for the acquisition of portable biological signals may also be used for the proposed circuit. In order to deliver power from either V_{DD}, V_{OUT}, V_{SS} or V_{OUT}, the suggested circuit is constructed. There is significant CMRR in the proposed circuit. It is a low voltage increase of the common mode and a large voltage increase of the difference mode. The circuit has been constructed to prevent the power supply from V_{DD} to V_{SS}, i.e. the driving power cannot be shortened. This makes it an ideal differential amplifier for the proposed circuit. Competent and speculative combinations of CMOS logic are used to produce the improved functionality of the suggested amplifier circuit with a cross-connected NMOS Gate Terminals. The suggested circuit with a novel MOS combination provides improved performance [8].

S. Mallick *et al.* presented in the article that this study offers a new hybrid optimization method, which combines Backtracking Search Algorithm (BSA) with an evolutionary algorithm, the Diverse Evolution, which is generally recognized (DE). The BSA-DE method is used to optimize two analogue circuits, namely CMOS differential amplifier circuit with the current mirror load and CMOS 2-stage operational amplifier (op-amp). The BSA-DE technique serves as the optimum solution for two typical analogue circuit modes. BSA has a basic framework capable of resolving multimodal issues quickly and effectively. DE is a stochastic heuristic technique based on population and is capable of solving global issues with optimization. In this document, the size of the transistors is optimized with the suggested BSA-DE to decrease the circuit areas and enhance circuit performance. The findings of the simulation validate BSA-superiority DE's in global convergence features and in good tuning capabilities and prove to be a potential option for an optimum CMOS circuit design [9].

D. Comer et al. presented a review on the topic of CMOS Op Amps. In a high speed system, the suggested architecture would be used on chips (SOCs). A fundamental analogue building block of OPAMP implements FinFET's low leakage current, low power dispersion and high-current driving capabilities. Dynamic biasing techniques in this suggested architecture are utilized to improve the OPAMP slew rate. This method can enhance the Common Mode Range (ICMR) input and improve gain stability. A mixed mode device and circulation simulation on FinFET in sub-16-nm node technologies are used to assess the performance of a differential amplifier. The study showed that the common mode rejection ratio of FinFET based OPAMP is 76 dB with an enhanced area, power and bandwidth performance. The design presented is less noise and better than traditional MOSFET in low power nano circuits[10].

3. DISCUSSION

In the nanoscale age of the analogue CMOS concept, it is becoming increasingly vital to understand the physical variables which influence circuit reliability and performance and how they will be mitigated or overcome. The first section of the document provides elements impacting the matching of devices, including devices, and also local and long-haul impacts. Various trustworthiness implications, including physical design restrictions for future downscaling, were explored. It may be advantageous, in certain circumstances, to surpass a few hundred millivolts of the water supply indicated in the foundry. Models that contain the dependency on the form of the output waveform are provided to achieve this. Condition Vsb > 0 needed for setup of the cascode circuit. The role of the other terminal voltages is examined, because in high-scale systems, Vsb > 0 increases both hot and cold carriage damage effects. The second half of the article deals with trends in the properties of the device and its effect on the design of analogue nanoscale CMOS circuits. Several circuit design approaches are being explored to deal with the main ideals of CMOS nanoscale technology. For example, on-chip precise and temperature-insensitive distractions methods, digital analogue circuit calibration and controller and high-voltage circuits design. It is becoming increasingly necessary to achieve excellent energy efficiency in ICs able to house 109 devices. This article also examines the development of analogue to digital conversion figure.

Due to the use of the modified MOS structure with pull-up and pull-down stacked transistors, the differences amplifier gain factor is enhanced to 5 dB compared to conventional differential amp circuits. A 45 nm CMOS technology optimizing proposed CMOS based differential amplifier. The simulations were conducted using the virtual analogue spectrum simulator cadence. The experimental implementations were made using the proposed circuit for the assessment of leakage power and efficiency with greater consistency. The simulated results obtained for both the amplifier circuits show the efficacy, with the convergence speed, specifications and parameters for the optimum design of CMOS amplifier circuits, of the proposed BSA-DE-based method to DE, harmony search (HS),

artificial bee colony (ABC) and PSO. BSA-DE-based design technology has been demonstrated to generate the least area of the MOS transistor for each amplifier circuit, and each designed circuit shows the best performance characteristics such as gain, power dissipation etc.

4. CONCLUSION

The differential amplifier is the initial phase of the operational amplifier. The difference between the two signals is just amplified and any common signal is rejected. Since the CMOS technology extends to the nanoscale range, a number of essential elements must not be tackled and overcome to properly build analogue and physical systems. In the nano scaling age of the analogue CMOS idea, physical factors that impact the reliability and performance of the circuit are becoming more and more important to comprehend. Using the modified MOS structure, the difference gain of the amplifier factor is increased at 5 dB compared with standard differential amp circuits. An MOS Differential Amplifier was studied in this paper. ICMR has explained performance characteristics including gain response, response phase, and slew rate. A MOS differential amplifier for the specified parameters with 800nm technology was developed as an exemplary example. The design was checked using the MAGIC VLSI tool with the help of the NG spice.

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