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IMPACT OF WORK FUNCTION AND TEMPERATURE VARIATION ON SCHOTTKY-BARRIER HETERO-DIELECTRIC GATE ALL AROUND NANOWIRE FIELD EFFECT TRANSISTOR

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Abstract: The GAA MOSFET (Gate All Around Metal Oxide Semiconductor Field Effect Transistor) technology have been considered as suitable one for implementation of digital circuits at nanoscale. The single metal Schottky barrier Source /drain GAA MOSFET devices have been designed using 5nm radius, 10nm channel length, and high-k gate dielectric gate oxide. The electrical characteristics of proposed devices like I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS and DIBL have been evaluated for variable work function and temperature. The proposed devices showed diminished SS and DIBL as compared to existing literature. Hence, these proposed structures are suitable in low power design circuitry.

IndexTerms: **Semiconductor, MOSFET, Nanoscale, Subthrehold Swing, Drain Induced Barrier Lowering**

I. INTRODUCTION

The expeditious advancement of silicon technology is ongoing with present generation technologies of gate lengths less than 22 nm. As scaling of ICs is specified from the Moore's law , which achieved an immense of research in the Nano world. For the circuit designing, MOSFETs were used in silicon era's. Various research articles for the enhancement of short-channel effects of conventional bulk MOSFETs have been published. In the past decade FinFET and Trigate devices have been analysed comprehensively [1, 2].

At the nanoscal,,Bulk CMOS devices are displacing by FinFETs. FinFET dimensions are determined by channel length. The gate configuration improves electrical control over channel conduction and eliminates short channel effects. FinFET is a generic word that refers to any Fin-Based, Multi-gate Transistors. Based on the configuration of FinFET , there are various kinds of FinFETs accessible like double gate FinFET, Multi gate FinFET, TrigateFinFET, Omega –FinFET and All Around Gate FinFET(AAG)[3].

Work function difference of 0.5eV recommended for DMG JNT design, as also for best recifying behaviour[4].The work function difference between the metal contact and the intrinsic silicon body has been used to construct a novel rectifier termed the CP diode. We used palladium (Pd) as the anode and erbium (Er) as the cathode since it has a large workfunction (4.9 eV), as the cathode (4.4 eV).The gate work-functions for the midgap gate and n-polysilicon gate, respectively, are 4.71eVand 4.17eV[5].During the downscaling of transistors, multiple short channel effects are commenced, among them DIBL(Drain Induced Barrier Lowering),SS (Sub-Threshold Swing) are focussed in present work by the variation of temperature and workfuction. For a decade change in drain current, SS is the change in gate voltage. As the channel becomes shorter, DIBL is the potential barrier lowering due to expanded depletion region caused by increased drain voltage. Proposed device has single metal schottky barrier gate all around nanowire FET (SM-SB-GAA NWFET),gives better results by saving resources and easing fabrication and is useful in sub-threshold digital applications that require low power[6-12].

2. Device Modelling

The dopingless single metal hetero- dielectric Gate All Around Nanowire Field Effect Transistor with a concept of charge plasma and source drain schottky contact device configuration has been modelled and shown in figure1 and figure 2,respectively.Figure 3(a) and figure 3(b) shows 2D device structure of designed device and also outlines the asymmetrical distribution of high-K and low-K gate oxide along the length of devices (D1(L1=15nm,L2=5nm)and D2(L1=16nm,L2=4nm)) respectively.

Table 1 shows the design specifications used for designing the proposed structure at the channel length of 20nm. In this work high-k dielectric gate oxide $Hf_xTi_{1-x}O_2$ with permittivity 50 and 70 encloses SiO_2 in cylindrical manner. High-k gate dielectric material rises up the gate capacitance thereby diminishing the leakage current and static power consumption [13].

The proposed devices are simulated using Drift-diffusion model, the Lombardi mobility model, Kane's model through Band to-band tunnelling (GBB) and Shockley Read-Hall (SRH) carrier recombination mechanism [14].

The performance parameters of designed devices such as on-current (I_{ON}), off- current(I_{OFF}),sub- threshold swing(SS),drain induced barrier lowering(DIBL) has been analysed by changing the metal gate work function and temperature .The work function is lying between 4.1eV to 5.0eV and temperature is varied from 300K to 550K . Figure 4 demonstrates the input gate voltage variation with respect to the drain current for different drain voltages of proposed structure [15-18].

The boundary conditions used for evaluating the performance parameters of proposed structure are drain voltage of 0.1V, 1V and ramped gate voltage from 0V to 1V.

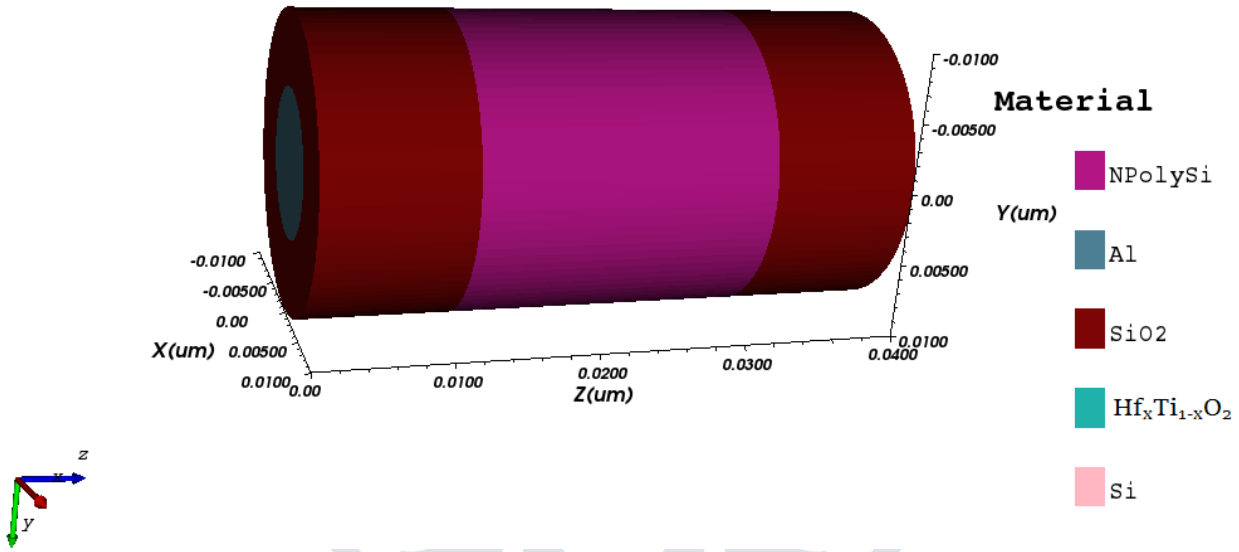

Fig.1. Side view for asymmetrical high-k and low-k gate oxide length along the channel of dopingless single metal hetero- dielectric Gate All Around Nanowire Field Effect transistor(SM HD GAA NWFET).

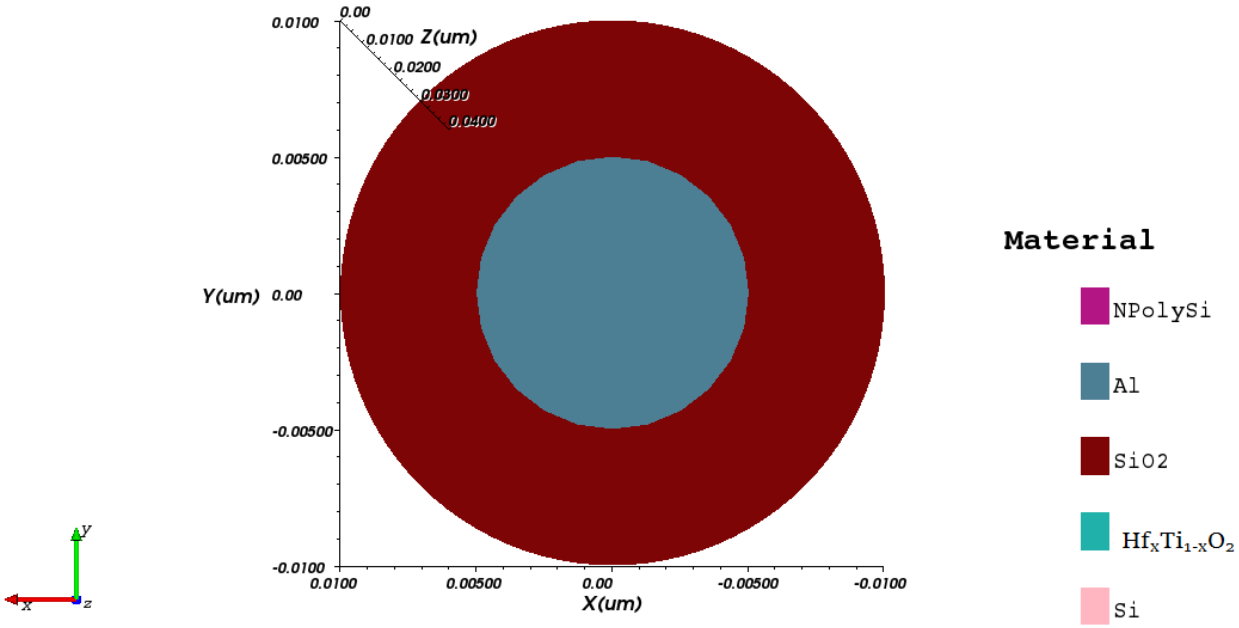

Fig.2.Top view for asymmetrical high-k and low-k gate oxide length along the channel of dopingless SM HD GAA NWFET.

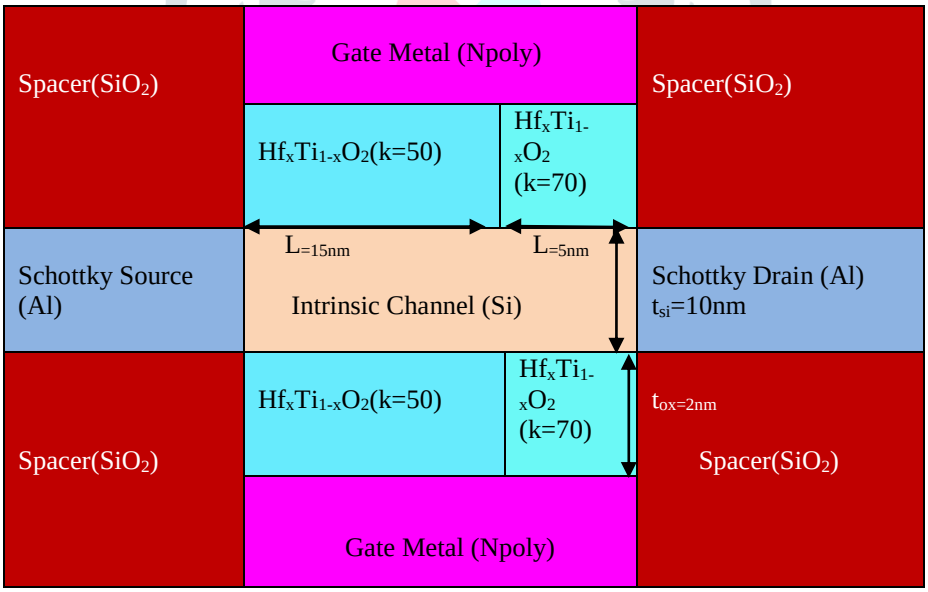

Fig.3(a). 2D structure of dopingless SM HD GAA NWFET,device D1(L1=15nm,L2=5nm)

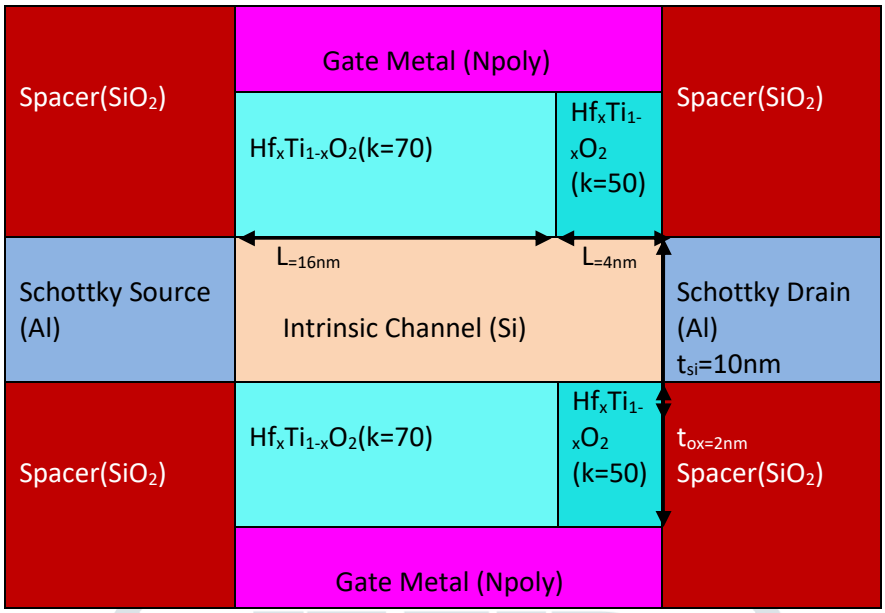

Fig.3(b). 2D structure of dopingless SM HD GAA NWFET,device D2(L1=16nm,L2=4nm)

Table 1.Device Specification of proposed device

Symbol	Parameters	Values
r_{si}	Silicon body radii (nm)	5
t_{ox}	Oxide thickness (nm)	2
$L_{S/D}$	S/D length (nm)	10
φ_G	Work function of gate (eV)	4.6-5.0
L_{si}	Length of si channel (nm)	20
N_{ch}	Doping concentration of channel (cm^{-3})	1E16
$\varphi_{S/D}$	Work function of source/drain (eV)	4.1-4.3

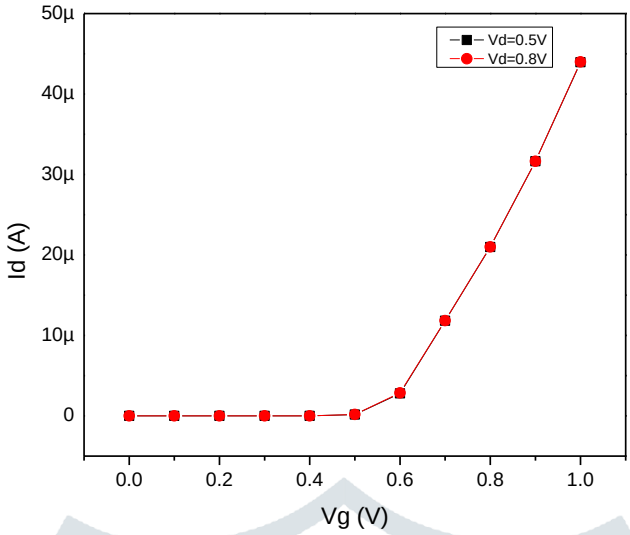

Fig.4. I_d –V_g charachteristics of SM HD GAA NWFET at different drain voltages.

3. RESULT AND DISCUSSION

The proposed device is designed and simulated in Cogenda VISUAL TCAD environment. The electrical characteristics like on-current (I_{ON}), off- current(I_{OFF}),sub- threshold swing(SS),drain induced barrier lowering(DIBL) has been analysed for proposed structure. The on-current is defined as the value of drain current calculated at Vd=0.1V and gate voltage at 1V.The leakage current is referred as drain current estimated at zero input gate voltage. Sub-threshold swing is defined as ratio of change in applied voltage to the decade change in drain current. DIBL (drain-induced barrier lowering) is defined as lowering in the transistor's threshold voltage (Vth) with rising drain voltages [16]. The impacts of variable gate metal, metal source/drain work function and temperature have also been evaluated. The variable ranges of work function and temperature are 4.1eV to 5.0eV and 300K to 550 K, respectively.

3.1. IMPACT OF DIFFERENT GATE AND SOURCE/DRAIN WORK FUNCTION

The gate and source/drain work function plays a very important role in designing high performance nanoscale semiconductor devices. Work function is defined as the energy that is required to remove an electron from a metal surface completely. Thus it is a measure of how a particular metal holds electron tightly. The different combinations of gate and source/drain work function(eV) taken are :C1(4.6-4.1),C2(4.6-4.2),C3(4.6-4.3),C4(4.8-4.1),C5(4.8-4.2),C6(5.0-4.1),C7(5.0-4.2) and C8(5.0-4.3).The influence of different gate and source/drain work functions on device's performance parameters are analysed as follows:

3.1.1. Impact on On –current (I_{ON}) and Leakage current (I_{OFF})

Figure 5(a) and 5(b) indicates the extracted values of I_{ON}(ON- current) and I_{OFF}(OFF-current) for different work function of proposed devices D1(L1=15nm,5nm) and D2(L1=16nm,L2=4nm).From the simulation it has been concluded that ON-current is maximum at the work function combination of C4(4.8eV-4.1eV).The current ratio value of C8 (5.0eV and 4.3eV) work function (WF) combination in Device D1 has been increased by seven times with respect to C1 (4.6eV and 4.1eV) work function (WF) combination as shown in figure5(c).

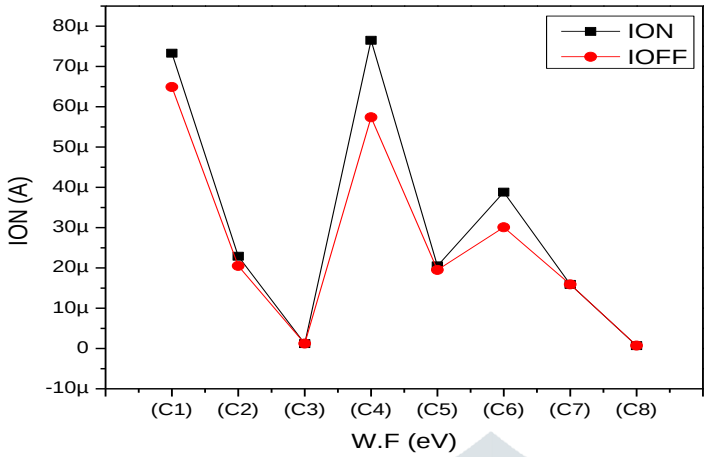

Fig. 5(a).Impact of work function (W.F) on ON-current (I_{ON}) for SM HD GAA NWFET

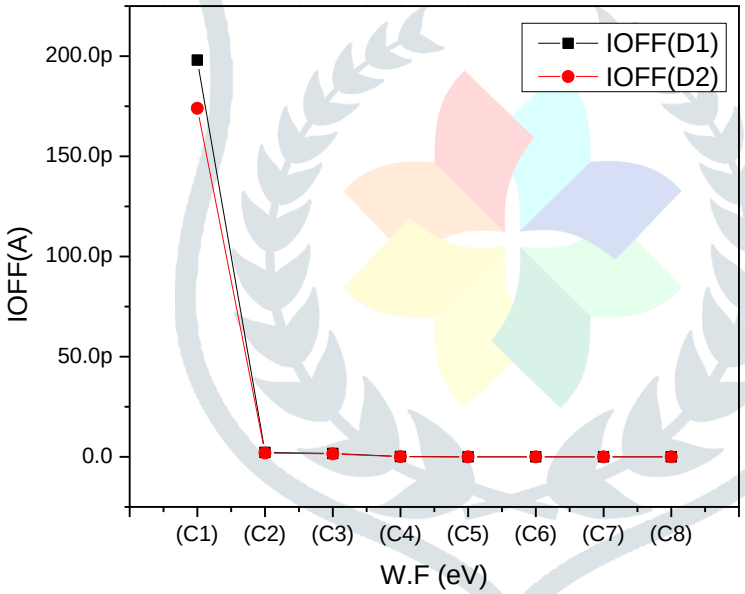

Fig.5(b). Impact of work function (W.F) on OFF-current (I_{OFF}) for device single metal HD SB GAA NWFET.

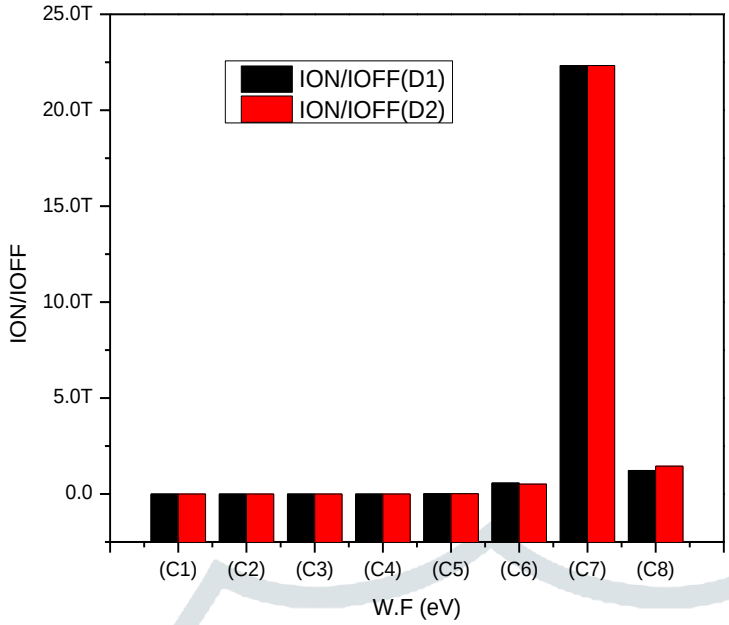

Fig. 5(c).Impact of work function (W.F) on current ratio (ION/IOFF) in structure SM HD GAA NWFET.

3.1.2. Impact of work function on SS and DIBL

As both performance parameters should be minimised for a device because less the short channel effects are, better will be device performance. Simulation shows better results for device D2 in which SS is reduced to 62mV/dec at work function combination of 5.0-4.2eV (C7) and is illustrated in figure 6(a). The sub-threshold swing definition illustrates how current behaves as a function of voltage in an exponential manner and is mathematically calculated as given in equation (1)

$$SS = \frac{\partial V_g}{\partial log_{10} I_D} \quad (1)$$

In MOSFET'S, DIBL (drain-induced barrier lowering) is also one among the short-channel effects that indicates to a lowering in the transistor's threshold voltage (Vth) with rising drain voltages. Among the two designed devices DIBL is much reduced in device D2 (L1=16nm, L2=4nm) to the value of 5.2mV/V for the work function combination of 5.0eV-4.2eV (C7) and is shown in figure 6(b). The SS and DIBL of proposed devices (D1 and D2) have been decreased by 2.7% and above 50% respectively with respect to the referred device [13].

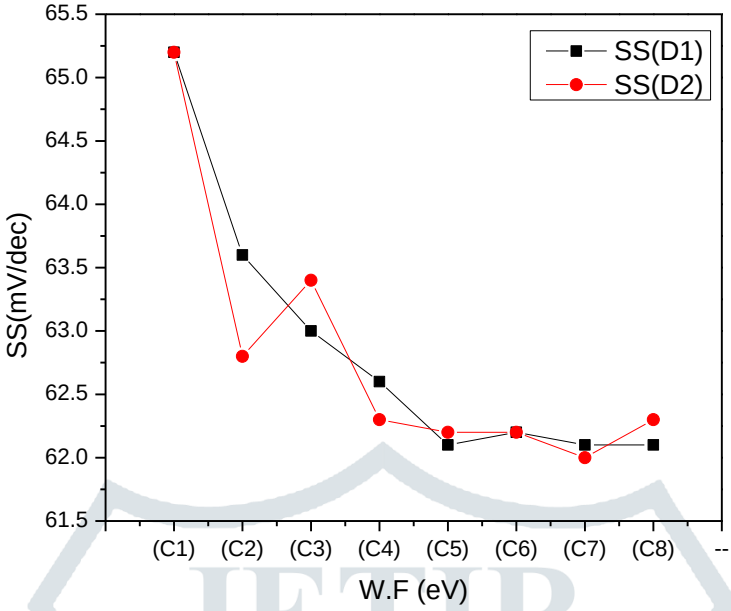

Fig. 6(a).Impact of work function (W.F) on sub-threshold swing (SS) for SM HD GAA NWFET.

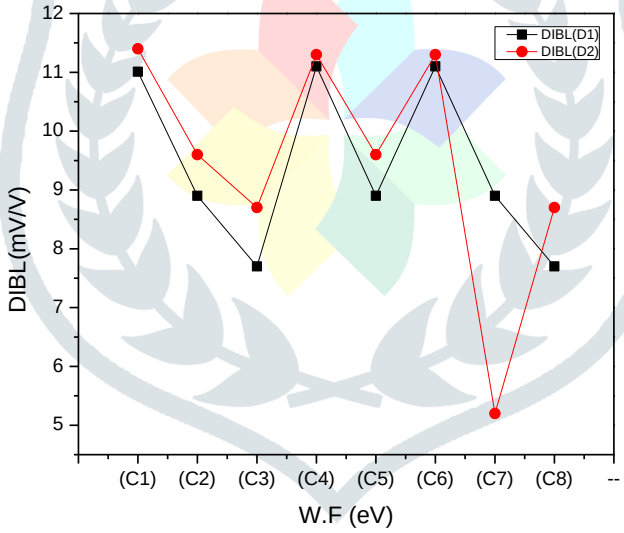

Fig. 6(b).Impact of work function (W.F) on Drain induced barrier lowering (DIBL) for SM HD GAA NWFET.

3.2 IMPACT OF TEMPERATURE VARIATION

The dependence of temperature of various MOSFET settings causes dc characteristics to fluctuate. The drain current reduces as the temperature rises at higher gate to source voltages, indicating that the MOSFET has a negative valence at higher gate to source voltages. The current increases with temperature at decreasing gate to source voltages. As a result, the ON current falls with temperature while the OFF current increases, resulting in poor circuit performance at high temperatures [19].

From the figure 7(a) designed devices concludes that for the device D1(L1=15nm,L2=5nm) ,at temperature 550k , maximum ON-current of 2.55E-05A is obtained as compared to the device D2(L1=16nm,L2=4nm) whose maximum ON-current is 2.11E-05A.

Thus with the increase in temperature, ON-current increases. Simultaneously, with the increase in temperature, OFF-current also increases as shown in figure 7(b) and the least leakage current (I_{OFF}) is observed at temperature of 300k (1.09E-15).

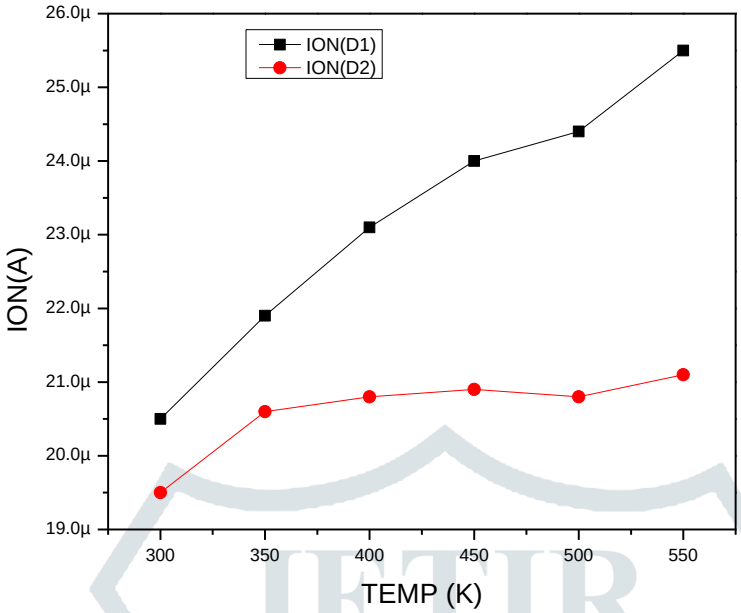

Fig. 7(a).Impact of temperature (TEMP) on On-current (ION) for the device SM HD GAA NWFET.

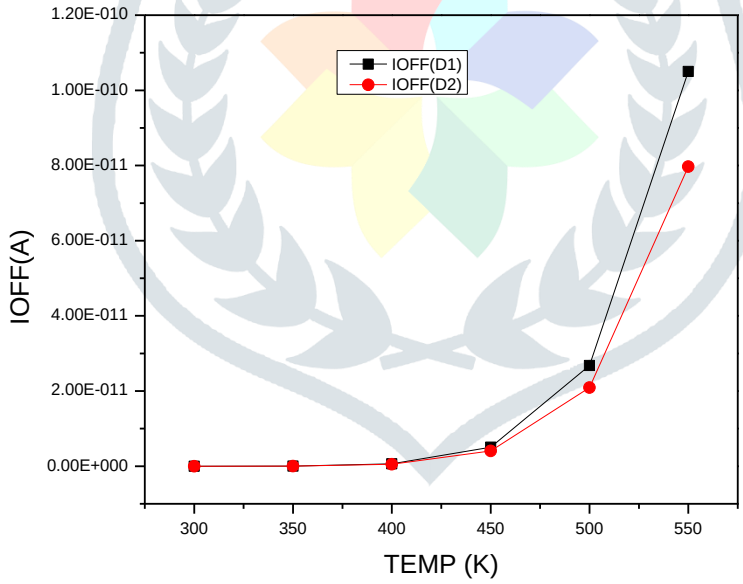

Fig.7(b).Impact of temperature (TEMP) on off-current or leakage current (IOFF) for the device SM HD GAA NWFET.

4. Conclusion

In this work, the electrical characteristics of single metal and Schottky source/drain based GAA MOSFET devices designed using $Hf_xTi_{1-x}O_2$ high-k gate dielectric have been analysed for the channel length of 10nm using Visual TCAD simulator. The impact of work function and temperature variations on these structures have also been evaluated and analysed. It has been observed that the short channel effect parameters viz. SS and DIBL have been reduced by 2.7 % and above 50% w.r.t. device designed by Agam et al.,2019 [13]. Therefore, the proposed devices are suitable in implementation of digital circuits.

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