Five-level Inverter for PV Applications with Reduced Harmonics

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***Abstract :t*—Two-level inverters are popularly used in PV systems to converter DC voltage into AC voltage. But the two-level inverters contains drawbacks like poor harmonic profile, high dv/dt and so on. To address these issues, many multi-level inverters are proposed in the literature. But harmonics are still present at first center and which is equal to switching frequency even with multi-level inverters. In order to shift harmonics to further higher levels, switching frequency has to be increased. If the switching frequency of inverter increases, switching losses increases. The percentage of losses increases further more in medium voltage and high voltage applications. To address this issue, a novel PWM technique for a five-level inverter is presented in this paper. The five-level inverter is developed by using one leg of three-level diode clamped inverter and one leg of two-level inverter. Two isolated DC voltage sources are connected to the entire inverter configuration. By using a novel PWM technique, all harmonics are shifted near to second center band which is equal to two times switching frequency. As availability of isolated dc sources are common in case of different PV system modules, two dc sources can be easily obtained. The proposed inverter is simulated in MATLAB/Simulink and results are presented. The analysis is carried to study the behavior of the inerter during the failure of some switching devices and Dc sources.**

Keywords—Fault tolerant inverters; Multi level- inverters; PV applications; Sine-Triangle PWM.

I. INTRODUCTION

Power generation using PV systems is becoming more popular due to lack of availability of fossil fuels [1]. As power generated with PV system is DC, inverters are required to converter it into AC quantity. Conventional two-level inverters are popularly used in this application. But, the output voltage of these inverter contains more harmonic component which will deteriorates lifetime of the load [2]-[5]. The rate of rise of output voltage (dv/dt) of two-level inverter is also considerably high [6]. If any switch of a two-level inverter fails, entire system will not function [7]. These issues are minimized by using multilevel inverters [8]-[9]. Although conventional multilevel inverters have many advantages, these are suffering with some disadvantages like neutral point voltage balancing issue [10], requirement of more number of capacitor banks [11] and isolated dc sources [12]. To minimize these drawbacks of conventional multilevel inverters, many multilevel inverter configurations were proposed in the literature. An interesting five-level inverter configuration is proposed in [13] which are using only two-level inverters to produce five-level voltage waveform. A multilevel inverter configuration is also proposed in [14]-[15] which will minimize the problems associated with conventional multilevel inverters. On the other hand, reliability is the important issue as the inverters are often used in critical load applications like motor control which drives the critical load and reactive power compensation etc. If anyone switch of the conventional multilevel (neutral point/flying capacitor) inverters fails, the inverter cannot be operated. Moreover, there are many causes for the failure of switching devices/gate driver circuits as these are sensitive parts of inverter circuit. The failure of switching device may occur due to various reasons like aging, miss firing, dv/dt, over voltage, overt current etc. In case of critical loads, failure of inverter circuit causes huge production loss. In this regard an interesting five-level inverter configuration is proposed in [16] which is constructed by using one leg of three-level neutral point clamped inverter and one leg of two-level inverter and a bi-directional switch (four quadrant switch). The main drawback of this inverter configuration is it requires one extra bi-directional switch to operate the inverter during the failure of some switching devices. By extending this concept, a five level inverter configuration is proposed in this paper by using only six switching devices. Moreover first center band harmonics are cancelled by using a noel pwm technique which is more suitable to the proposed inverter configuration. In this pwm technique, gating pulses for three-level inverter leg is produced as presented in [17] which is well known technique. But gating pulses for two-level inverter leg is produced by using the concept presented in the next section.

II DESIGN OF FIVE-LEVEL INVERTER AND PWM TECHNIQUE

The power circuit of a five-level inverter configuration is shown in Fig. 1. It requires eight switching devices and out of these six switching devices are controlled devices and two are uncontrolled diodes. But conventional five-level inverter requires eight controlled switching devices which will increase control complexity of the system. In this inverter circuit, two isolated DC voltage sources with a magnitude of Vdc/2 are used to feed entire configuration. The voltage rating of control switches S_1 and S_2 is equal to V_{dc}. The voltage rating of control switches S_3 to S_6 is equal to $V_{dc}/2$. All these six switching devices are conventional two quadrant switches. During the voltage level V_{dc}, the switching devices S_1, S_5 and S_6 will conduct and the switching devices S_1, S_4 and S_5 will conduct for the voltage $V_{dc}/2$ as shown in Fig.2. Similarly the switching devices S_2, S_5 and S_6 will conduct for zero voltage level. The negative voltage level $V_{dc}/2$ can be produced by switching S_2, S_4 and S_5 and negative V_{dc} can be produced by switching S_2, S_3 and S_4. In this way five voltage levels can be produced at the output of inverter.

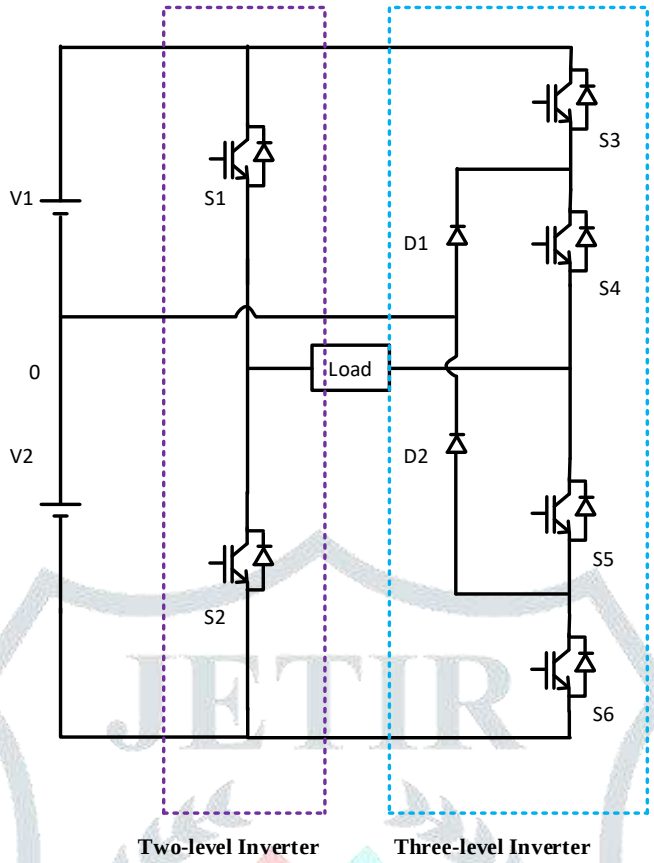


Fig. 1: Power circuit of a five-level inverter Topology.

But in this PWM technique, decoupled PWM concept is used to produce gating signals for each switch of the inverter. Fig. 1 shows two separate legs of two-level inverter and three-level inverter. The gating signals for two-level inverter leg is produced by using one sine wave and two carrier waves as shown in Fig. 3(a). If modulating signal is greater than top carrier wave then S_1 will be conducting and if modulating signal is less than bottom carrier signal then the switch S_2 will be conducting. Modulating and carrier signals used for three-level inverter are shown in Fig. 3(b). Here modulating signal is phase shifted by 180^0 compared with modulating signal of other modulating signal and carrier signals are in phase with each other. Logic to generate gating signals for three-level inverter leg is shown in Table I.

TABLE I
POSSIBLE SWITCHING COMBINATIONS TO GENERATE FIVE-LEVEL VOLTAGE WAVEFORMS

Switches / Voltage Levels	S_3	S_4	S_5	S_6	Modulating and carrier waves
$+V_{dc}/2$	ON	ON	OFF	OFF	M > C1
0	OFF	ON	ON	OFF	C1 < M < C2
$-V_{dc}/2$	OFF	OFF	ON	ON	C2 < M

(M-Modulating signal, C1- Top carrier and C2- bottom carrier)

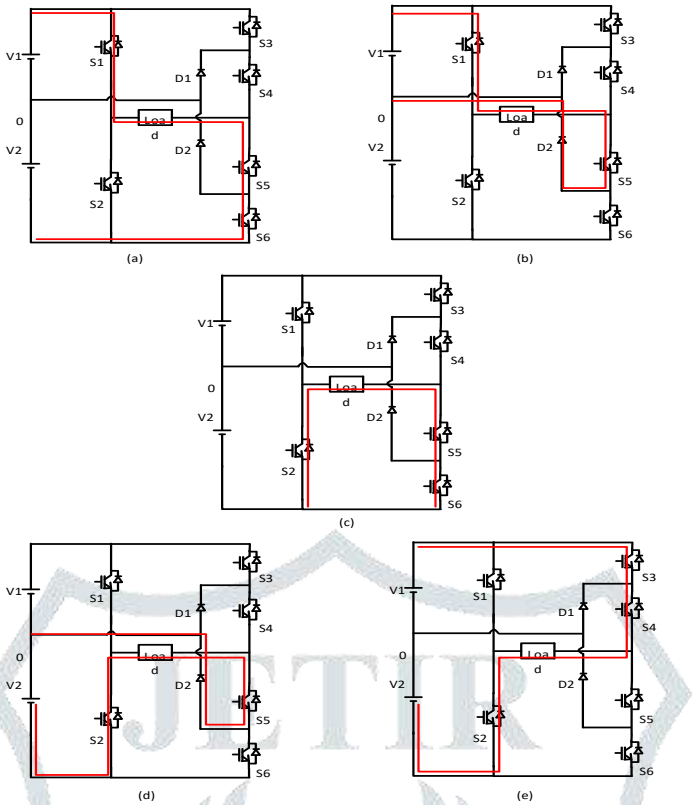
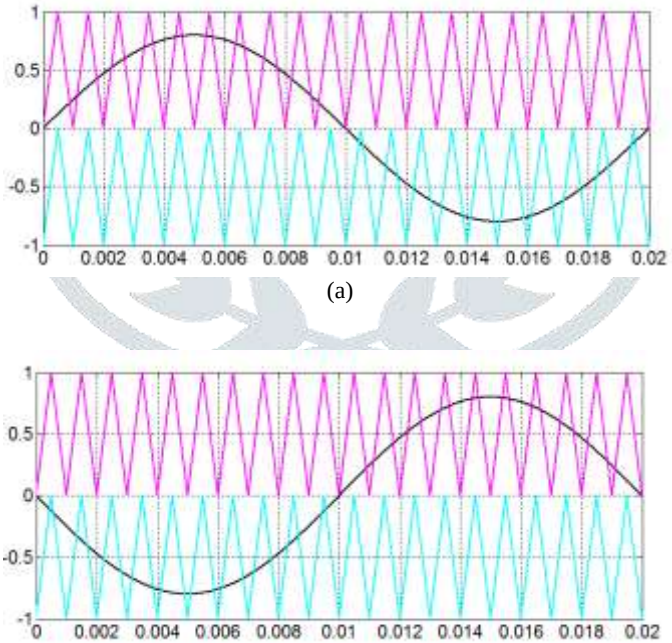


Fig. 2: Power circuits for getting five-level voltage wave forms (a) V_{dc} (b) Vdc/2 (c) Zero (d) $-V_{dc}/2$ and (e) $-V_{dc}$.

By providing 180^0 phase shift between modulating signals, harmonics will be shifted to two times the switching frequency. The harmonic spectrum of output voltages will be presented to show the cancellation of harmonics at first center band and it is presented in the next section.



(a)

(b)

Fig. 3: Proposed PWM technique for five-level inverter (a) modulating and carrier waves for two-level inverter (b) modulating and carrier waves for three-level inverter.

IV. Results and Discussion

The proposed five-level inverter configuration is simulated in MATLAB/Simulink and results are presented. The dc voltage source magnitude of V_{dc} is taken as 100V and load resistance of 10Ω and inductance of 50mH.

The voltage across the load and current through it are shown in Fig.4. From Fig. 4, it is clear that, five-level voltage waveform is produced. As total voltage is divided five voltage levels, dv/dt of the output voltage is also reduced. It is also clear from Fig.4 that, current waveform is sinusoidal as the voltage waveform is almost sinusoidal.

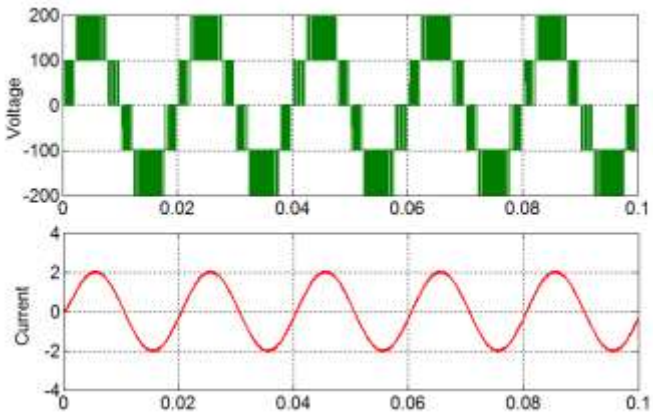


Fig.4: Top trace is the load voltage and bottom trace is the load current of a five-level inverter.

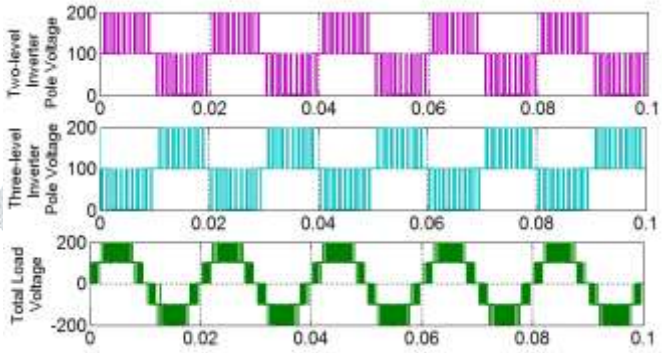
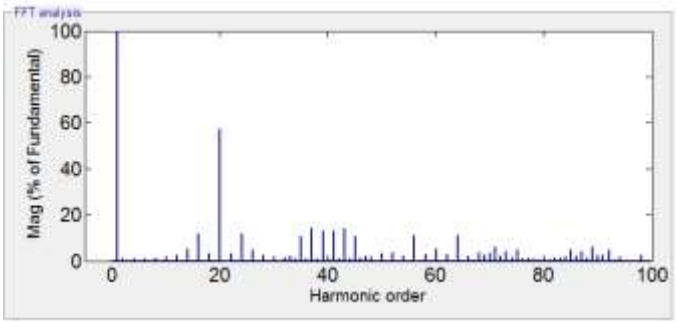
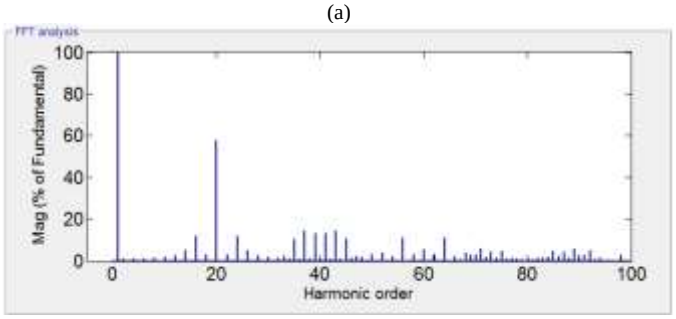


Fig.5: Top trace is the pole voltage of two-level inverter leg and second trace is the pole voltage of three-level inverter leg and bottom trace is the total voltage across load.

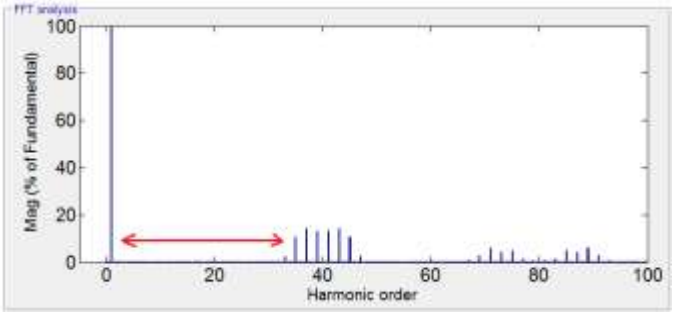
Fig.5 shows the two-level inverter pole voltage and three-level inverter pole voltage and output voltage. As gating pulses for two-level inverter are produced by using two carrier signals, pole voltage of two-level inverter is almost similar to three-level inverter output voltage. Fig. 6(a) shows harmonic spectrum of two-level inverter pole voltage where harmonics are present near to first center band which is equal to switching frequency. Similarly Fig. 6(b) shows the harmonic spectrum of three-level inverter pole voltage where harmonics are present near to first center band. As the modulating signals of two-level inverter and three-level inverter are phase shifted by 180^0, all odd center band harmonics are also phase shifted by 180^0. As effective voltage is the difference of both inverter pole voltages, all odd center band harmonics are cancelled.



(a)



(b)



(c)

Fig.6: Harmonic spectrum of output voltage (a) Harmonic spectrum of two-level inverter pole voltage (b) Harmonic spectrum of three-level inverter pole voltage (c) Harmonic spectrum of total voltage.

By using proposed inverter configuration and PWM technique all center band harmonics are shifted to two times the switching frequency.

V. CONCLUSION

A five-level inerter with decoupled PWM technique is proposed in this paper. All harmonics are shifted to two times the switching frequency without increasing switching frequency. To achieve this decoupled SPWM technique is used for this configuration. Harmonic spectrum and different voltage waveforms are presented to show the validity of proposed inverter configuration. Requirement of switching devices is reduced in this inverter configuration compared to conventional five-level inerter configuration. Moreover, control complexity of the proposed inverter is also less compared to conventional five-level inverter. The same inverter can be operated as a three-level inverter and two-level inverter during the failure of different switching devices. Whereas conventional neutral point clamped inverter/flying capacitor inverter cannot be operated during the failure of any one switching device. The proposed inverter circuit is simulated using MATLAB/Simulink. The number of voltage levels can be increased further by cascading these units.

REFERENCES

[1] K. Nallamekala, S. Dandabatthina and V. K. Tella, "A novel fault tolerant 21-level inverter configuration for PV applications," 2017 International Conference on Circuit ,Power and Computing Technologies (ICCPCT), Kollam, 2017, pp. 1-7.

[2] H. s. Patel and R. G. Haft "Generalized techniques of harmonic elimination and voltage control in thyristor inverters Part I: Harmonic elimination", IEEE Trans. Ind. Applicat vol. IA-9, pp.310 -317 1973.

[3] K. K. Nallamekala, M. Kalyan U and S. K, "Harmonic reduction technique with a five-level inverter for four pole induction motor drive," *2013 1st International Future Energy Electronics Conference (IFEEC)*, Tainan, 2013, pp. 482-487.

[4] J. Chatzakis, M. Vogiatzaki, H. Rigakis, M. Manitis, E. Antonidakis "novel High Bandwidth Pulse-Width Modulated Inverter", Proceedings of the 10th WSEAS International Conference on CIRCUITS, Vouliagmeni, Athens, Greece, July 10-12, 2006 pp280-285.

[5] Donald Grahame Holmes, Brendan P. McGrath "Opportunities for Harmonic Cancellation with Carrier-Based PWM for Two-Level and Multilevel Cascaded Inverters", Industry Applications, IEEE Transactions on Vol. 37, No. 2, March/April 2001.

[6] K. K. Nallamekala, B. S. Umesh and K. Sivakumar, "A five-level inverter topology for four pole induction motor drive using four two-level inverters and two isolated DC sources," *2014 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Mumbai, 2014, pp. 1-5.

[7] Y. Takami; T. Kato; K. Inoue, "General-Purpose Computation Method of a Power Converter for Frequency Characteristics - Application to Stability Analysis of a Grid Inverter -," in IEEE Journal of Emerging and Selected Topics in Power Electronics , vol.PP, no.99, pp.1-1.

[8] Rodriguez, J.; Jih-Sheng Lai; Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol.49, no.4, pp.724,738, Aug 2002.

[9] Mohan M., Renge and Hiralal M. Suryawanshi, "Five-Level Diode clamped Inverter to eliminate Common Mode Voltage and Reduced dv/dt in Medium voltage rating Induction Motor Drives," IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1598–1607, Jul. 2008.

[10] Kai Tian; Bin Wu; Narimani, M.; Xu, D.D.; Zhongyuan Cheng; Reza Zargari, N., "A Capacitor Voltage-Balancing Method for Nested Neutral Point Clamped (NNPC) Inverter," in Power Electronics, IEEE Transactions on , vol.31, no.3, pp.2575-2583, March 2016.

[11] Druant, J.; Vyncke, T.; De Belie, F.; Sergeant, P.; Melkebeek, J., "Adding Inverter Fault Detection to Model-Based Predictive Control for Flying-Capacitor Inverters," in Industrial Electronics, IEEE Transactions on , vol.62, no.4, pp.2054-2063, April 2015.

[12] Rabinovici, R.; Baimel, D.; Tomasik, J.; Zuckerberger, A., "Thirteen-level cascaded H-bridge inverter operated by generic phase shifted pulse-width modulation," IET Power Electron., vol.6, no.8, pp.1516,1529, September 2013.

[13] K. K. N. and K. Sivakumar, "A Quad Two-Level Inverter Configuration for Four-Pole Induction-Motor Drive with Single DC Link," in IEEE Transactions on Industrial Electronics, vol. 62, no. 1, pp. 105-112, Jan. 2015.

[14] Babaei, E.; Laali, S., "Optimum Structures of Proposed New Cascaded Multilevel Inverter With Reduced Number of Components," in Industrial Electronics, IEEE Transactions on , vol.62, no.11, pp.6887-6895, Nov. 2015.

[15] Babaei, E.; Laali, S.; Bayat, Z., "A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches," in Industrial Electronics, IEEE Transactions on , vol.62, no.2, pp.922-929, Feb. 2015.

[16] Madhukar Rao, A.; Sivakumar, K., "A Fault-Tolerant Single-Phase Five-Level Inverter for Grid-Independent PV Systems," in Industrial Electronics, IEEE Transactions on , vol.62, no.12, pp.7569-7577, Dec. 2015.

[17] Nallamekala, K.K.; Sivakumar, K., "A Fault-Tolerant Dual Three-Level Inverter Configuration for Multipole Induction Motor Drive With Reduced Torque Ripple," in Industrial Electronics, IEEE Transactions on , vol.63, no.3, pp.1450-1457, March 2016.