An Innovative fifteen level inverter

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Abstract

This paper presents a single-phase multilevel inverter topology. An algorithm for the configuration of asymmetric sources for the fifteen level multilevel inverter is being proposed. This topology comprises simple logic of various difference combination of the DC source. The simulation is performed in MATLAB – SIMULINK and the simulation results show the effectiveness to attain the fifteen level output voltage and an acceptable harmonic distortion as per standard norms and conditions.

Keywords: *Asymmetric Multilevel inverter, DC source, PWM control techniques, THD*

INTRODUCTION

Unlike several decades ago, the electrical power now can be generated from diverse sources, namely fuel cells, photovoltaic, tidal, batteries are cells generally produce energy in dc form which needs to be converted into ac source necessitating an inverter. A single Semiconductor switch is not proper for high power conversion since the current and voltage rating of a switch is not appropriate for high power conversion. Hence, the use of multiple semiconductor switches makes it possible for voltage and current sharing between the semiconductor switches and thereby the power transformation happens with better efficiency. For increasing voltage levels the number of switches also will increase in number. Henceforth the voltage stresses and switches loss will increment and the circuit will end up the complex. By utilizing the proposed topology number of switches will diminish fundamentally and consequently, the proficiency will move forward. In high power applications, the consonant substance of the output waveforms must be lessened however much as could reasonably be expected with a specific end goal to stay away from twisting in the lattice and to achieve the most extreme vitality proficiency. In this paper, the idea for fifteen level output has been proposed. Also the proposed Modulation scheme has the benefit of low switching frequency.

PROPOSED TOPOLOGY FOR FIFTEEN LEVEL

The idea received for the proposed topology is that the inverter ought to be fit for integrating all conceivable added substance and subtractive blends of the DC levels of the information sources. All the possible combinations are depicted in table 1.

Table 1: Output for different DC source combination

Number of DC source	Number of output level	Number of state
1	v1, 0, v2	3
2	v1,v2,0,-v1,-v2,(v1+v2),(v1-v2),-(v1+v2),-(v1-v2)	9
3	V1,v2,v3,0,-v1,-v2,-v3,(v1+v2) ,(v1+v3) ,(v2+v3),(v1-v2) ,(v1-v3) ,(v2-v3) ,-(v1+v2) ,-(v1+v3) ,-(v2+v3) -(v1-v2) ,-(v1-v3) ,-(v2-v3),(v1+v2+v3) ,(v1+v2-v3) ,(v1-v2+v3) ,(v1-v2-v3), (-v1+v2+v3) ,(-v1+v2-v3) ,(-v1-v2+v3) ,(-v1-v2-v3)	27
M	All the possible state	3^m

We can obtain a generalized structure of number of levels equal to "m". Their voltage can be assigned as v1 , v2 …….Vm. Then all the possible connections can be attained by proceeding in same manner as done one, two, and three DC source. Here fig.3 shows the proposed inverter structure with three DC source.

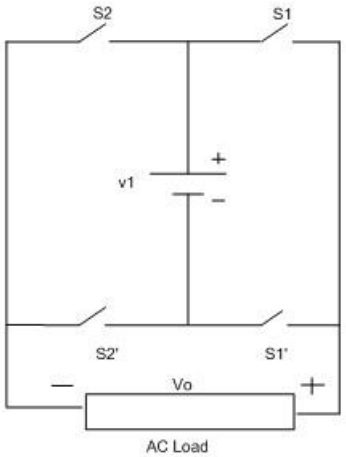

Fig. 1: Proposed topology with one DC source.

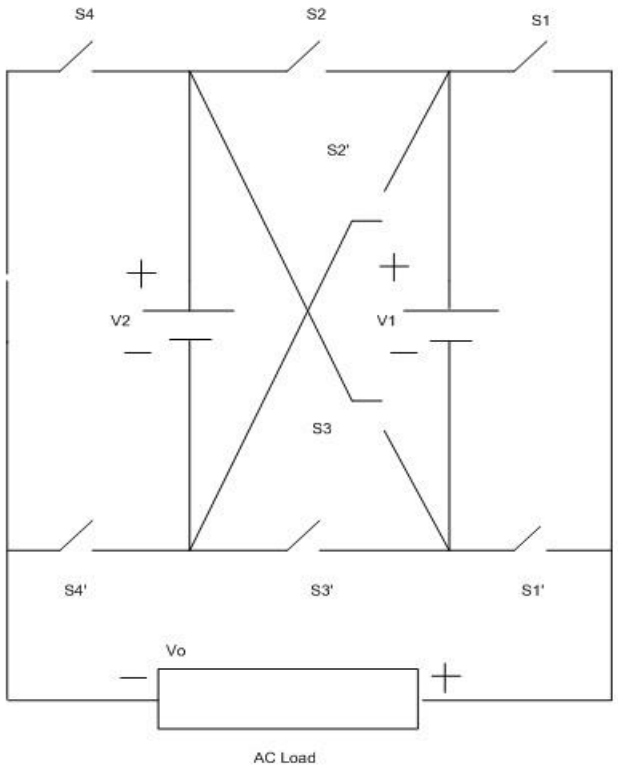

Fig. 2: Proposed topology with two DC source.

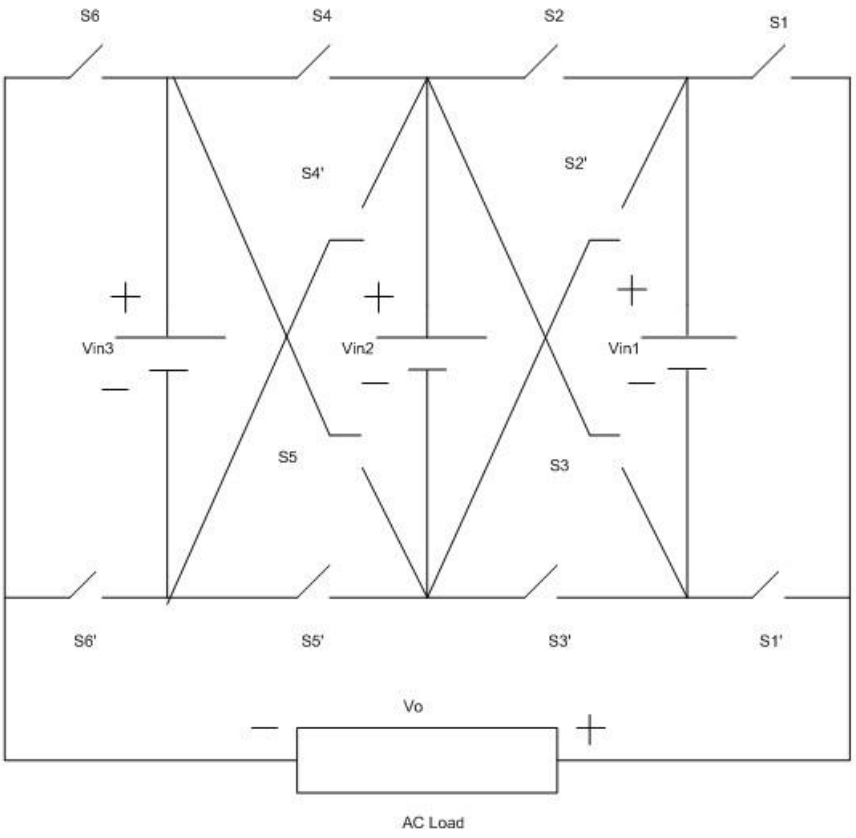

Fig. 3: Proposed topology with three DC source.

A. FIFTEEN LEVEL PROPOSED TOPOLOGY:

A fifteen level topology segment diagram has been depicted in fig. 3. This proposed topology utilizes three DC source. Table 2 is lookup table for switching states for fifteen level topology. In this table for a given number of switches, when the selected switches are in ON state, rest of alternate switches stay in OFF state. Equations given below, gives how many switches and output levels.

Number of switches required = 4m … (1)

Number of levels in the output voltage = 6m-3 … (2)

Number of reduction states = 2^{2m} -4m+1 … (3)

Where m is number of DC sources.

Table 2: Lookup table for switching states for fifteen level

Level of signal	Voltage output level(v1=v2=90v ,v3=30v)	Switches in ON state			
7	v1+v2+v3	S1	S3	S5	S6’
6	v1+v2	S1	S3	S5’	S6’
5	v1+v2-v3	S1	S3	S5’	S6
4	v1+v3	S1	S3	S4	S6’
3	v1	S1	S3’	S5’	S6’
2	v1-v3	S1	S3’	S5’	S6
1	v3	S1	S2	S4	S6’
0	0	S1	S2	S4	S6
-1	-v3	S1’	S3’	S5’	S6
-2	v3-v1	S1’	S2	S4	S6’
-3	-v1	S1’	S2	S4	S6
-4	-v1-v3	S1’	S2’	S5’	S6
-5	v3 –v1-v2	S1’	S2’	S4	S6’
-6	-v1-v2	S1’	S2’	S4	S6
-7	-v1-v2-v3	S1’	S2’	S4’	S6

B. MODULATION SCHEME:

A multilevel inverter is used for synthesizing a staircase waveform which imitating sine wave. It is advance improved by multicarrier PWM methods. A variety of multilevel modulation arrangements are summarized in. The control Systems can be extensively named PWM and stepped. When the number of output level is high, then carrier based PWM control techniques is used. This paper presents,

Fourteen triangular waveforms of 400 Hz frequency being used in carrier waveform and a sinusoidal waveform of 50 Hz frequency used as reference wave. Fig 4 is Schematic diagram of PWM techniques.

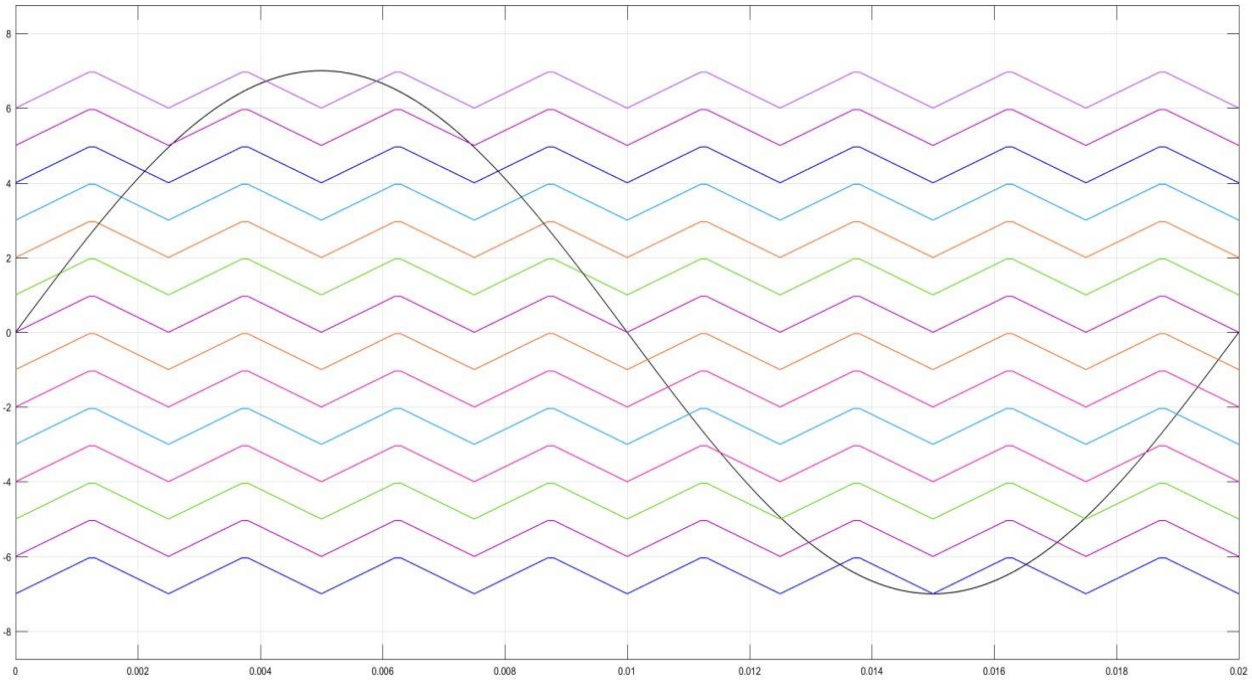

Fig. 4: PWM technique for fifteen level topology

SIMULATION RESULT

The execution of the proposed topology is approved by playing out the recreation of a fifteen level inverter in MATLAB/SIMULINK. Three DC source v1=v2= 132v and v3=44v. The load is considered for the simulation, where Active power is 215w and Reactive power is 160 var. The output waveform and harmonic analysis are shown in fig5,6 and 7.

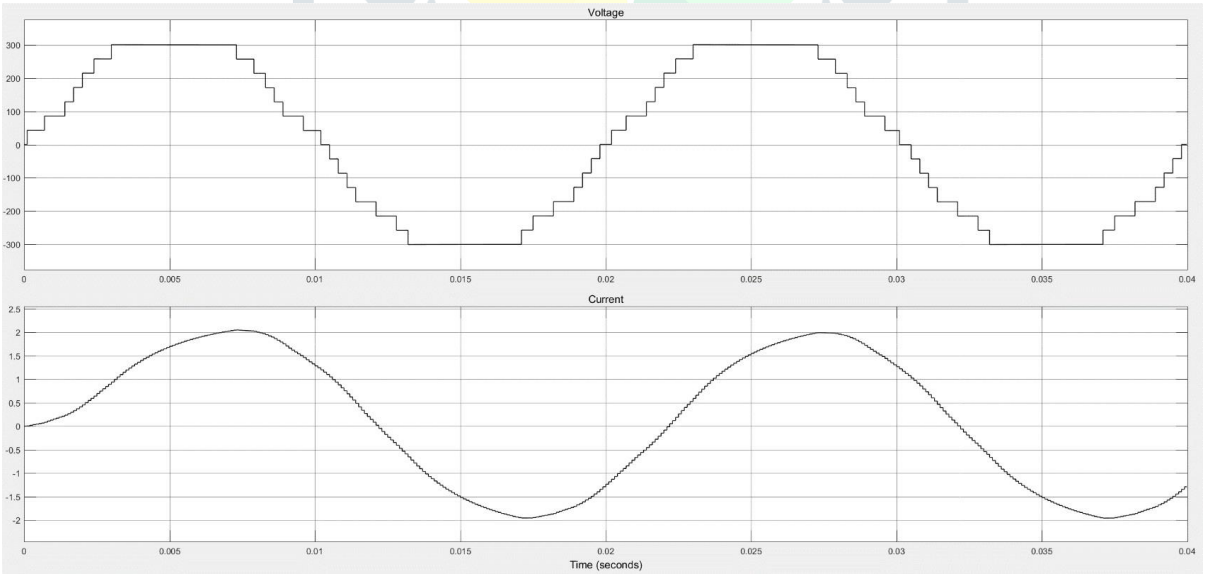

Fig. 5: Output waveform for fifteen level inverter

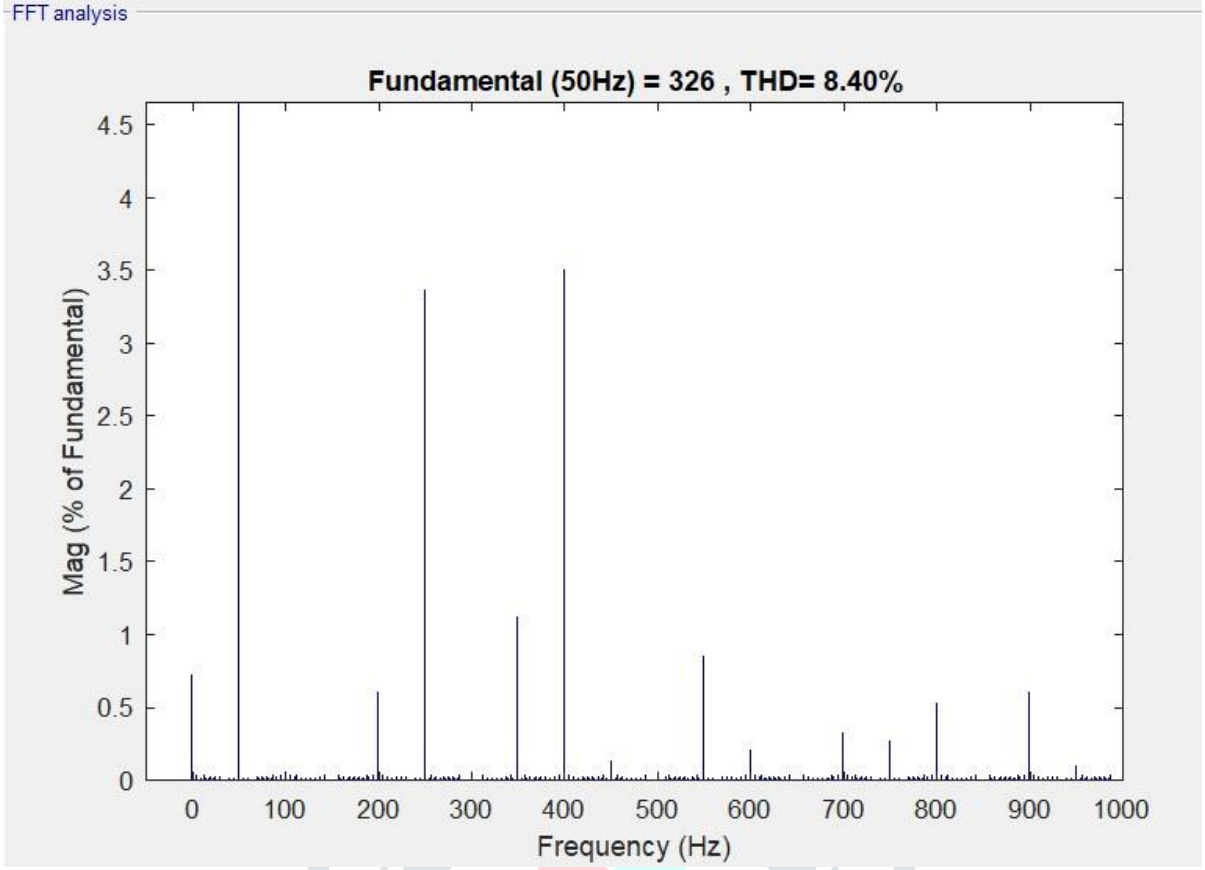

Fig. 6: FFT analysis for voltage waveform

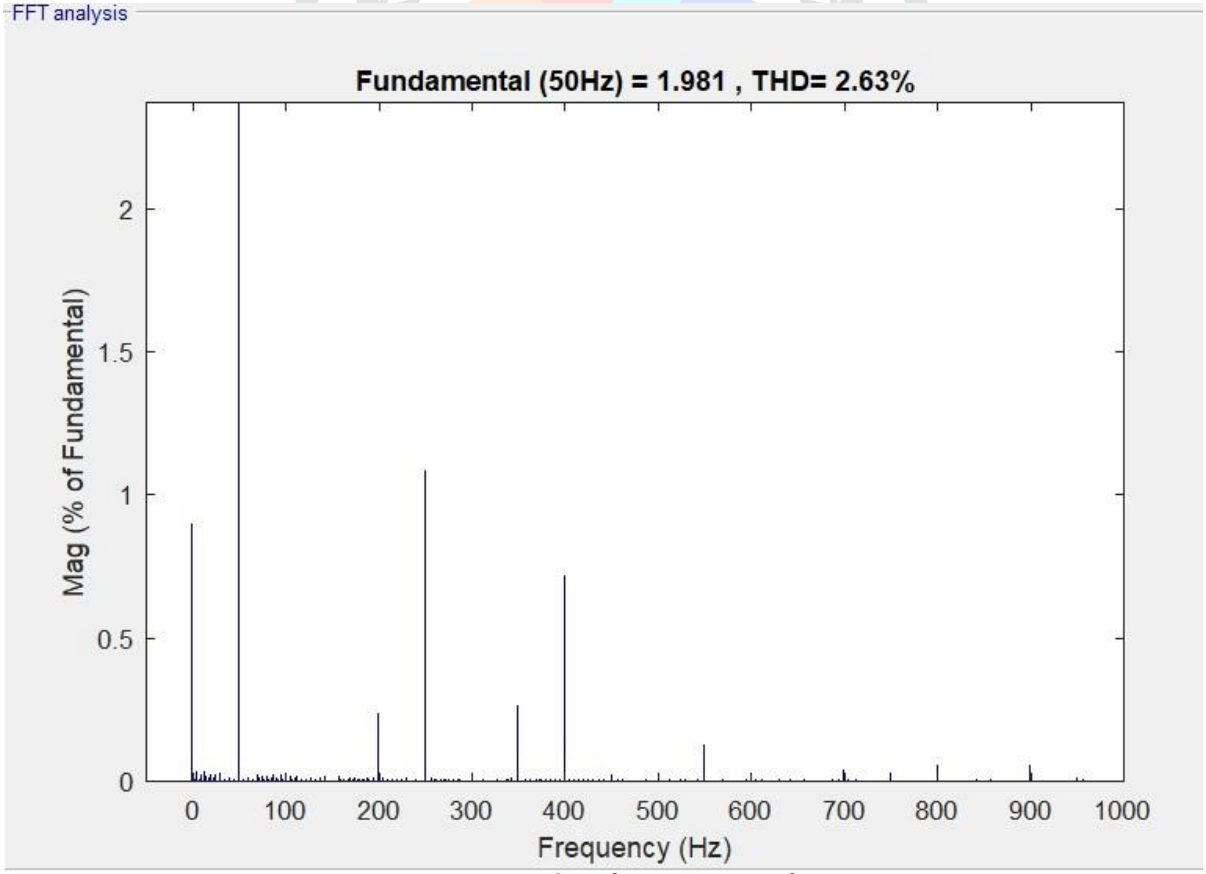

Fig. 7: FFT analysis for current waveform

CONCLUSIONS

In this paper, a new structure is proposed for multilevel inverter. The proposed work/simulation gives less THD using the optimal or minimal components. It has been saw that, THD level is found 2.63%, which is under 5% as per rules given in IEEE 519.

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