Reconfigurable Low Area Complexity Filter Bank Architecture for Software Defined Radio

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***Abstract*— The ability to support multiple channels of different communication standards, in the available bandwidth, is of importance in modern software defined radio (SDR) receivers. An SDR receiver typically employs a channelizer to extract multiple narrowband channels from the received wideband signal using digital filter banks. Since the filter bank channelizer is placed immediately after the analog-to-digital converter (ADC), it must operate at the highest sampling rate in the digital front-end of the receiver. Therefore, computationally efficient low complexity architectures are required for the implementation of the channelizer. The compatibility of the filter bank with different communication standards requires dynamic reconfigurability. The design and realization of dynamically reconfigurable, low complexity filter banks for SDR receivers is a challenging task. This paper reviews some of the existing digital filter bank designs and investigates the potential of these filter banks for channelization in multi-standard SDR receivers.**

***IndexTerms*— Software defined radio , Channelization . Digital filter banks . Reconfigurability . Low complexity**

I. INTRODUCTION

The ability to support multiple channels of different communication standards, in the available bandwidth, is of importance in modern software defined radio (SDR) receivers. The most computationally demanding block in the digital front-end of a software defined radio (SDR) receiver is the channelizer which operates at the highest sampling rate. Channelizers are employed in the SDR receivers for extracting individual channels (frequency bands) from the digitized wideband input signal. SDR can be regarded as an ultimate communications solution which can ideally cover any cellular communication standard in a wide frequency spectrum with any modulation and bandwidth. An SDR receiver typically employs a channelizer to extract multiple narrowband channels from the received wideband signal using digital filter banks. Since the filter bank channelizer is placed immediately after the analog-to-digital converter (ADC), it must operate at the highest sampling rate in the digital front-end of the receiver. Therefore, computationally efficient low complexity architectures are required for the implementation of the channelizer. The compatibility of the filter bank with different communication standards requires dynamic reconfigurability[3]. SDR can be regarded as an ultimate communications solution which can ideally cover any cellular communication standard in a wide frequency spectrum with any modulation and bandwidth. FPGA based channelizers are essential components and enable channel selection to be configurable based on the end application. The goal is to obtain maximum use of a single design through software reconfiguration of hardware assets and dynamic configuration and selection of channels, while ensuring highest level of fidelity of signals received at the destination[4].

II. MOTIVATION

The wireless industry has been experiencing an exponential growth with the emergence of new radio access technologies and standards. All these technologies have been optimized to obtain a good trade-off between data rate, range and mobility to suit specific application needs. Lack of harmony in spectrum allocation globally has alsoresulted in this growth. However, with the increase in trade relationship between different continents, researchers had to look for a common multi-standard wireless communication platform which can support all these radio technologies and standards. This has resulted in the birth of the software defined radio (SDR) concept. SDR can be regarded as an ultimate communications solution which can ideally cover any cellular communication standard in a wide frequency spectrum with any modulation and bandwidth.

III. LITERATURE REVIEW

Hentschel T. in paper [1] entitled "Channelization for software defined base-stations*"* proposed the Per-Channel (PC) Approach. It is based on a parallel arrangement of many one channel channelizers.The basic architecture of the PC approach is shown in figure 1. In figure 1, the order of channelization is filtering (H0(z) to Hn(z), digital down conversion (DDC), sample rate conversion (SRC) and finally baseband processing (BBP).The filter, H0(z), is a low pass filter and all other filters, H1(z) to Hn(z)), are bandpass filters. It is possible to do digital down conversion followed by filtering and consequently, all the filters will be low pass filters (all

filters are H0(z)). It is also possible to further reduce the complexity of the PC approach by employing polyphase decomposition ofeach of the filters and then moving the SRC to the left of filtering operation (i.e.,performing SRC before filtering).By employing polyphase decomposition, the speed of filtering operation can be relaxed[1].

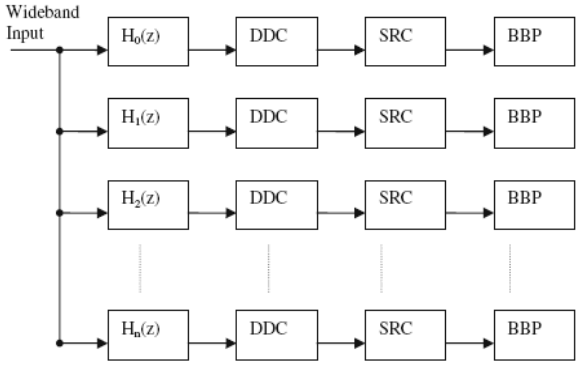

FIGURE 1: PER-CHANNEL APPROACH BASED CHANNELIZATION

The PC approach is a straightforward approach and hence relatively simple. But the main drawback is that, the number of branches of filtering-DDC-SRC is directly proportional to the number of received channels i,e. the complexity of the PC approach is directly proportional to the number of channels. Hence the PC approach is not efficient when the number of received channels is large. The filters used in the PC approach are of a very high order and this results in high area complexity and thus increased static power.

Pucker, L. in paper [2] entitled "Channelization techniques for software defined radio" proposed DFT Filter Banks. DFT filter bank is a uniformly modulated filter bank, which has been developed as an efficient substitute for PC approach when the number of channels need to be extracted is more, and the channels are of uniform bandwidth (for example many single standard communication channels need to be extracted). The main advantage of DFT filter bank is that, it can efficiently utilize the polyphase decomposition of filters. The limitations of DFTFBs is that the channel filters have fixed equal bandwidths corresponding to the specification of a given standard. DFTFBs cannot extract channels with different bandwidths known as non uniform channels, because they are modulated FBs with equal bandwidth for all bandpass filters. If the channel bandwidth is very small compared to wideband input signal (extremely narrowband channels), the prototype filter must be highly selective resulting in very high-order filter. As the order of the filter increases, the complexity increases linearly. Also the DFT size needs to be increased. Reconfigurability is another key requirement as we had mentioned earlier.

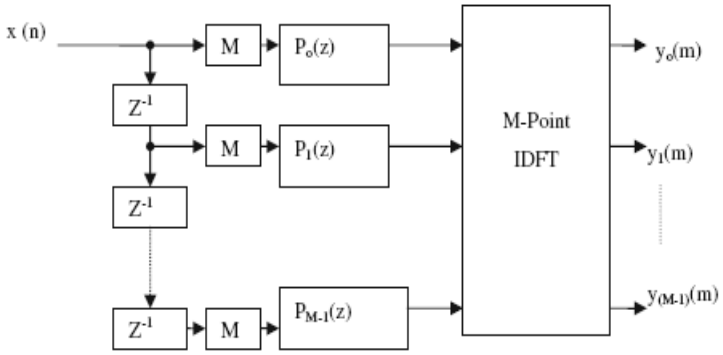

FIGURE 2 : DFT FILTER BANK.

Ideally, the reconfigurability of the filter bank must be accomplished by reconfiguring the same prototype filter in the filter bank to process the signals of the new communication standard with the least possible overhead, instead of employing separate filter banks for each standard. However reconfiguration of DFTFB suffers from following overheads: 1. The prototype filter needs to be reconfigured. Generally DFTFB employs the polyphase decomposition. Hence reconfiguration can involve changing the number of polyphase branches which is a tedious and expensive task. 2. Downsampling factor needs to be changed. If down sampling is to be done after filtering, then we need separate digital down converters. This will add more cost. 3. The DFT needs to be reformulated accordingly which is also expensive[2].

R. MAHESH et.al. in paper [3] entitled "Reconfigurable Low Area Complexity Filter Bank Architecture Based on Frequency Response Masking for Non uniform Channelization in Software Radio Receivers" proposed a new reconfigurable FB based on the FRM approach for extracting multiple channels of non uniform bandwidths. The FRM approach is modified to achieve following advantages: 1) incorporate reconfigurability at the filter level and architectural level, 2) improve the speed of filtering operation, and 3) reduce the complexity.

The advantage of conventional FBs such as PC approach and DFTFBs is that they can be implemented in the polyphase decomposed form .While doing so, the speed of operation of the filters can be reduced significantly. This will also result in reduced dynamic power consumption. But the filters used in the PC approach and DFTFB are of a very high order and this results in high area complexity and thus increased static power. Hence it is important to reduce the area complexity and thus static power consumption. This technique is an attempt towards design of FBs with reduced area complexity and improved reconfigurability when compared with conventional resampling-based FBs. The frequency response masking (FRM) technique was originally proposed for designing low complexity sharp transition-band finite impulse response (FIR) filters. A reconfigurable low complexity channel filter for SDR receivers based on the FRM technique was proposed. The objective of the work was to realize a channel filter to extract a single channel (frequency band) from the wideband input signal. Thus the method is more suited for SDR handsets where only one channel needs to be extracted at a given time. However, in SDR base station receivers, simultaneous extraction of multiple channels of multiple communication standards would be required. Therefore, an FB that is capable of extracting multiple channels of non uniform bandwidths corresponding to different wireless standards is needed in a base station. New low complexity reconfigurable architecture is as follows:

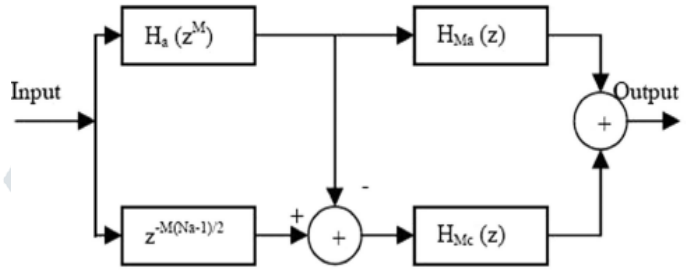

FIGURE 3 : FIR FILTER ARCHITECTURE BASED ON FRM TECHNIQUE.

FIR filters are employed as channel filters because of their linear phase property and guaranteed stability. Sharp transition-band FIR filters are required in the channelizer to meet the stringent wireless communication specifications. In conventional FIR filter designs, higher order filters are required to obtain sharp transition-band. The complexity of FIR filters increases with the filter order. One of the major concerns regarding the implementation of FRM-based architectures is the excessive use of memory, i.e., memories corresponding to delay in the structural adder line (z^{-M}) and that for obtaining complementary delays, Z^{-M}(Na-1)/2.

I. OVERALL ANALYSIS OF REPORTED WORK

It can be stated as from the table that the FRMFB architecture offers the lower area and delay in operation followed by DFTFB and PC approach. From Table 1, it can be noted that the FRMFB architecture offers area reduction of 85% over the PC approach and 67.3% over DFTFB. In FRMFB, the reduction in the number of multiplications when compared with other FBs is more than four times when compared with the complexity imposed by the delays and hence result in low area complexity implementations as can be seen from Table 1.

Table 1: Analysis of reported work

Metrics	Ref.1 PC Approach	Ref.2 DFTFB	Ref.3 FRMFB
Area (mm2)	50.738	23.2077	7.591
Delay (ns)	43	32.4	18.65

IV. PROBLEM DEFINITION / FORMULATION

The per-channel (PC) approach is an efficient channelization approach, if the number of channels to be received is low. But the complexity of the PC approach is directly proportional to the number of channels. Hence the PC approach is not efficient when the number of channels is large.

Efficient implementations of a channelizer using discrete Fourier transform (DFT) filter banks (DFTFBs) are available. A uniform DFTFB can be realized by implementing one low-pass filter (LPF) and a corresponding modulator such as DFT. The limitation of the DFTFB is that the channel filters have fixed equal bandwidths corresponding to the specification of a given standard. The limitations of DFTFBs for SDR receiver applications is that DFTFBs cannot extract channels with different bandwidths known as

non uniform channels. Therefore, for multi-mode receivers, distinct DFTFBs are required for each communication standard. Hence the complexity of channelizer increases linearly with the number of standards.

In reconfigurable FB based on the FRM approach conventional FIR filter designs are used. so, higher order filters are required to obtain sharp transition-band. The complexity of FIR filters increases with the filter order. One of the major concerns regarding the implementation of FRM-based architectures is the excessive use of memory, i.e., memories corresponding to delay in the structural adder line (z^{-M}) and that for obtaining complementary delays, Z^{-M}(Na-1)/2.

VI . OBJECTIVE

The objectives of the proposed design are best described as below:

- Reduction in area of overall design has to be done by designing the blocks like adders and multipliers with having lowest complexity.
- We have to optimize the delay of design by using barrel shifter (a circuit that shifts multiple bits at a time).

VII . PROPOSED METHODOLOGY

It is well known that one of the efficient ways to reduce the complexity of multiplication operation is to realize it using shift and add operations. In contrast to conventional shift and add units are used in previously proposed reconfigurable filter architectures.

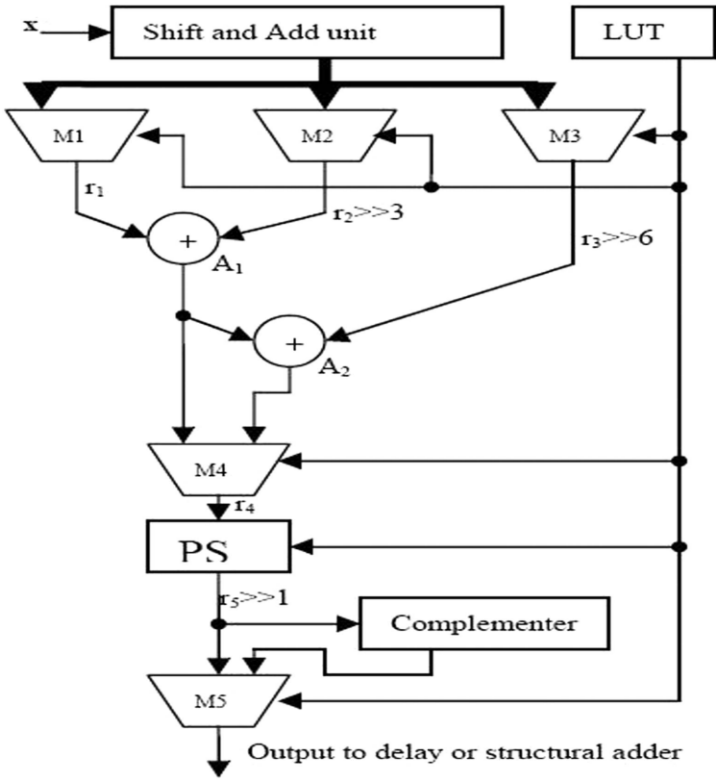

FIGURE 4: PROPOSED RECONFIGURABLE FILTER ARCHITECTURE.

A *programmable shifter* is more complex. Often the speed of multiplication *limits* the performance of the digital processor. So, we can use barrel shifter (a circuit that shifts multiple bits at a time) in proposed architecture instead of programmable shifter. The time required/delay will considerably improve by doing this and the proposed architecture is modified for reducing its complexity.

Barrel shifters have the ability to shift data words in a single operation over standard shift left or shift right registers that utilize more than one clock cycle. Barrel shifters will continue to be used in smaller devices because it has a speed advantage over software implemented ones. In general, it can be concluded that a barrel-shifter is appropriate for smaller shifters. For large shift

values, the log shifter becomes more effective, in terms of area and speed. Also log shifter is more regular and hence can be easily generated automatically.

In reconfigurable FIR filter architectures based on a binary sub-expression elimination (BSE) algorithm has been proposed. The architecture is consisted of a shift and add unit which will generate all the 3-bit BCSs using 3 adders. The proposed architecture of the filter for an 8-bit coefficient is shown in figure.4. M1 and M2 are 8:1 multiplexers; M3 is a 4 : 1 multiplexer and M4 and M5 are 2 : 1 multiplexers. The input is given to the shift and add unit whose output is shared among the multiplexers.

VIII . PROBABLE OUTCOME

- The proposed architecture will inherently be less complex with respect to area.
- The proposed architecture will have optimized delay.

IX. TOOLS / PLATFORM

- Xilinx software
- Altera FPGAs

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