Design and Simulation of Quantum Cellular Automata Based XOR Gate With Optimize Complexity and Cell Count

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***Abstract*— Quantum dot Cellular Automata (QCA) is a recent and potentially attractive technology to implement computing architectures at the nano scale. The basic primitive in QCA is the majority gate. The QCA cells have features on the very low nanometer scale, much smaller than the present state of art size of the smallest transistor. In this paper we present a novel implementations for XOR gate using QCA cells with minimum complexity, minimization of clock require for getting output and cell count in comparison with the already proposed designs. The proposed circuit was varied using simulation from QCA-designer tool. The proposed QCA implementation is useful for building more complex circuits.**

***Index Terms*—QCA, XOR gate, QCA-designer.**

I. INTRODUCTION

Quantum Cellular Automata (QCA) is a nanotechnology that has recently been identified as one of the most emerging technology with potential application in future generation processing units [1, 2] as the CMOS technologies approach [3, 4] its fundamental physical limits in the recent years to development of nanotechnology for future generation ICs [5, 6].In the recent years QCA gets popularity to create computing devices and implementing any logic function. The basic design block of QCA circuit is majority gate; hence, constructing QCA circuits using majority gates has attracted a lot of attentions [7, 8]. Lot of studies has reported that QCA can be used to implement general purpose computational and memory circuits. QCA achieved high device density, fast switching speed, room temperature operation and very low power consumption, compare to any recent emerging technology [2].

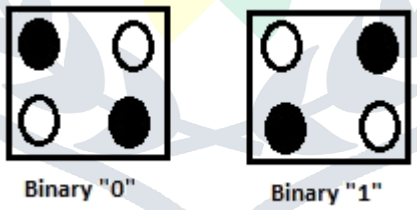


Figure 1: Quantum cellular automata.

The objective of this paper is to design a novel XOR gate by which we design a half adder circuit, here we also implement detailed design, layout and simulation of combinational circuits [9]. We proposed an optimal design for XOR based half adder circuit. The aim is to maximize the circuit density and focus on the layouts that are simple and minimal in their use of cells. The proposed QCA circuits have been designed and simulated using the QCA designer tool [10]. The rest of the paper is organized as follows. In section 2, provide a brief background to QCA technology, in section 3 we design a novel XOR gate, in section 4 we simulate and compare the proposed design with previous existing methods. Finally we conclude this paper in section 5.

II. QUANTUM-DOT CELLULAR AUTOMATA (QCA)

Quantum technology has gradually applied in various field, Quantum dot cellular automata is projected as a promising nanotechnology for future ICs. QCA technology is based on the interaction of bi-stable [7, 8] QCA cells constructed from four quantum dots. The cell is charged with the help of two free electrons which are able to tunnel between adjacent dots. These electrons tend to occupy antipodal sites as a result of their mutual electrostatic repulsion. Thus there exist two equivalent energetically minimal arrangements of the two electrons in the QCA cell, but no current flows into or out of the cell [11, 12] as shown in fig.1.

These arrangements are denoted as cell polarization P=+1 and P=-1. Using these two cell polarization P= +1 which represents "1" and P= -1 represents "0", binary information is en-coded in the charge configuration of the QCA cell [13, 14]. Unlike conventional logic circuits in which information is transferred by electrical current, QCA operates by the Columbic interaction that connects the state of one cell to the state of its neighbors, which results in a technology of which information transfer is the same as information transformation. One of the primary logic gates in QCA is the majority voter (MV). The basic logic function in majority voter is MV(A,B,C)=AB+BC+CA, which can be realized by only five QCA cells, as shown in fig.2(a)and fig.2(b) shown the logical block diagram of a majority gate. Logical AND (fig. 3. (a)) and OR (fig. 3 (b)) function can be implemented from the majority voter by fixing one input(control input) permanently to a 0 or 1. The inverter is another one basic gate in QCA and is shown in fig.3(c). The interconnected fabric bus is shown in fig.3 (d).

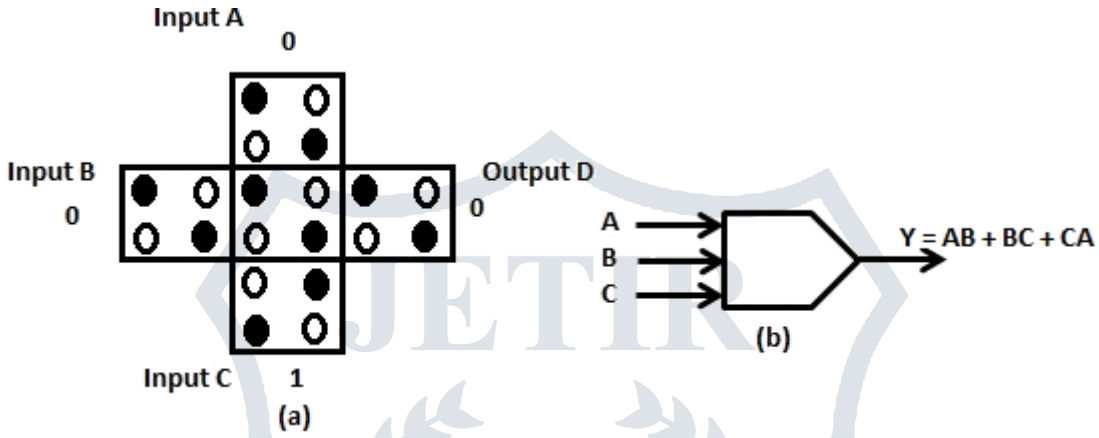


Figure 2: (a) A QCA majority voter gate, (b) Basic block diagram of a QCA MV gate.

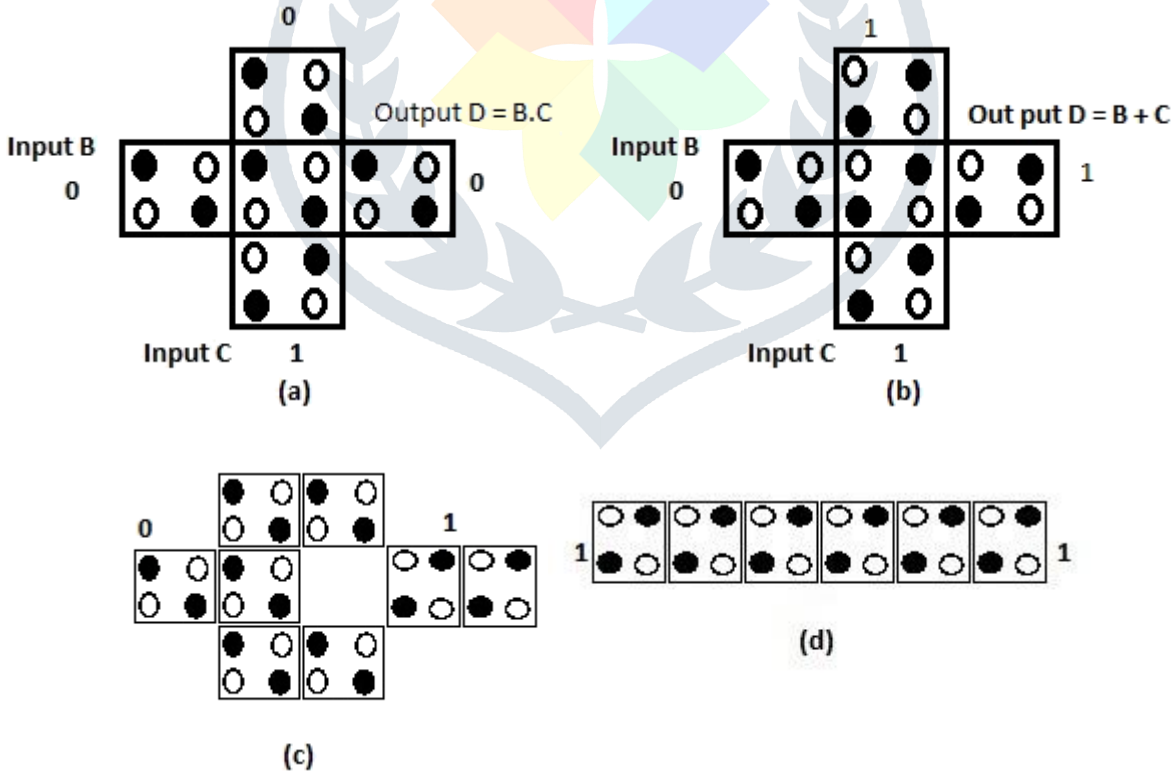


Figure 3: (a) QCA AND gate,(b) QCA OR gate,(c) QCA inverter gate and (d) QCA bus.

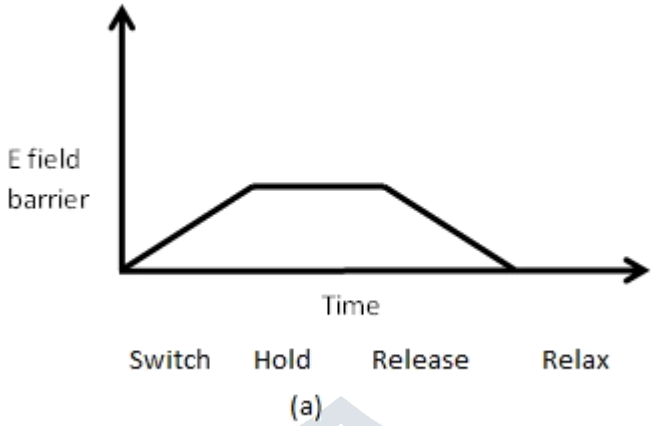


Figure 4: Four phase QCA Clocking.

Several advantages any one can get using QCA technology like it is “edge driven" means an input is brought to an edge of a QCA block; it is evaluated and output at another edge. This also means that no power lines need be routed internally. QCA systems should be very low power, because there is no current owing. Only enough energy needs to add to lift the electrons from their ground states. Finally we can say that the required space for a circuit is very small as because the size of QCA cells are very small. In VLSI design, clocking is control by a reference signal, but in QCA the timing is accomplished by clocking in four different and periodic states as shown in fig4. A QCA circuit is divided into one dimensional zones and every zone is maintained in a phase. The use of quasi-adiabatic switching technique for QCA circuits requires a 4-phased clocking signal, which is commonly supplied by CMOS wires buried under the QCA circuitry for modulating the electric field. These four phases are treated as Relax, Switch, Hold and Release [15, 16]. During the first phase the actual computation takes place therefore the inter-dot barrier is slowly raised and a cell attains a definitive polarity under the incense of its neighbors. During the second phase, barriers are high and a cell remains its polarity. During the third phase, barriers are lowered and a cell loses its polarity and finally in the last phase, there is no inter-dot barrier and a cell remains un-polarized. Timing zones of a QCA circuit are arranged by the following periodic execution of these four clock phase. There must be a latch between two clocking zones. A signal is latched when one clocking zone goes into Hold phase and acts as input to the subsequent zone. Clocking system provides inherent pipelining [17, 18] and allows multi-bit information transfer for QCA by signal latching. As because a zone in the Hold phase is followed by a zone in the switch phase. Designs are partitioned along one dimension, thus effectively creating columns of clocking zones. The clocking signal is applied through an underlying CMOS circuitry which produces required electric field to modulate the tunneling barrier of all cells in the zones.

III. EARLIER WORK

In article [19], three approaches to design a XOR gate have been proposed, where first one require 44 no. of cells and four nos. of clock are applied, second approach require 55 nos. of cells and four nos of clock and third approach require 62 nos. of cells and four nos. of clock to design a XOR gate. In article [20] authors proposed seven different implementation of XOR gate. first one require 34 number of cells, four number of clocks are required to execute the circuit and here 4 number of majority gates are required to complete the design of the circuit.

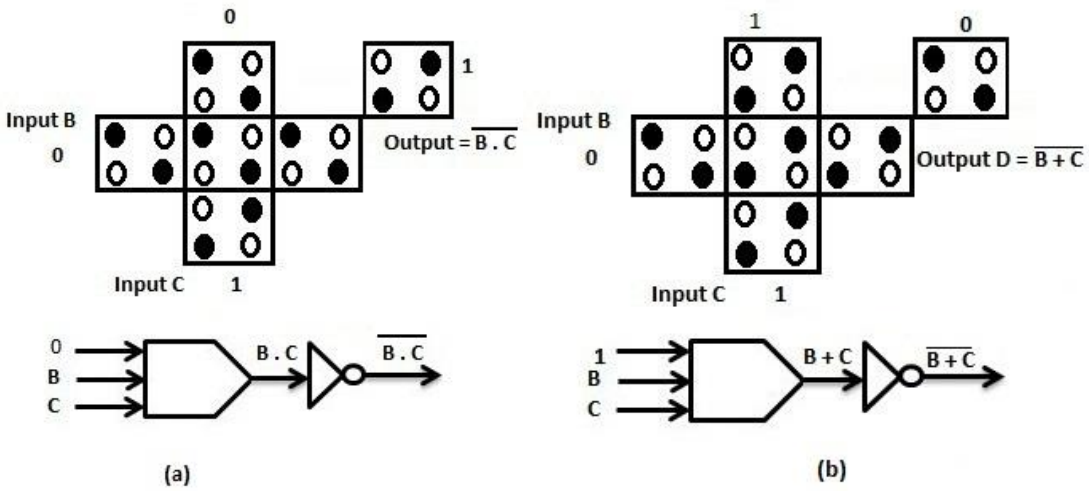


Figure 5: (a) QCA NAND gate, (b) QCA NOR gate.

IV. QCA IMPLEMENTATION

Basic logic gates AND and OR realized by fixing the polarization to any one of the input of the majority gate to either P=-1 treated as logic "0" or P=+1 treated as logic "1". The NAND can be implemented by inverting the output of AND gate fig. 5(a) shows the logic design of a NAND gate using QCA cells. Similarly the NOR gate is implemented by connecting OR gate followed by an inverting gate, fig. 5(b) shows the implementation of NOR gate just arranging the last two cells such that it acts like an inverting gate followed by the majority voter gate.
This two cell inverting circuits can minimize the area and complexity of any circuits.

QCA Implementation of Proposed XOR gate

The basic gates like AND, OR and NOT and the universal gates NAND and NOR are require to design a digital logic circuits. In addition of these gates Exclusive-OR (XOR) and Exclusive-NOR (XNOR) gates are also used to design a digital circuits. The XOR and XNOR gates are particularly useful in arithmetic operations as well as error-detection and correction circuits. These gates are usually found as two-input gates. There is no multiple-input XOR/XNOR gates are available since they are complex to fabricate with hardware.
The XOR gate can give the following logic operation:

$$A \oplus B = \bar{A}.B + A.\bar{B}$$

The representing symbol and the truth table of XOR gate is shown in fig. 6(a) and (b). In digital logic
XOR is a logical value depending on the two inputs and the logical value of XOR is true only if odd number of input is true otherwise the logical value is false. This forms a fundamental logic gate in many operations to follow. In digital logic if the specific type of gate is not available then it may be constructed by other available gates. An XOR gate can be trivially constructed from the basic gate AND, OR and NOT gates. However, this approach requires five gates of three different kinds. The expression of XOR gate D = $\bar{A}.B + A.\bar{B}$ can be represented by basic gates shown in fig. 7. We propose the QCA design and layout of XOR gate based on basic logic gates arrangements, the proposed design layout is shown in fig. 8(a), this layout require only two clock cycle and consist of only 32 number of QCA cells(including inputs and output cells) and an area of approximately also there is no cross over in the circuit.

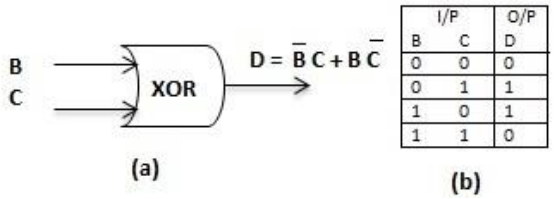


Figure 6: (a) XOR gate Graphical Symbol, (b) XOR gate truth table.

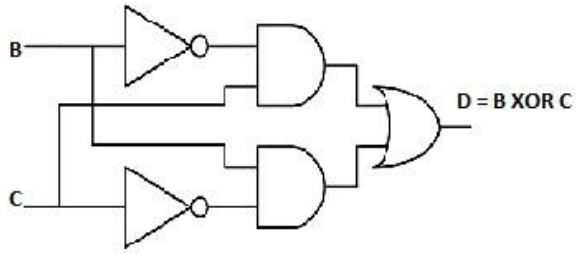
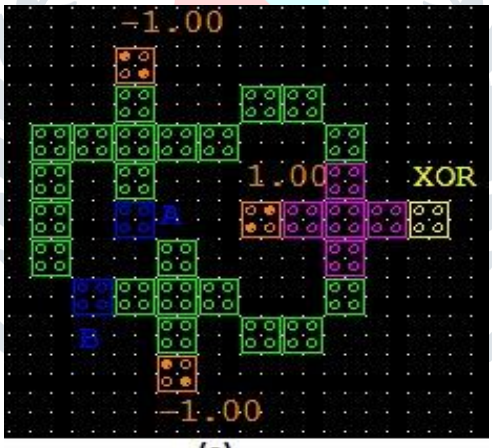


Figure 7: Implementation of XOR gate.

Simulation Results and Comparisons

To design the proposed circuit layout and functionality checking, we use a simulation tool for QCA circuits
QCA Designer version 2.0.3.The following default parameters are used for bitable approximation: cell size=18nm, clock high=9.800000e-022J, clock low=3.800000e-023J and Dot diameter=5nm. Fig.8 (b) shows the simulation results of proposed XOR gate. As we have identified that it is also possible to reduce the complexity (cells number), area and can increase the density up to some extent, in immediate manner we started to look for a new implementation methodology for XOR gate which is so simple and efficient. For the same we have applied a conventional approach, we used three majority gates where two are used for performing AND operations and one is used for OR operation. In our proposed circuit design method we have used 32 numbers of QCA cells and accordingly circuit area is reduced and it is comparatively dense enough and also there is 180^{o} of delay: Table 1 gives the comparison of proposed design with several previous designs [19, 20]. It is evident from table 1 that the proposed designs are efficient in terms of cell count, majority gate, delay, crossover and area to simulate circuits. The proposed design layout can be easily used to design complex circuits based on XOR operation.



(a)

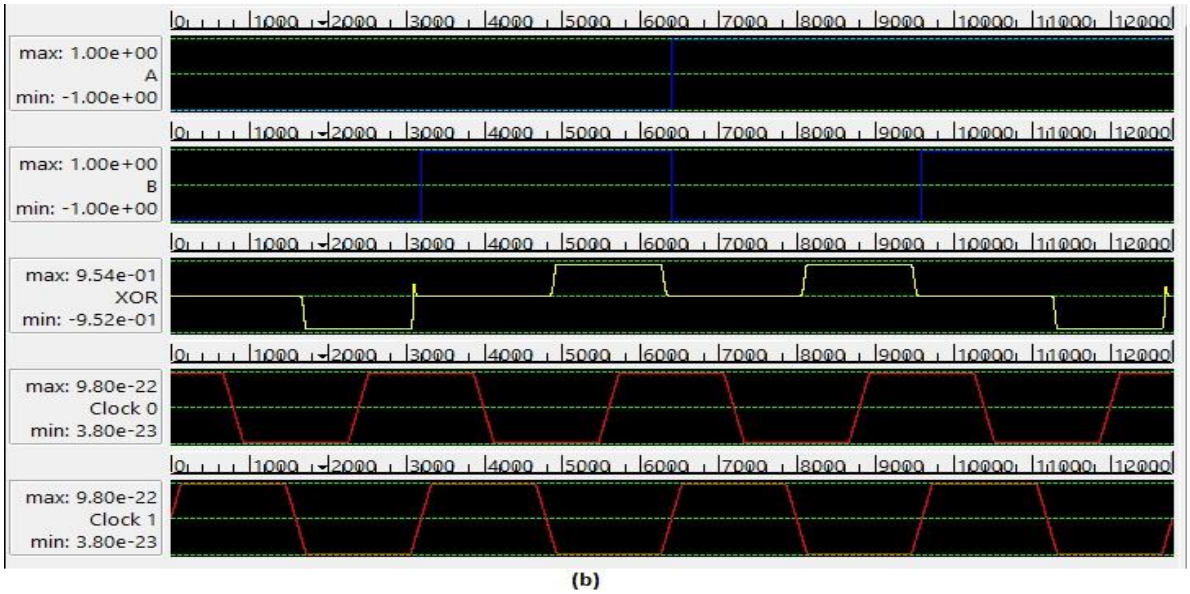


Figure 8: (a) proposed QCA XOR design layout (b) Simulation results of proposed XOR design.

Parameters	XOR as in paper[[19]]			XOR as in paper[[20]]							Our proposed XOR
	...a...	b	c	a	b	c	d	e	f	g	
No. of cells	41	55	62	34	54	52	52	48	54	42	32
No. of majority gate	3	4	4	4	3	4	4	3	3	3	3
Dealy	4	4	4	4	4	4	4	3	4	3	2
Total area(nm^2)	1980	3366	3168	1440	2880	2808	2808	1980	2700	1620	1620
Area use(nm^2)	738	990	1116	612	972	936	936	864	972	756	576
% of used area	37.3	29.4	35.2	42.5	33.7	33.3	33.3	43.6	33.0	46.6	35.5

Table 1: Comparative Study of our proposed design with some most recent design

V. CONCLUSION

In this article we proposed efficient structures of Quantum-dot Cellular based XOR gate with reduced number of QCA cells, area and delay in signal propagation from input to output. The proposed design has been implemented and simulated using bi-stable Approximation simulation of QCA Designer version2.0.3. By this approach we can go for designing complex sequential and combinational circuits. This methodology is very simple to implement. This QCA circuit is the future nanotechnology and different classical models can be replaced by this QCA logic circuit and this will become much more efficient and less complex than its other counterpart.

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