Design of IEEE 754 Format 32 Bit Complex Floating Point Vedic Multiplier - A Review

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Abstract— the floating point multiplier is extremely important part of many digital signal processing applications. This paper presents the design for a multiplier which computes complex and floating point numbers of 32 bits using Vedic multiplication technique. The Urdhva Tiryagbhyam sutra from Vedic mathematics is used for multiplication. The implementation of the Vedic mathematics and their application to the multiplier ensure substantial reduction of propagation delay which in turn improves speed. The design is capable of handling underflow and overflow cases. The inputs to the multiplier are provided in IEEE 754, 32 bit binary format.

IndexTerms— **Vedic mathematics, Urdhva Tiryagbhyam sutra, Floating point.**

I. INTRODUCTION

Multipliers are of utmost importance to many high performance systems like digital signal processing, image processing, microprocessor and multimedia [1] [2]. A system's performance is generally decided by the performance of the multiplier since multiplier is usually the slowest or fundamental element in the system. Hence high processing performance, low area and power consumption are the most important requirement of any system [3]. In the last few decades, several architectures for multiplier have been proposed and designed. In these algorithms, the multiplication process involves many intermediate stages before arriving at the final answer [4]. Because of the intermediate stages, which include several comparisons, addition and subtraction operation the speed of the multiplier reduces considerably [5]. Since speed of the multiplier is our main focus such architectures are not suitable for high performance systems. In order to increase the speed of the multiplier, an approach based on ancient Vedic mathematics can be implemented for multiplication.

IEEE 754 format:

IEEE(the Institute of Electrical and Electronics Engineers) has established a technical standard for representing floating point in 1985.An IEEE 754 format contains a set of representation of numerical values and symbols. An IEEE 754 format can be used to express very large or very small numbers precisely using scientific notation in binary form [6]. It includes arithmetic formats, interchange formats, rounding rules, operations and exception handling. The Binary Floating point numbers are specified in single and double formats .Single-precision floating-point format has the 32-bit explicitly shown and double-precision floating point format has the 64-bit explicitly shown. The IEEE 754 standard specifies a Single precision as having 3 areas that is 1 bit for showing the sign bit, 8 bit for showing the exponent part and 24 bit for showing mantissa , in which 23 bit are explicitly stored and 1 bit is hidden[7].

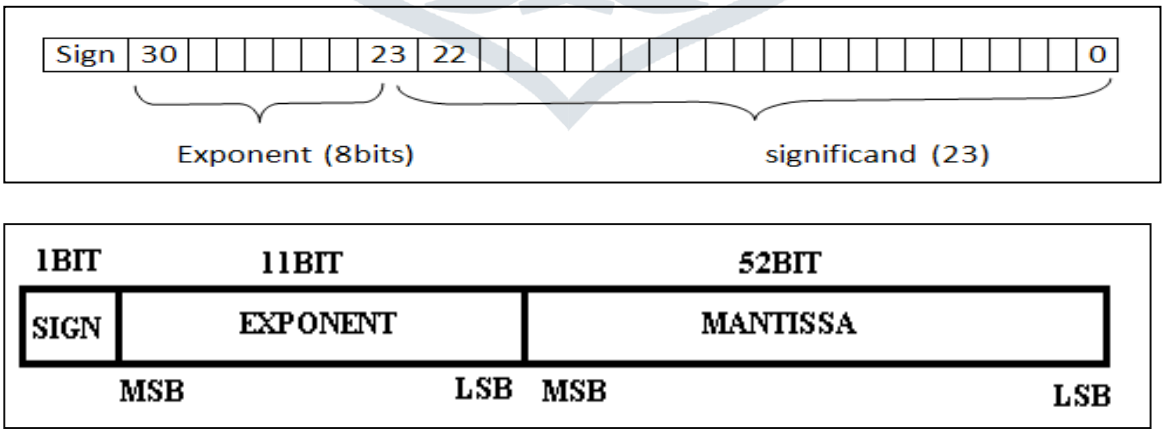

Fig.1 IEEE Format for single precision and double precision

The word 'Veda' means knowledge or wisdom in Sanskrit. Sri Bharathi Krishna Tirthaji (1884-1960) a pioneer of Sanskrit, mathematics, history and philosophy has developed 16 sutras from the ancient Vedic scripts in Sanskrit. Among the sixteen sutras, the Urdhva tiryagbhyam sutra can be used for multiplication of any numbers. In Sanskrit urdhva means 'vertically' and

tiryagbhyam means 'crosswise'. [8]. Working of this sutra can be explained by considering an example. Consider three bit numbers let A=a2a1a0 and B=b2b1b0[8].

1. The least significant bit of A is multiplied with the least significant bit of B giving s0=a0b0;
2. Then a0 is multiplied with b1, and b0 is multiplied with a1 and the result are added together as: c1s1=a1b0+a0b1; Here c1 is carry and s1 is sum.
3. Next step is to add c1 with the multiplication results of a0 with b2, a1 with b1 and a2 with b0. c2s2=c1+a2b0+a1b1 + a0b2;
4. Next step is to add c3 with the multiplication results of a1with b2 and a2 with b1.c3s3=c2+a1b2+a2b1;
5. Similarly the last step: c4s4=c3+a2b2;
6. The last stage of multiplication of A and B produces c4s4s3s2s1s0

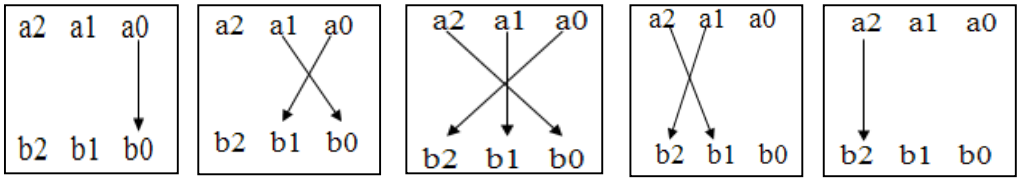

Fig. 2 The Urdhva Tiyagbhyam Multiplication method

II. Related Work

Sandesh, etal [8] proposed a high speed signed multiplier which uses Vedic multiplication technique published in Signal Processing, Computing and Control (ISPCC), 2012 IEEE International Conference on 15-17 March 2012. The method is for multiplier having fixed point numbers as inputs. They simulated their design and compared their result with simple Booth multiplier and Xilinx parallel multiplier intellectual property. The proposed work is 2.61 times faster than the normal Booth multiplier and 1.84 times faster than Xilinx parallel multiplier intellectual property according to their conclusion. In this multiplier the fraction number is first converted in the range of the desired Q m*n format by multiplying it with 2^n. The resultant value is truncated or rounded off to the nearest integer. Therefore it involves precision loss.

Jiun-Ping Wang et. al [9] proposed a design of high accuracy fixed-width modified Booth multiplier, published in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 19, No. 1, January 2011. In the paper the author has modified the partial product matrix of fixed-width multiplier to small degree and accordingly an effective error compensation function has been obtained. The author claims that compensation function makes the error distribution be more symmetric to and centralized in the error equal to zero, leading the fixed-width modified Booth multiplier to tiny mean and mean-square errors. They also designed simplified sorting network to implement compensation function. They reached into a conclusion by implementing their design and comparing their result with previous circuits based on fixed-width Booth multiplier, the proposed multiplier offers 12.3% and 6.3% reduction in mean –square error than others for 16-bit and 8 –bit respectively. Since the compensation network is simple it does not considerably increase the area. In whole the proposed architecture [9] are suitable for lossy application to minimize area and power consumption with good output quality. Because the proposed architectures is for lossy application the multiplier aims for precision. This multiplier can be further optimized for improving speed and lowering area.

Mustafa et. al[10] put forth an general approach for designing array and tree multipliers with overflow detection published in IEEE Transactions on Computers, Vol. 55, No. 8, August 2006. A single multiplier has been designed to perform either unsigned or 2's complement multiplication with overflow detection. The overflow detection circuit works in parallel to the multiplier hence reducing area and thereby reducing power consumption. Mustafa et. al [10] implemented their approach and compared with previous type of multiplier for area and delay, the result shows proposed design [10] has less area and delay compared to previous types. The limitation of this approach is that it can only be applied to simplified multiplier that produces (n+1) product bits.

Prabir et al [11] presented a design of a high speed complex multiplier that works on Vedic mathematic multiplication formula published in Proceeding of the 2011 IEEE Students' Technology Symposium14-16 January, 2011, IIT Kharagpur. In this design due to Vedic formulae, the partial products and sums are produced in single step which reduces the carry propagation from LSB to MSB. This minimizes the propagation delay and to an extent area also. They compared their architecture with mostly used complex multiplier which uses parallel adder based implementation and algebraic transformation based implementation. The comparison shows that the proposed architecture [11] provides 20% and 19% improvement in terms of propagation delay and power consumption respectively, in comparison with parallel adder based implementation. Whereas, with reference to the algebraic transformation based implementation, 33% and 46% improvement in terms of delay and power respectively was found. This multiplier uses 'Nikhilam Navatascaramam' sutra (Vedic formula) which has few disadvantage such as it can only be used to numbers whose unit- place sums to base of 10. The architecture has many adder and subtractor stage after multiplication stage.

Sushma et al [12] presents a design for high speed multiplication using Vedic mathematics approach published in Automation, Computing, Communication, Control and Compressed Sensing (iMac4s), 2013 International Multi-Conference on 22-23 March 2013. They also proposed an approach that utilizes 4:2 compressors and 7:2 compressors for addition. Compressors are capable of adding more three bits at time with less gate count. The implemented their design and compared their output with other multipliers. The result shows that in term of speed the proposed architecture [12] 1.12 times faster than other multiplier based on Vedic mathematics technique. It was also compared with Booth and Modified Booth multiplier and the proposed design was 2.112 times and 1.509 times faster respectively. The result further shows that in terms of area also it is efficient in comparison with others. This multiplier is only tested for simple numbers. Hence this technique can further be modified to be implementing other types of number.

III. CONCLUSION

We can conclude Vedic mathematic technique has many advantages compared to normal multiplier. Due to coherence and symmetry in the Vedic algorithm it can have a regular silicon layout. So the main objective is to design a multiplier architecture which will compute complex floating point numbers, such that architecture should be able to minimize delay. Since reducing the delay increases the speed. Precision and accuracy also play significant role. So, complex floating point multiplier will have flag rising circuits for undesired conditions.

IV. REFERENCE

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