SIMULATION AND IMPLEMENTATION OF HYBRID MULTILEVEL INVERTER

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Abstract-The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. Inverters can be two level or multilevel inverter. Multilevel inverter (MLI) as compared to two level inverters have advantages like minimum harmonic distortion, reduced EMI/RFI generation and can operate on several voltage levels. Now a days, asymmetrical MLI have received increasing attention because it is possible to synthesize voltage waveforms with reduced harmonic content, even using a few series-connected cells. This advantage is achieved by using distinct voltage levels in different cells, which can create more levels in the output voltage and minimize its total harmonic distortion (THD) without increasing the number of switching devices and isolated sources switching devices and isolated sources. As the number of voltage levels on the DC side increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion.

***Keywords*— Hybrid Multilevel Inverter, Total Harmonic Distortion**

I. INTRODUCTION

In the field of Power electronics the levels of output voltage have been changed using different Inverter topologies. Each inverter topology has its own limitations regarding different aspects like number of components used, stress on semiconductor switches and inverter efficiency. Some of these inverters have found place in industry for a variety of applications. Multilevel inverters (MLIs) have very important development for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum. The application of MLIs has been extended to the medium power range due the advantages of reduced distortion, dv/dt stress and common mode voltage.

II. Proposed HMLI Topology

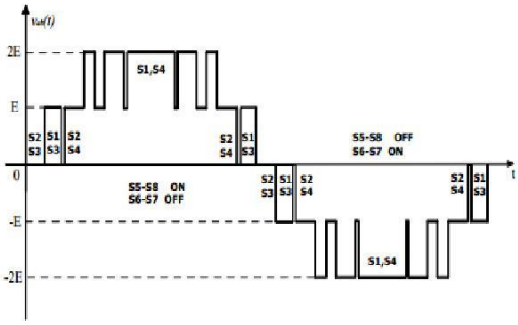
- Symmetrical Hybrid Multilevel inverter (SHMLI)
- Asymmetrical Hybrid Multilevel inverter (ASHMLI)

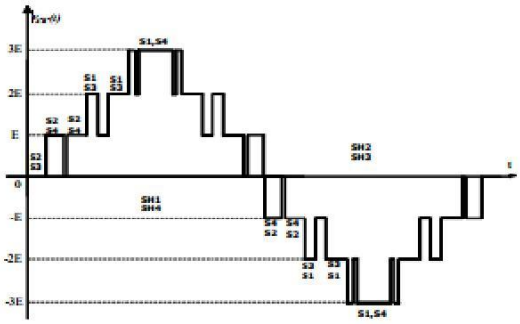
In symmetrical HMLI all H-bridge cells are fed by equal voltage source and hence all the arm cells produce similar output voltage levels while in asymmetrical HMLI all H-bridge cells are fed by un-equal voltage source and hence all the arm cells produce different output voltage levels.

Single Phase Topology:-

The SHMLI and ASHMLI topology in single-phase configuration is shown in **Fig.1 (a) and 2(a)** respectively**.** It consist of total 8 number of semiconductor switches (S1–S8) out of which middle arm switches (S1-S4) operates at high frequency(IGBT or MOSFET) while other four switches (S5–S8) form the normal H-Bridge operates at low frequency(IGCT or GTO). In **Fig. 1(b)** and **2(b)** single-phase SHMLI and ASHMLI generates 5-level output voltage. **i.e. 2E, E, 0, E, 2E** and 7-level output voltage **i.e. -3E, -2E, E, 0, E, 2E,** depending up on the modulation technique used.

The control strategy for the switches to get the desired output voltage level as shown in Fig3.2 (a) and (b) respectively [1,2]. The switch S1-S4 produces unipolar waveform and switches S5-S8 produces alternate output





voltage waveform. The modulation techniques used for driving the switches is based on the multicarrier PWM technique known as (1) phase-shifted disposition(PSD) (2) phase-disposition (PD) for the 5-level and 7-level output voltage respectively.

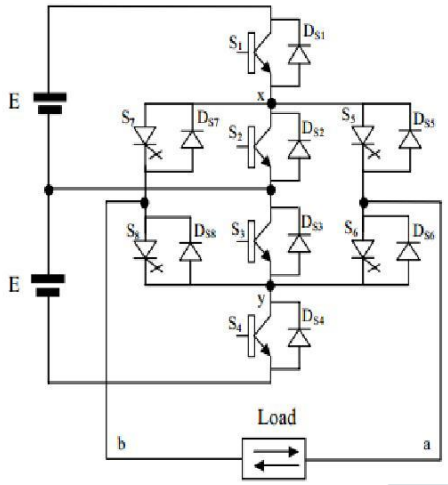


Fig.1 (a) Single-phase SHMLI

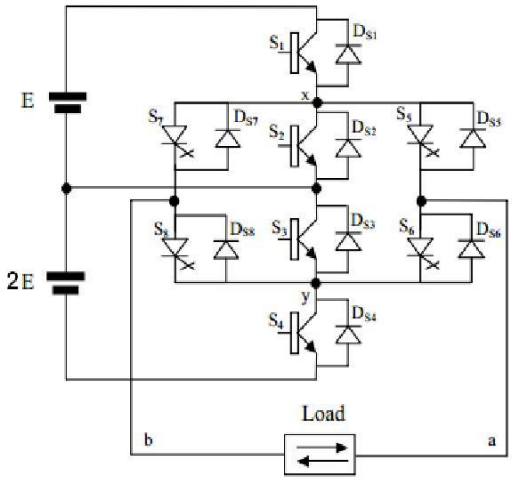


Fig. 2 (a) Single-phase ASHMLI

➢ Three Phase HMLI Topology

If three single phase outputs are connected in such that, they feed a three-phase load in star connection, then the outcome would be a three-phase hybrid multilevel inverter. The ASHMLI topology in three-phase configuration is shown in Fig. 3

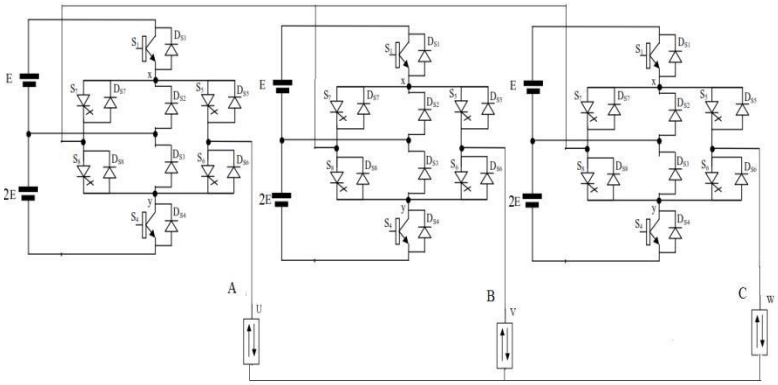


Fig. 3 Three phase ASHMLI

III. Modulation Techniques:

➢ **Phase Disposition (PD) Modulation in HMLI:**

Here, the output signal is generated through the comparison of a modulating signal Vm with three triangular carrier signals, all three carrier signals are in phase but displaced vertically with a value equal to its maximum value.

Control circuits used for the generation of pulses of command of the switches with modulating and carrier signal are shown in **Fig. 4(a)** and **4(b)** respectively.

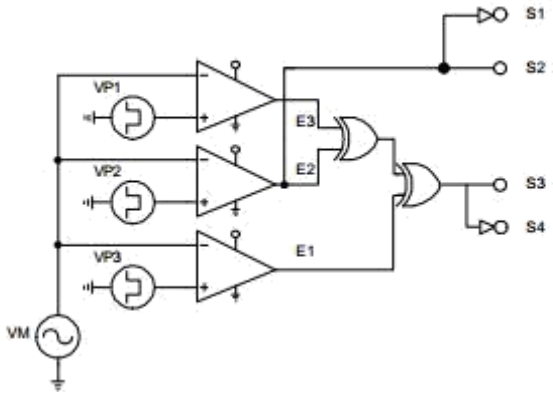


Fig. 4(a) Control circuit for the switches in single-phase asymmetrical HMLI

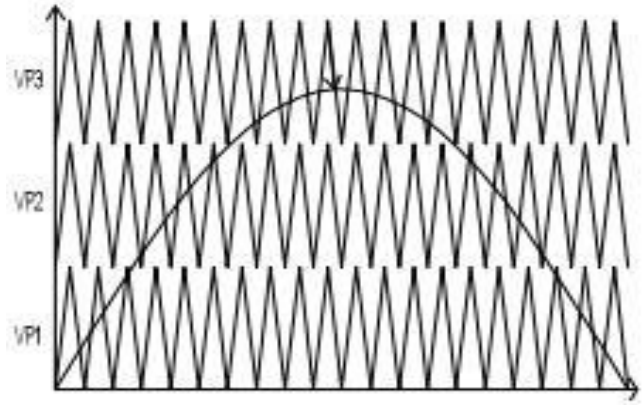


Fig. 4(b) Modulating and Carrier signal

IV. Simulation Results.

(Single phase inverter topology)

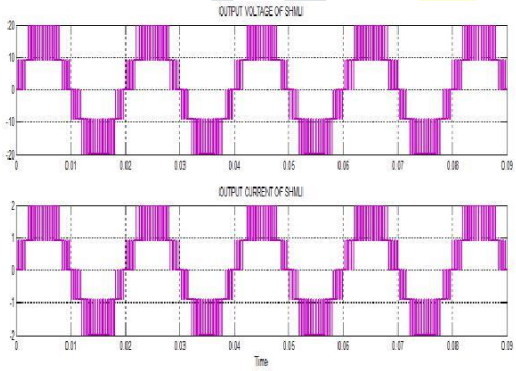


Fig: 5(a) Output voltage and current of single phase SHMLI (R load)

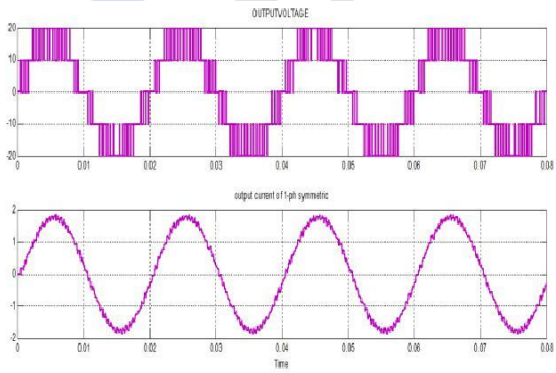


Fig.:5(b) Output voltage and current of single phase SHMLI (RL load)

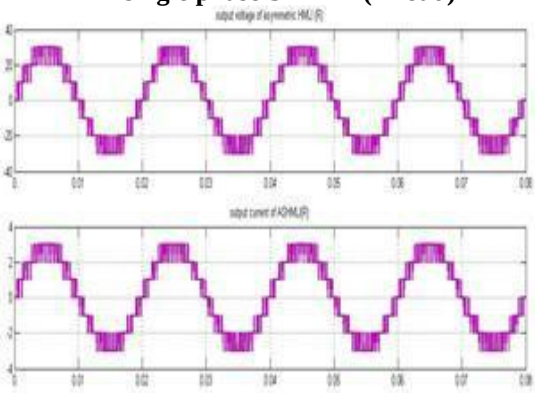


Fig: 5(c) Output voltage and current of single phase ASHMLI (R load)

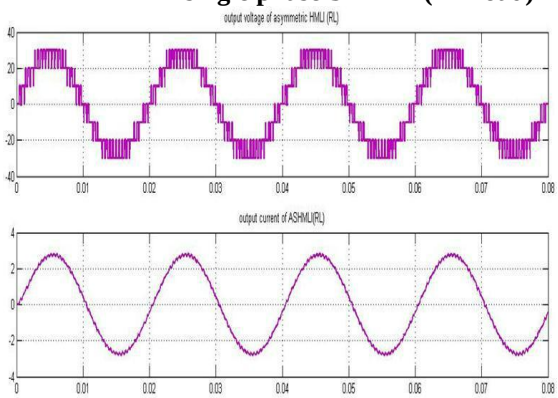


Fig: 5(d) Output voltage and current of single phase ASHMLI(R-L load)

V. Simulation Results.

(Three phase inverter topology)

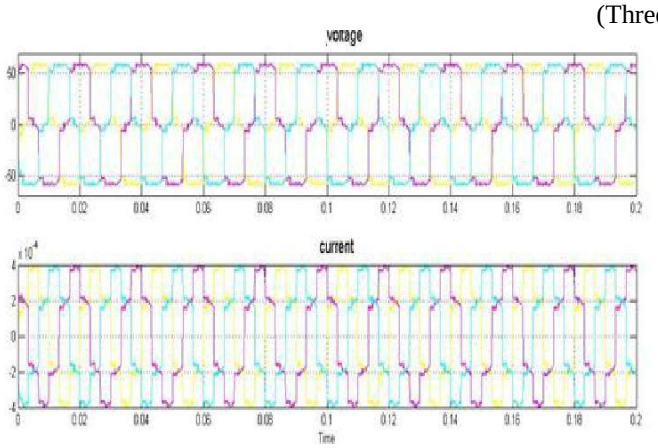


Fig: 6(a) O/p voltage/current of three phase ASHMLI(R)

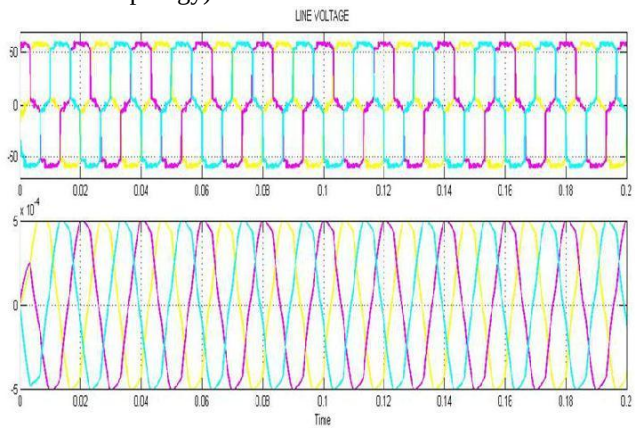


Fig: 6(b) O/p voltage/current of three phase ASHMLI (RL)

VI. THD ANALYSIS

Single phase HMLI

Topology	Quantity/load	R	R-L
Symmetric	Voltage	32.52%	32.53%
	Current	32.52%	10.85%
Asymmetric	Voltage	21.35%	21.36%
	Current	21.35%	2.66%

Three phase AHMLI

Quantity/load	R	R-L	R-L-E
Voltage	18.88%	24.90%	27.26%
Current	4.50%	5.20%	9.69%

VII. Experimental Results

To validate the operation of Hybrid Multilevel Inverter, a prototype experimental setup of single phase multilevel inverter is built. Specifications: 2E=24 volts, E=12 volts, operating at 1500 Hz switching frequency and fundamental frequency of 50 Hz. The switches used as a MOSFET are IRF840.The modulation strategy used is based on PD (Phase Disposition) and implemented using TLP250 for vertical switches. The output voltage waveforms without PWM and with PWM technique are as shown in fig. 7(a) and 7(b) respectively.

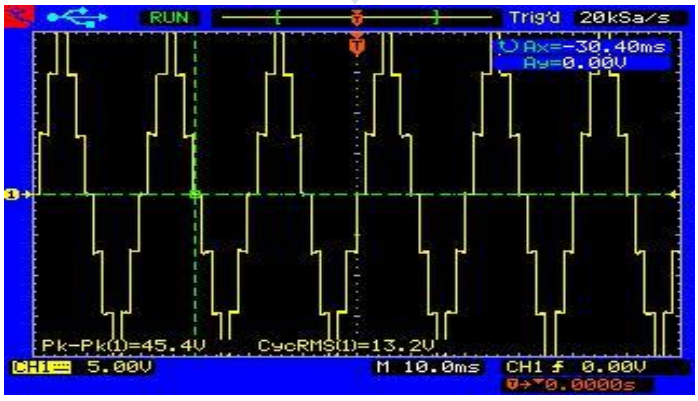


Fig. 7(a) and 7(b): Output voltage across the load without PWM & with PWM respectively.

VIII. Conclusion

This paper presented the circuits on SHMLI as well as ASHMLI for a single phase as well as for three phase for various kind of loads and its results. The vertical cell uses high frequency switches and low frequency switches are used for H-Bridge. Total no of output voltage levels are generated by vertical cell and it depends upon the no of sources used.

The advantage of this topology over symmetric is that it generates greater amount of output levels for the same no of switches, but the disadvantage is greater efforts of voltage to synchronize with a high frequency switches.

IX. Acknowledgment

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