The High performance Adder Circuits by Multiplexers

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Abstract: *Low power circuits increased with the use of large number of portable devices like cell phones, calculators, miniature computers etc. long battery life is required for all the devices which can be achieved by reducing power consumption of individual circuits. First method to reduce the power consumption is by operating the devices at low current and low voltage i.e. called as sub-threshold operation and the region of operation is called sub-threshold region. In this region, leakage current is used as operating current and power consumption is reduced significantly. This paper mainly focuses on the operation of various High performance Multiplexer based on1-bit Adder circuits [1] in sub-threshold region. The reduction in average power when compared to their super-threshold operation is analyzed. The variation of performance parameters and limitation of frequency of operation with variation in supply voltage are investigated. By varying the supply voltage below the threshold voltage, power can be reduced considerably. All the investigations in the paper are carried out using H-spice simulation tool. The circuits used are of 65nm process technology.*

Keywords: *Power dissipation, Propagation delay, power delay product, Sub-threshold.*

(1) Introduction

Designing of Demanded devices becomes very difficult because of change in semiconductor scaling trends. Increase in the growth of higher density devices which are resulted in power dissipation per chip to increase significantly due to shrinking of transistor sizes and hence we go for Smaller MOSFETs. If the Transistor is smaller we can pack more and more devices in a given chip area and with more functionality in the same area. The unit cost per integrated circuits is mainly depends on the number of chips that can be produced per wafer. Hence, reducing the price per chip more chips per wafer are built in smaller ICs. Doubling of transistor density was first observed by Gordon Moore in 1965 and is commonly referred to as Moore's law .In fact, over the past 30 years the number of transistors per chip has been doubled every 2-3 years by introducing of new technology. For example, the number of MOSFETs in a microprocessor fabricated in a 45 nm technology can well be twice as many as in a 65 nm chip.

An integrated circuit creates problems of substantial localized heat generation that can impair circuit operation due to ever-increasing density of MOSFETs. At high temperatures Circuits operate more slowly and decreases reliability and shorter lifetimes. To overcome this, Heat sinks and other cooling methods are used for integrated circuits and microprocessors. The power dissipation problem is major role in industry design. Without Significant low power research efforts we cannot reduce the Power dissipation. The methods used for low-power design are pipelining, parallelism, voltage scaling and switching activity reduction. These methods are not sufficient in many applications such as portable computing gadgets, medical electronics, where ultra low-power consumption with medium frequency of operation (MHz) is the primary requirement. The new method of sub-threshold leakage current has gained a wide interest in recent years to achieve ultra low-power consumptions in portable computing devices. The design consideration at various levels of abstraction have been extensively studied for both logic and memory circuits. This paper mainly focuses on achieving low power consumption by operating various circuits in the sub-threshold region [2]. The circuits considered are different 1-bit adder circuits which are compared [3] based on the performance metrics.

1.0 1-Bit Adder Sub-threshold Circuits using 65nm Process Technology

1.1 Introduction:

The most critical components of a processor that determines its throughput of 1-bit adder cell , as it is used in the ALU, the address generation and floating point unit for in case of cache or memory access. Therefore, it is inherent that modifications made to the full adder cell affect the system as a whole. In the paper, various 1-bit adders are implemented in the sub-threshold region [4] and their performance is analyzed.

1.2 The High Performance Adder Multiplexer (HPAM)

With the explosive growth in portable personal communication systems (PCS's), laptops and the evolution of the shrinking technology and flexible circuits, the research efforts to find high-performance digital systems[5] has been intensified. In the paper, four multiplexed based adders which give smaller delays (and thus higher performance) than the conventional adder and Symmetric Adder even in the sub-threshold region are implemented and the results are verified. The High performance Multiplexer based adder uses the pass-gate 2:1 multiplexer as shown in the Fig1. [6].

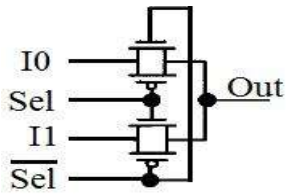

Fig 1 CMOS MUX Pass-Gate.

The usage of CMOS transmission gate in the multiplexer will improve the speed and without any degradation in the output voltage level.

1.2.1 High Performance Adder1 Multiplexer (HPA1M)

The first architecture, shown in Fig.2(a), uses 6 multiplexer gates to accomplish the full adder function.

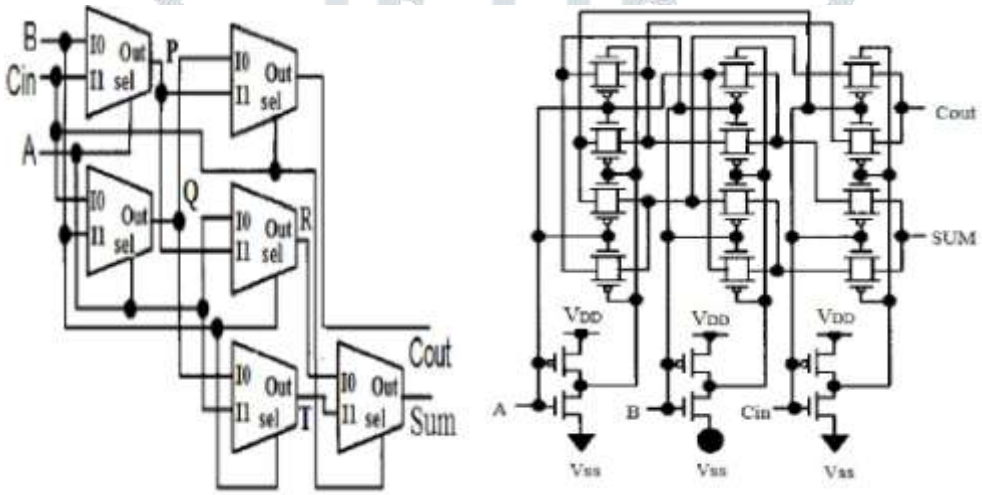

Fig 2.(a) High Performance Adder1 and Transistor level circuit diagram (**HPA1M**)

The HPA1M has all its internal nodes connected to fresh input signals (A, B and C_{in}). Thus, the short circuit current and switching activity of the nodes will be kept to a minimum. The SUM signal will have a critical delay equal to three times the critical delay of the used multiplexer gate, and equal to two in case of the C_{out} signal[7,8,9]. The HPAM1 circuit implemented using the pass gate multiplexer has 30 Transistors (15 PMOS and 15 NMOS).

The HPA1M circuit has been simulated using H-SPICE software in the sub- threshold region with V_{DD}=0.2V at a frequency of 100KHz (pulse duration is 10µs) and the results are as shown in the Table 1

Table 1 Simulation results of HPA1M

Parameter	Value
Carry rise time (s)	4.17E-08
Carry fall time (s)	4.19E-08
Sum rise time (s)	5.60E-08
Sum fall time (s)	2.7983E-08
Average Power (W)	2.6209E-09
Carry Delay (s)	1.8657E-08
Sum Delay (s)	2.5268E-08
PDP (J)	6.6224E-17

The Simulation Waveforms in Fig 3(a) shows the outputs SUM and C_{out} for inputs A=00001111, B=00110011, C_{in}= 01010101. The inputs have a rise and fall times of 25ns. The outputs SUM=01101001 and C_{out} = 00010111 are found to be in accordance with corresponding output values in Table 1.

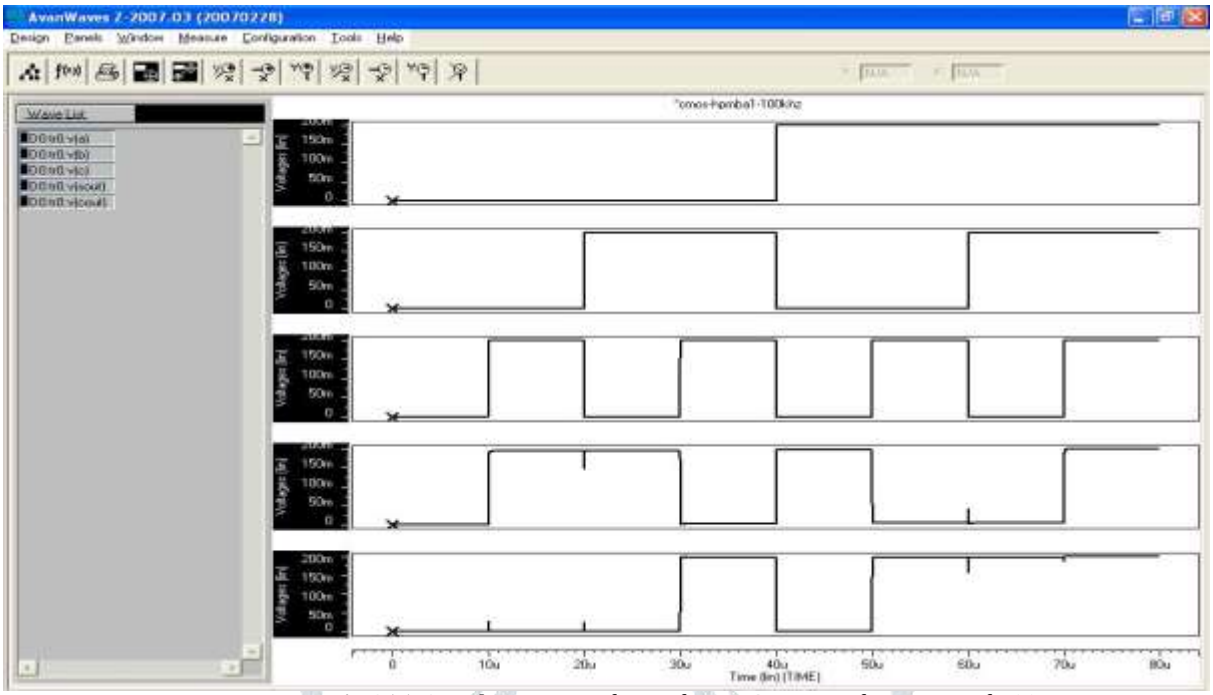

Fig 3(a) Simulation Waveforms for HPA1M at a frequency of 100KHz

The HPAM1 has been simulated under various frequencies in the range 10KHz (0.01MHz) to 10MHz. From the simulation results the rise time, fall time and delay are found to be constant while the average power increases with increase in frequency .The Simulation Waveforms of HPMBA1 at a frequency of 10MHz is as shown in the Fig 3(b) and it is observed that the output waveforms are distorted.

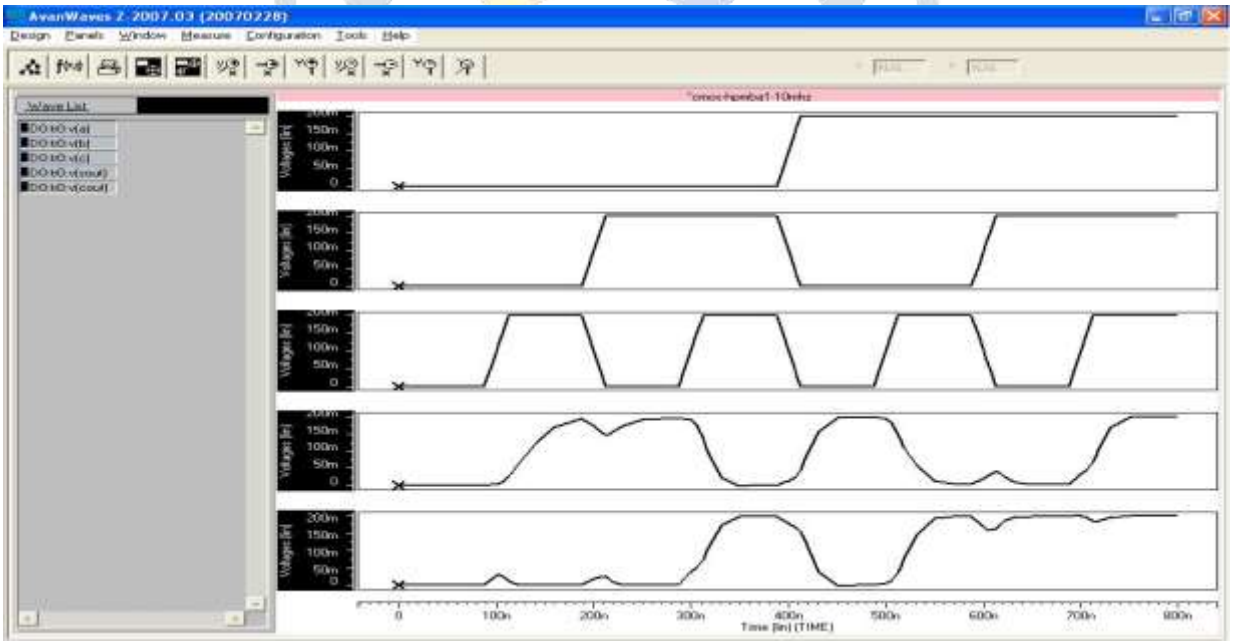

Fig 3(b) Simulation Waveforms for HPA1M at a frequency of 10MHz

1.2.2 High Performance Adder2 Multiplexer (HPA2M)

The HPA2M further improves SUM and C_{out} signal delay by adding five multiplexer gates and two inverters as shown in the Figure 3.16.

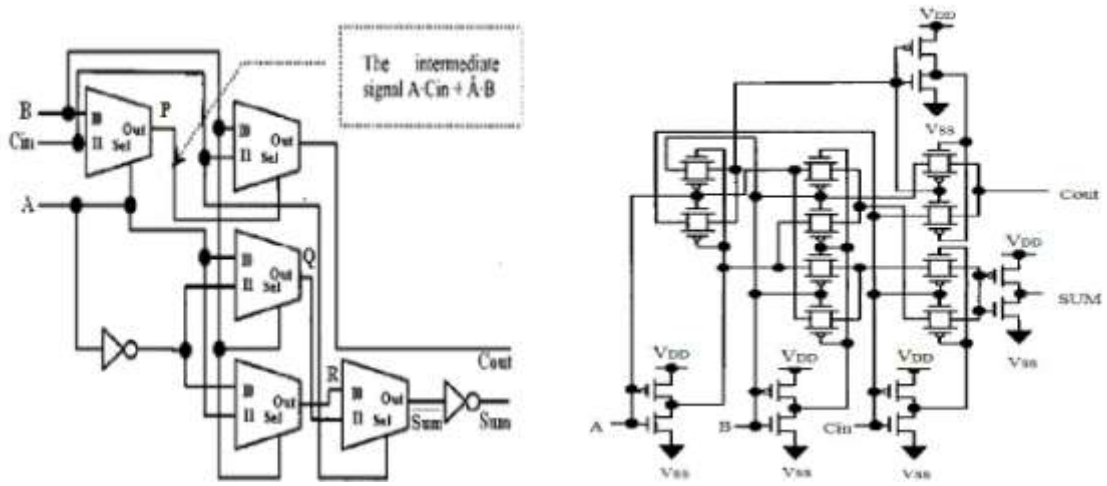

Fig 4 High Performance Multiplexer Based Adder2 (HPA2M) and Transistor level circuit diagram of HPA2M

The C_{out} signal of HPMBA2 is formed by using an immediately generated signal{(B ∧ A) ∨ (Cin ∧ A)}. Thus, the delay of C_{out} is equal to critical delay of one multiplexer gate plus the delay from sel port to out port. The SUM delay will be equal to two times the critical delay of the multiplexer and two times the critical delay of the inverter.

However, increase in the switching activity and the short circuit current at the nodes power consumption of HPA2M will be higher than that of HPA1M with the nodes supplied by the intermediately generated signals. Also, the presence of two inverters will add to the short circuit current of this architecture. The HPA2M circuit implemented using the pass gate multiplexer has 30 Transistors (15 PMOS and 15 NMOS). The HPA2M circuit and has been simulated using H-SPICE software in the sub-threshold region with V_{DD}=0.2V at a frequency of 100KHz (pulse duration is 10μs) and the results are as shown in the Table 2.

Table 2 Simulation results of HPA2M

Parameter	Value
Carry rise time (s)	2.8133E-08
Carry fall time (s)	3.1139E-08
Sum rise time (s)	1.9713E-08
Sum fall time (s)	2.5879E-08
Average Power (W)	3.6255E-09
Carry Delay (s)	1.2049E-08
Sum Delay (s)	2.3096E-08
PDP (J)	8.3665E-17

The Simulation Waveforms in Figure 3.18 shows the outputs SUM and C_{out} for inputs A=00001111, B=00110011, C_{in}= 01010101. The inputs have a rise and fall times of 25ns. The outputs SUM=01101001 and C_{out} = 00010111 are found with corresponding output values in Table 2.

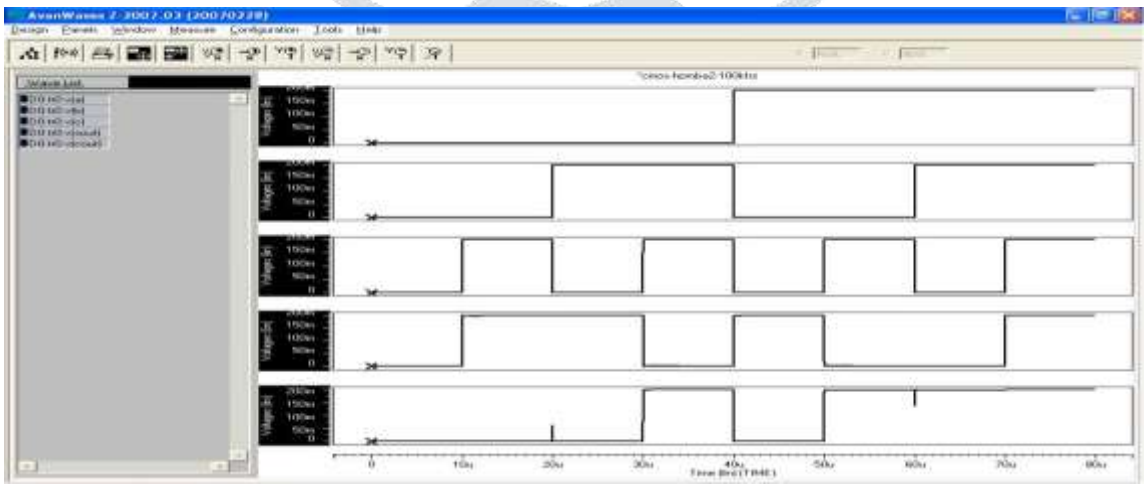

Fig 5 Simulation Waveforms for HPA2M at a frequency of 100KHz

The HPA2M has been simulated under various frequencies in the range 10KHz (0.01MHz) to 10MHz. The Simulation Waveforms of HPA2M at a frequency of 10MHz is as shown in the Fig6 and it is observed that the output waveforms are distorted.

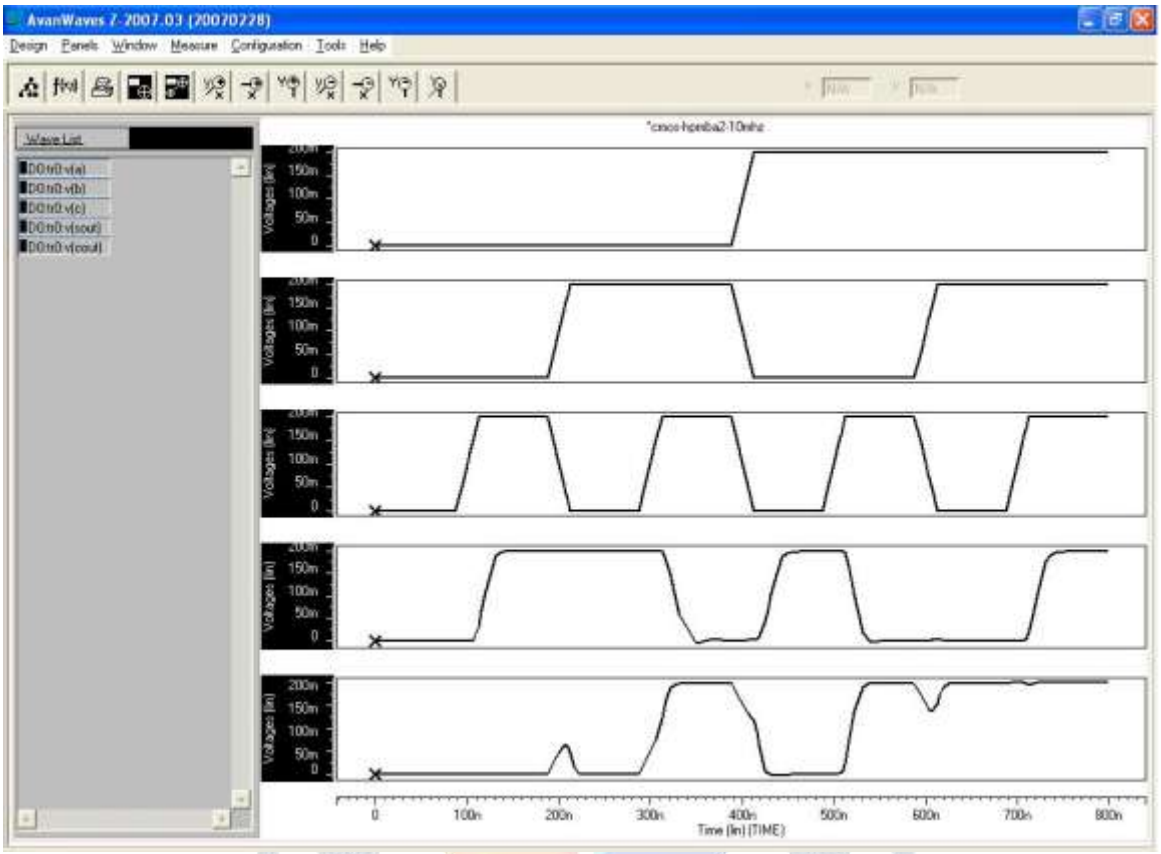

Fig 6 Simulation Waveforms for HPA2M at a frequency of 10MHz

1.2.3 High Performance Adder3 Multiplexer (HPA3M)

This architecture is an improved version of HPA3M. It has four multiplexer gates and two inverters as shown in Fig 7.

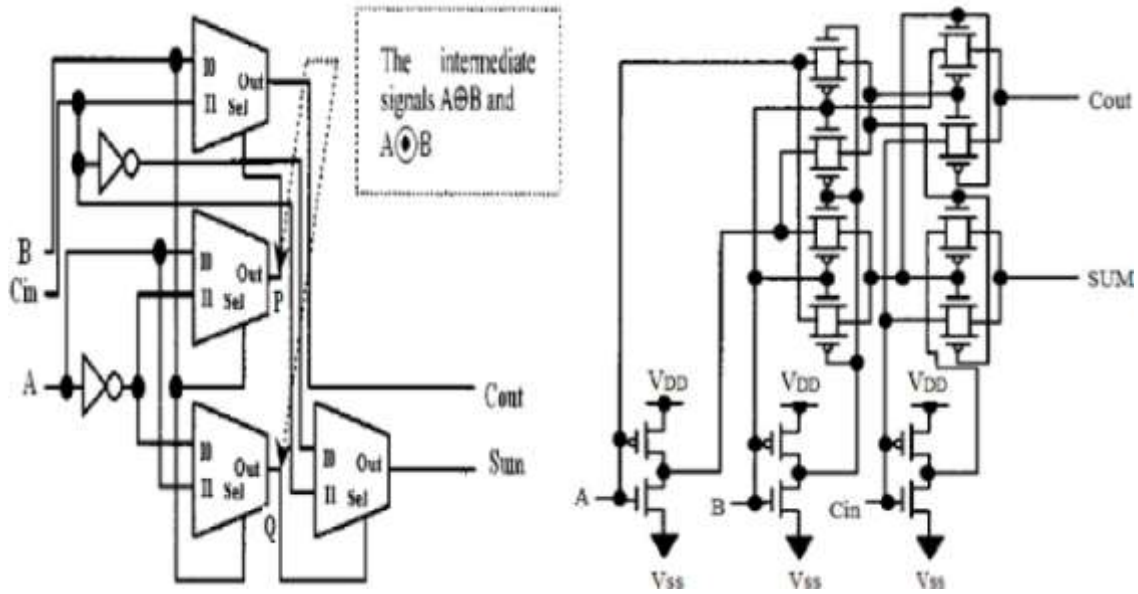

Fig 7 High Performance Multiplexer Based Adder3 (HPA3M) and Transistor level circuit diagram of HPA3M

The SUM delay is less than HPA2M as it is equal to the critical delay of one inverter and one multiplexer plus the delay from Sel port to Out port.The C_{out} delay will be higher as it is now equal to the sum of the critical delay of one multiplexer gate, the critical delay one inverter and the delay from Sel port to Out port. Due to lesser number of components the power consumption is less when compared to HPA2M. Comparing HPA1M with HPA3M, the latter will have better delay characteristics, but will retain will have higher power consumption due to the usage of intermediately generated signals to produce SUM and C_{out}.

The HPA3M circuit designed using the pass gate multiplexer has 22 Transistors (11 PMOS and 11 NMOS). The HPA3M circuit has been simulated using H-SPICE software in the sub threshold region with V_{DD}=0.2V at a frequency of 100KHz (pulse duration is 10µs) and the results are as shown in the Table 3.

Table 3 Simulation results of HPA3M

Parameter	Value
Carry rise time (s)	2.7567E-08
Carry fall time (s)	3.0141E-08
Sum rise time (s)	2.9476E-08
Sum fall time (s)	3.0918E-08
Average Power (W)	2.8168E-09
Carry Delay (s)	1.2815E-08
Sum Delay (s)	1.4648E-08
PDP (J)	4.1261E-17

The Simulation Waveforms in Figure 3.23 shows the outputs SUM and C_{out} for inputs A=00001111, B=00110011, C_{in}= 01010101. The inputs have a rise and fall times of 25ns. The outputs SUM=01101001 and C_{out} = 00010111 are found to be in accordance with corresponding output values in Table 3.

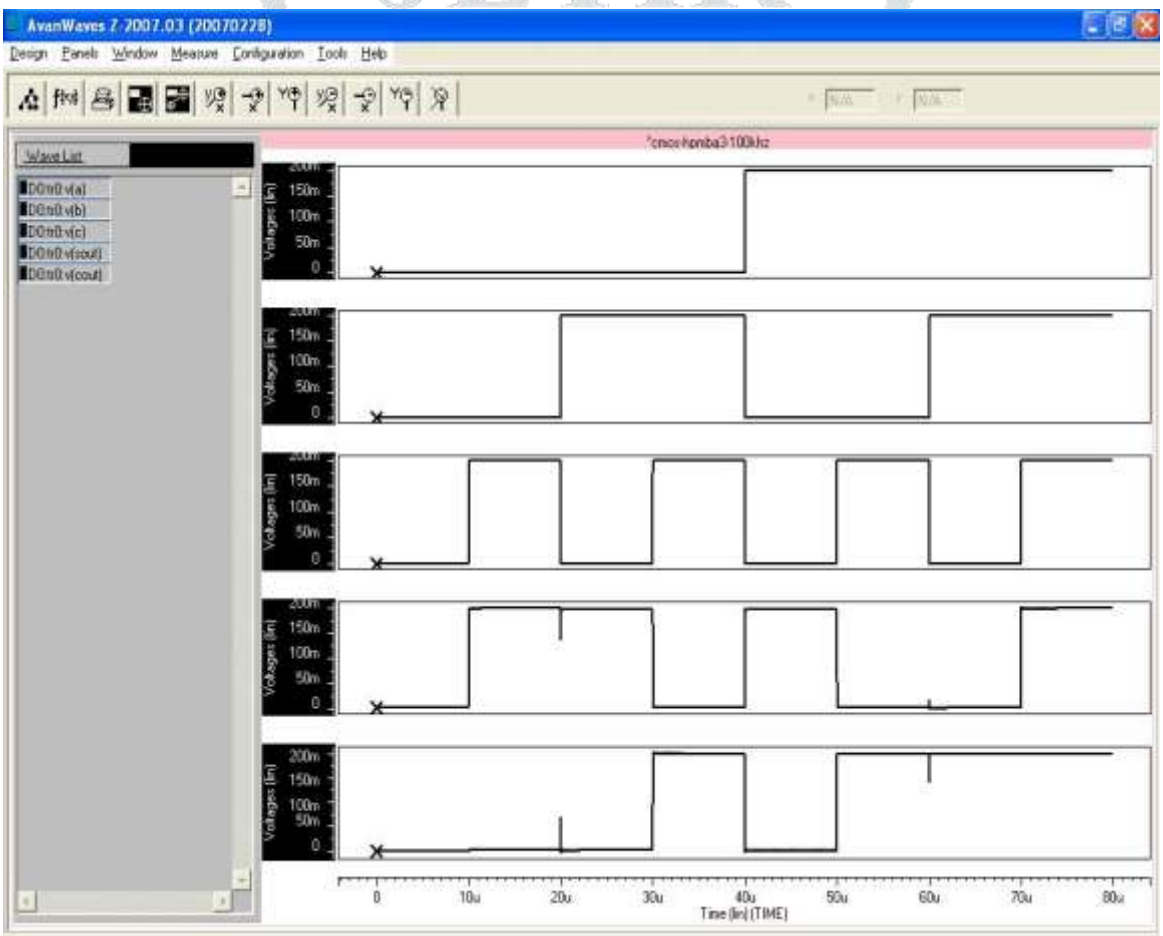

Fig 8 Simulation Waveforms for HPA3M at a frequency of 100KHz

The HPA3M has been simulated for various frequencies in the range 10KHz (0.01MHz) to 10MHz. The Simulation Waveforms of HPA3M at a frequency of 10MHz is as shown in the Fig 9 and it is observed that the output waveforms are distorted.

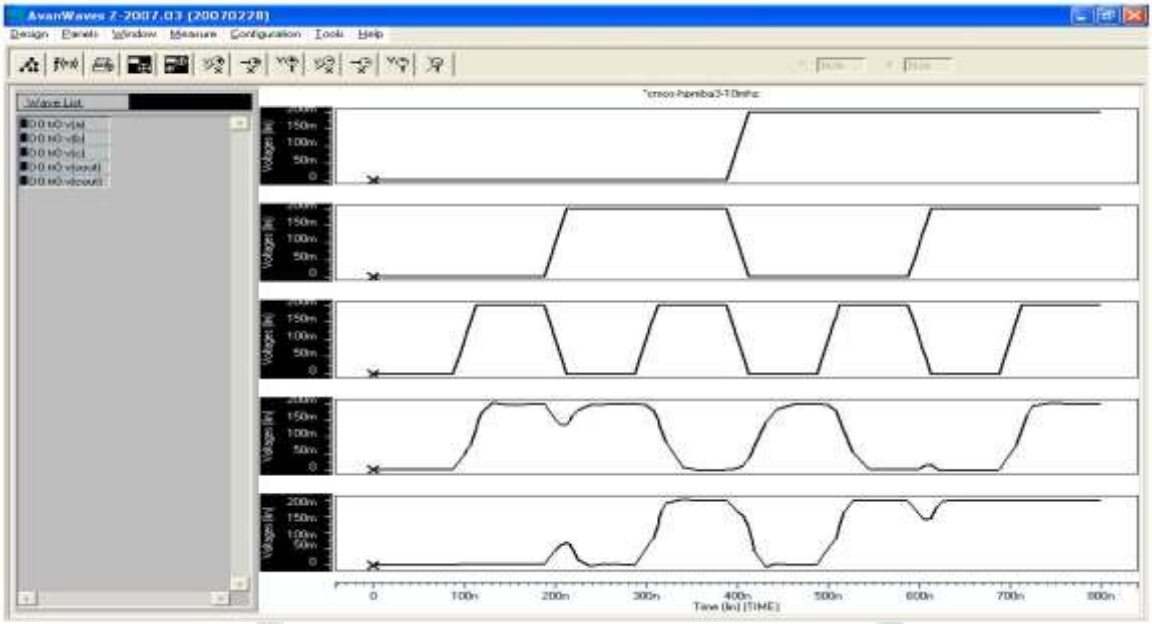

Fig 9 Simulation Waveforms for HPA3M at a frequency of 10MHz

1.2.4 High Performance Adder4 Multiplexer (HPA4M)

The HPMBA4 design is another modification of HPA2M. One inverter in the HPA2M is replaced with two inverter-like structures to decrease the short circuit current power consumption. The first structure is basically a CMOS inverter with its NMOS source connected to signal A instead of V_{DD} while the second one has its PMOS connected to A. Therefore the HPA4M uses one inverter, two inverter-like structures and five multiplexer gates as shown in the Fig 10.

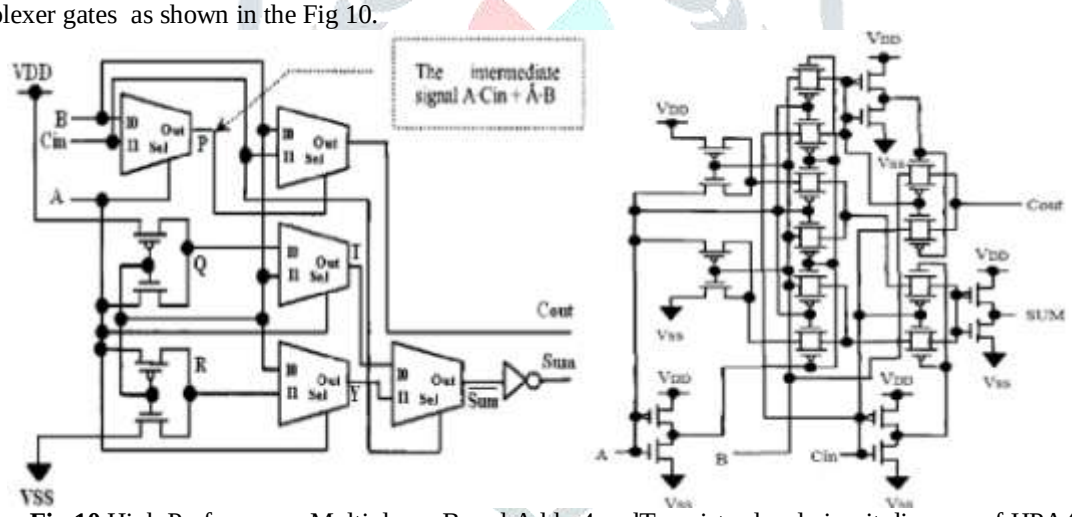

Fig 10 High Performance Multiplexer Based Adder4 andTransistor level circuit diagram of HPA4M

The C_{out} delay of HPA4M is similar to that of HPMBA2 but the sum delay is found to be lesser. The HPA4M circuit designed using the pass gate multiplexer (Fig 10) has 32 Transistors (16 PMOS and 16 NMOS). The HPA4M circuit and has been simulated using H-SPICE software in the sub threshold region with V_{DD}=0.2V at a frequency of 100KHz (pulse duration is 10µs) and the results are as shown in the Table 4.

Table 4 Simulation results of HPA4M

Parameter	Value
Carry rise time (s)	2.8130E-08
Carry fall time (s)	3.2742E-08
Sum rise time (s)	1.9634E-08
Sum fall time (s)	1.7544E-08
Average Power (W)	3.3622E-09
Carry Delay (s)	1.2454E-08
Sum Delay (s)	2.1312E-08
PDP (J)	7.1655E-17

The Simulation Waveforms in Fig 11 shows the outputs SUM and C_{out} for inputs A=00001111, B=00110011, C_{in}= 01010101. The inputs have a rise and fall times of 25ns. The outputs SUM=01101001 and C_{out} = 00010111 are found to be in accordance with corresponding output values in Table 4.

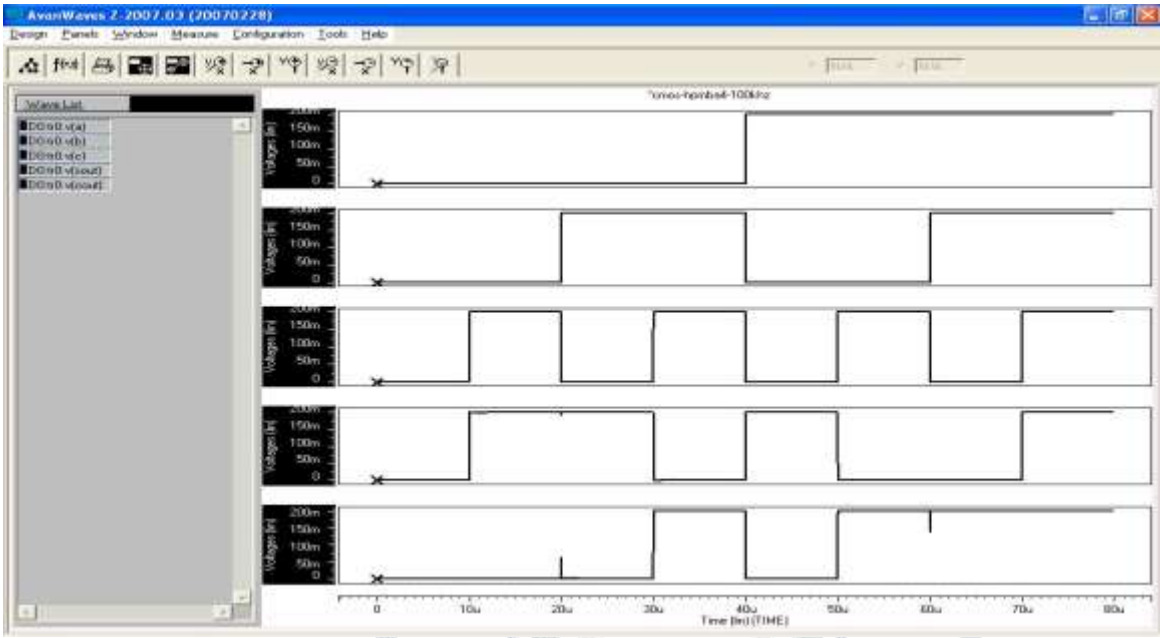

Fig 11 Simulation Waveforms for HPA4M at a frequency of 100KHz

The HPA4M has been simulated for various frequencies the range 10KHz (0.01MHz) to 10MHz. The Simulation Waveforms of HPA4M at a frequency of 10MHz is as shown in the Fig 12 and it is observed that the output waveforms are distorted.

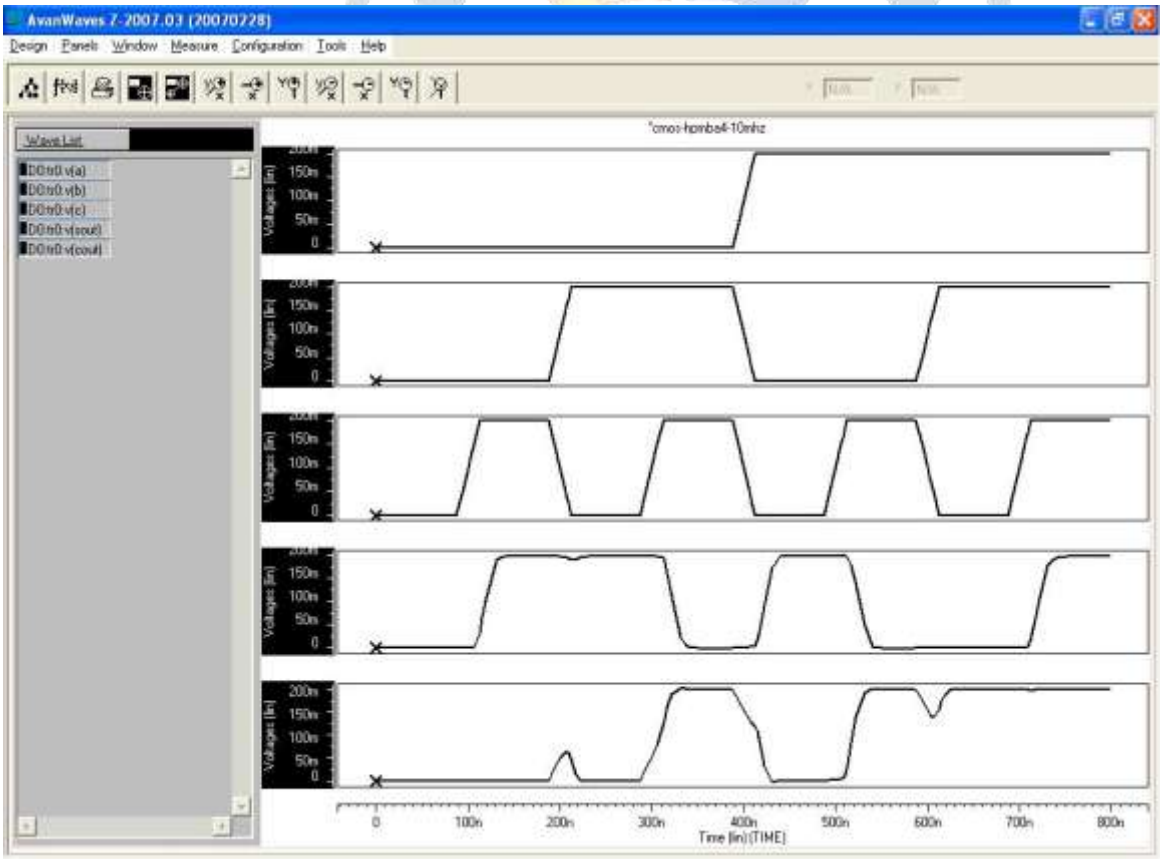

Fig 12 Simulation Waveforms for HPA4M at a frequency of 10MHz

The high performance multiplexer based adders can be used to improve performance in sub threshold region. However, we can further reduce the power of 1-bit adder cell in sub threshold region by using low power multiplexer based adders.

These employ very less number of transistors and hence achieve lower power dissipation. The lowest number of transistors with which a 1-bit adder can be constructed is 10.

II. Discussion Of Results

In the paper, 4 1-bit High Performance Multiplexer Based Adders are designed in sub-threshold region.
The silicon chip area occupied by the any circuit will be proportional to the number of transistors required for implementing it. The HPAMs have vey smaller delays compared to the general conventional 1-bit adder. The HPA1M, HPA2M, HPA3M and HPA4M have 10%, 17.4%, 47.66% and 23.79% speed increment (decrement in delay) over conventional adders. The HPAMs occupy less area when compared to the conventional 1-bit adder. The decrements in area, taking the conventional 1-bit adder as reference for HPA1M, HPA2M, HPA3M and HPA4M are 34.78%, 34.78%, 52.17%, and 30.43%, respectively.

2.1 Comparison of all 1-bit adders

All the 1-bit adder circuits have been simulated at 100KHz (duration of pulse is 10µs) frequency under both super threshold region (V_{DD}=0.8V) and sub threshold (V_{DD}=0.2V) and the results have been tabulated in the Table5.

Table 5 all 1-bit adders Simulation results

Parameter/Adder	Average power (W)		Propagation Delay (s)		Power Delay Product (J)	
	V_{DD}=0.2V	V_{DD}=0.8V	V_{DD}=0.2V	V_{DD}=0.8V	V_{DD}=0.2V	V_{DD}=0.8V
HP A1M	2.6209E-09	2.7824E-08	2.5268E-08	1.4864E-09	6.6224E-17	4.1359E-17
HP A2M	3.6255E-09	3.9876E-08	2.3096E-08	1.0072E-09	8.3665E-17	4.0165E-17
HP A3M	2.8168E-09	2.9283E-08	1.4648E-08	8.5658E-10	4.1261E-17	2.5084E-17
HP A4M	3.3622E-09	3.6885E-08	2.1312E-08	8.1058E-10	7.1655E-17	2.9898E-17

From Table 5, it can be observed that the adders when operated in sub-threshold region have lower power consumption (nearly 0.1 times of that in super- threshold region) and higher propagation delay (greater than ten times of that in super-threshold region).

III. Conclusions

From the various 1-bit adders that are implemented using 65nm technology, it is observed that HPA2M has the highest average power, the HPA3M has the least propagation delay and it does not produce any degradation in the output voltage levels.

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