Implementation of SPI Protocol Using Error Correcting Techniques

[1]KRITIKA BRAMTA , [2]BHAVNA PLAHA
[1]M.TECH (Student)   , [2] ASSISTANT PROFFESOR
[1] Department of Electronics and Communication Engineering
[1]Bahra University, Shimla-Hills, H.P, India

Abstract- SPI (Serial Peripheral Interface), introduced by Motorola is full duplex, synchronous serial communication with peripheral devices for transmission of data at extreme speed and over short distance. The main purpose of developing such technology was to replace parallel interfaces and to facilitate serial link communication between integrated circuits for low or medium data transfer speed with on-board peripheral. In order to enhance the performance of Serial Peripheral Interface protocol some error checking and correcting property must also be introduced in the protocol. An error checking and correcting approach is used for this purpose which can not only detect or correct the error in data transmission and reception, but also controls the overhead and can work with the present versions of the protocol.

Keywords: SPI Protocol ,error checking and detecting technique - CRC(Cyclic Redundancy Check)
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I. INTRODUCTION

SPI stands for Serial Peripheral Interface is employed for communication between integrated circuits for high/low/medium information transfer speed with on-board peripheral [1]. The SPI bus is a synchronous serial data link standard, named by Motorola that operates in full duplex mode[3]. SPI is a serial interface protocol with features like minimizing the number of pins, great transmission speed and uncomplicated to use. Serial Peripheral Interface protocol comprises of master-device and slave-device for transmitting the information as well as receiving the information. The communication method is initiated by the master-device solely. The chip chooses signal and clock signal which are generated by the master-device only[1]. The SPI bus is all-purpose standard for controlling any digital electronics that allows a clocked serial stream of bits.

II. SPI PROTOCOL

SPI (Serial Peripheral Interface) is service to provide economical board-level interfaces between different devices like microcontrollers, DACs, ADCs. The communication in SPI protocol takes place in terms of master/slave relationship, where the master initiates the data frame. When the master generates a clock and a slave device is selected, data may be transferred in either one or both directions at the same time. Although, where SPI is involved the data are always transferred in both directions simulatenously.
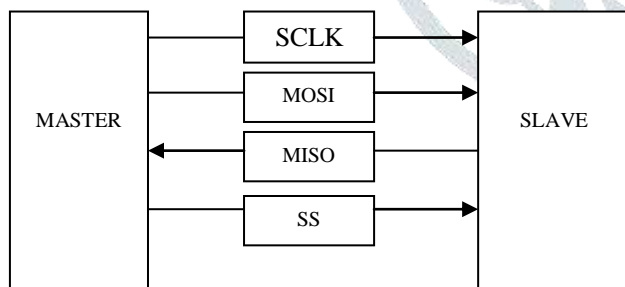

Fig1. Master/Slave block diagram of SPI protocol

The SPI bus interface consists four logic signals namely Serial Clock (SCLK), Master Output Slave In (MOSI), Master In Slave out (MISO) and Slave Select (SS) [3]. Figure 1. shows signals in a single-slave configuration. SCLK is generated by the master and input to the slave. MOSI transmit the data from master to slave. MISO transport the data from slave back to master. A slave device is selected when the master affirms its SS signal.

III. SPI DESIGN

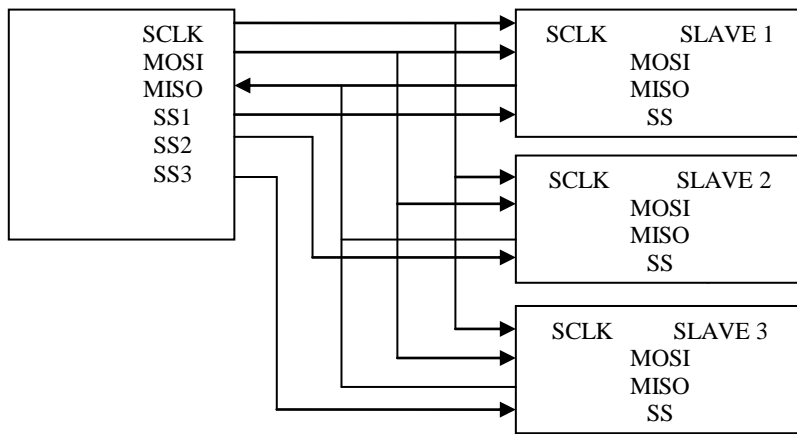The relationship between the master and multiple slaves can be illustrated by Fig 2

Fig 2 the master generates a separate slave select signal for each slave

Four signals are-

SS- A slave select signal (SS) for each slave, used to select the slave the master communicates with [4]

SCLK - This is often the serial clock signal. It's generated by the master

MOSI - The signal is generated by Master, recipient is that the Slave.

MISO -The signals area unit generated by Slaves, recipient is that the master.

IV. PROPOSED METHODOLOGY

In order to introduce error detection and correction capability to the SPI protocol, Cyclic Redundancy Check (CRC) is used. Since all the digital systems are error prone and error detection and correction is important whenever there is a non zero probability of error. CRC are used for detecting the corruption of digital content during its production, transmission, processing or storage [5]. CRC algorithms treat each bit stream as a binary polynomial and calculate the remainder from the division of the stream with corresponding to the remainder is transmitted together with the bit stream [5].

The proposed methodology takes 3 bits out of the total 8 bits of address or data bits. Basically the blocks of data which enter gets a short check value attached to it which is based on the remainder of polynomial division of their contents. Corrective action can be taken if presumed data is found with errors or corrupted if the check values are not matching. CRC uses some polynomial to detect and correct the errors. The generator polynomial used here is given by

$$g(x) = x^2 + 1 \qquad (1)$$

This equation can be implemented on the remaining bits of the address and data field and can be implemented by simply performing the ex-or operation.

V. SIMULATION AND RESULT

Figure 1 shows the components used in the SPI Master implementation and Figure shows its Simulation waveforms after applying CRC error detection and correction codes. All the coding and the simulation is performed on the XILINX software. The Simulation is performed on XILINX ISIM and Coding is done on XILINX ISE.
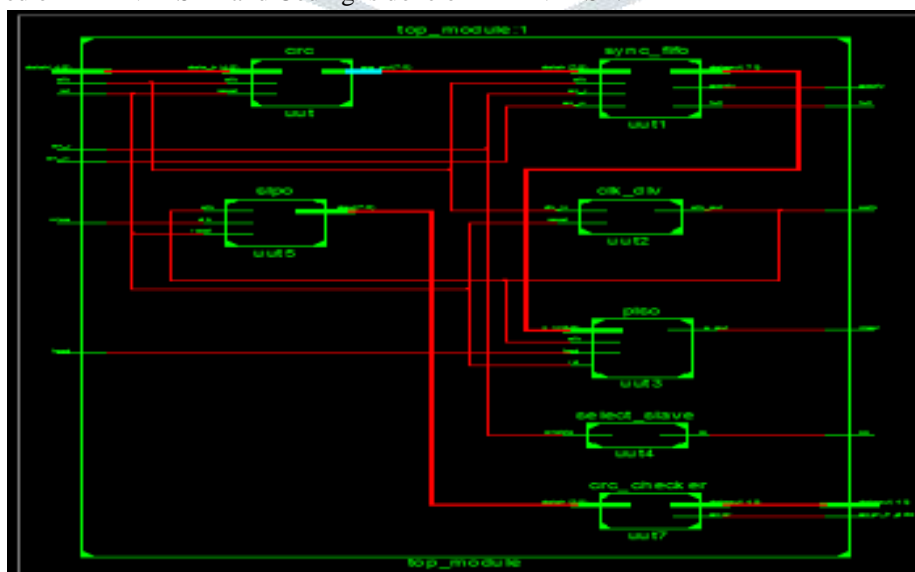
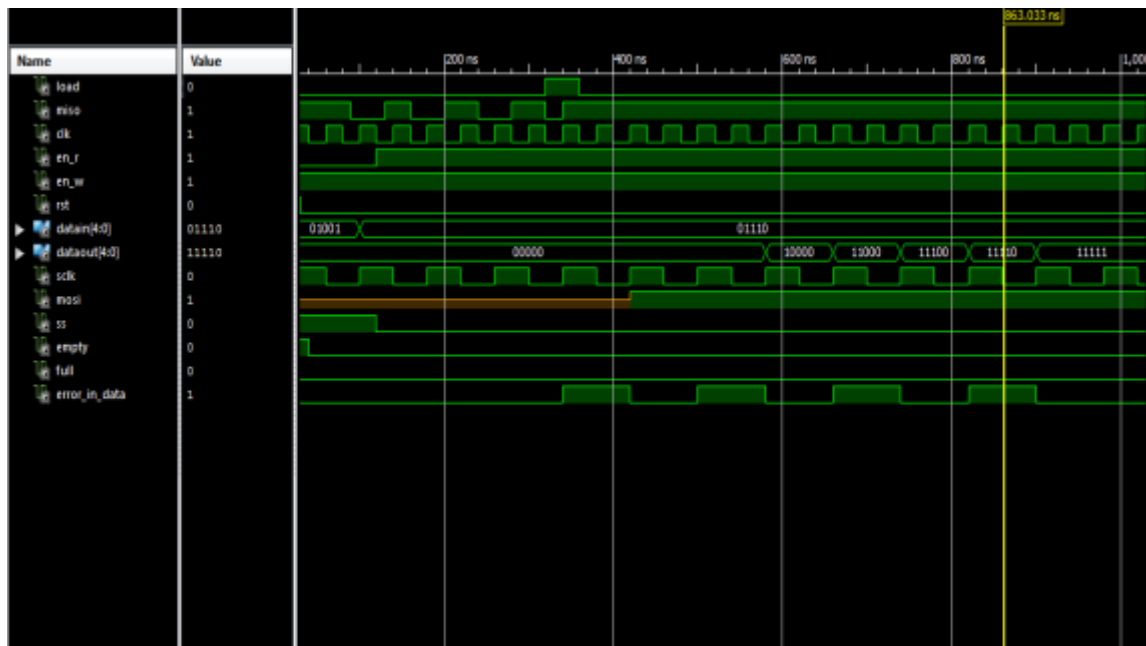**Fig** 3. Top Module Implementation of SPI with CRC

Fig 4. Simulation Waveforms

VI. CONCLUSION AND FUTURE SCOPE

The Error Detection and Correction on SPI Protocol is achieved using Cyclic Redundancy Check. SPI Protocol shows improvement in terms of the Error detection and Correction but with the loss in number of Address and Data Bits. In future several other Error detection and Correction techniques must be implemented and the performance of SPI must be measured.

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