A Low-Power VLSI Technique for Portable Electronic Devices

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Abstract: *In portable electronic devices that operate on battery power, it is essential to have power saving techniques to increase the operating time as they are energy constrained. This paper presents a novel power saving technique supported by two design models for multimedia purposes. The two designs are with two varying significance. The most significant part is turned off when it can't produce different results. This is done to save power consumption. The two design examples explored in this paper have varying hardware configurations thus reveal different realization. The models are namely multi-transform model and multimedia functional unit. The former computes three transforms for H.264 encoding while the latter supports six functions which are commonly used namely addition, multiplication, subtraction, interpolation, MAC and sum-of-absolute-difference. For these designs the proposed VLSI technique is capable of saving power by 27% and 24% respectively at the expence of 20% area overheads.*

Index Terms - *Low-power design, multimedia, digital signal processing, video coding, image coding*

I.   Introduction

Designing Integrated Circuits for portable electronic devices are essential is challenging as they are energy constraint. The ICs for such devices should be made energy efficient in order to let the devices operate long time. As many wireless, small handheld devices with innovative technologies came into existence, they are capable of processing multimedia or digital signal processing applications. As a matter of fact, the multimedia applications such as H.264 CODECs is very complex in terms of mathematical complexity [2] causing more power consumption in hand held multimedia enabled devices. This warrants new VLSI technique implementations for making such devices energy efficient. Many techniques came into existence for reducing power consumption in VLSI designs. They include dynamic voltage frequency scaling, multiple supply voltages, threshold-voltage controlling, power-down techniques, clock gating, switched-capacitance reduction, and voltage scaling [3], [6]. All these techniques are efficient in reducing power consumption with some cost due to multimedia designs. They achieve it by reducing dynamic power that has significant share in power dissipation. To improve the power saving features in VLSI designs, this paper proposes a novel technique that ensures low power dissipation while supporting two kinds of designs that have various capabilities. The existing techniques explored in [7]-[10] that focus on reducing dynamic power minimizing switched capacitance. In case of [7] while making arithmetic operations, the un used parts are turned off in order to reduce power consumption. This technique is known as partially guarded computation. It could reduce power usage up to 44% with area overheads up to 36%. The drawback with this technique is that it can't reduce power consumption in case of adders due to the kind of circuitry. A new adder was introduced in [8] which is a 32 bit model with two inputs namely sign extension and dynamic range determination in order to reduce power consumption. A multiplier is presented in [9] for effective dynamic range which resulted in Booth codes. Delay and area overheads are the two drawbacks of [9]. Glitching power minimization is the technique used in [10] for replacing existing gates with new ones which are equal in terms of functionality. It is capable of saving only 6.3% power dissipations. A double switched circuit block is used in [11] could reduce power dissipation during downtime. Finally DCT is used in [12] which follows adaptive bandwidth approach. However, it has trade offs between arithmetic precision and power consumption.

This paper explores the two design models and also the proposed tecniuqe for reducing power consumption. The flexible and scalable design of processor that supports multimedia is as given in fig. 1.
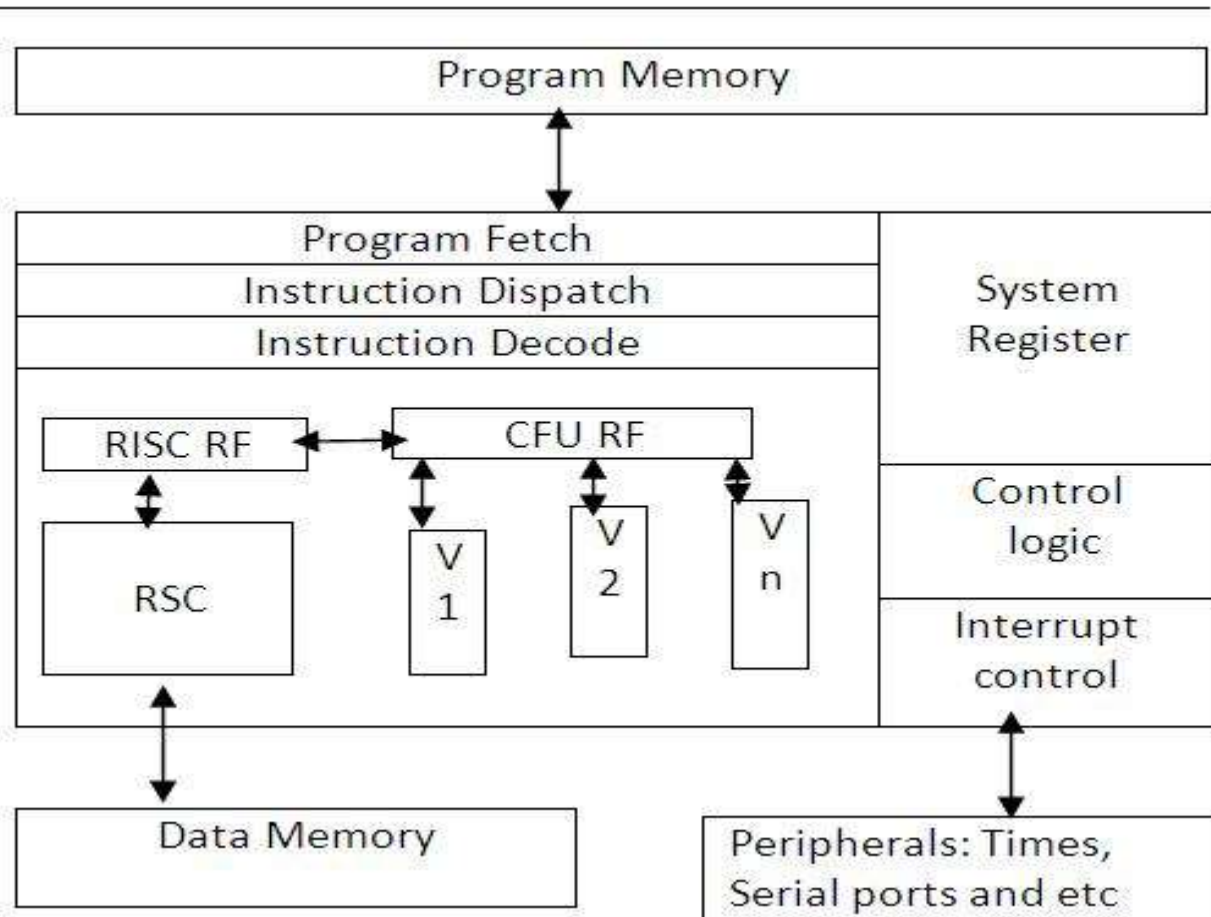
Fig. 1 –Multimedia processor

As can be seen in fig. 1, the proposed technique can be applied to two design models. In each design the realization is different with different hardware configurations. With much focus on the optimization, the proposed technique can reduce power dissipation with 1.8-V supply voltage.

The reminder of the paper is organized as described here. The proposed technique is explored in detail in section II. The two design examples are explored in section III. Implemetation is discussed in detail in section IV. Analysis and evaluation is provided in section V while the section VI makes conclusions to this paper.

II.   Proposed Technique

This section provides details about the proposed technique which reduces power dissipation. Under this technique two kinds of hardware designs are implemented and tested for the robustness of the proposed technique. In fact this paper presents a novel power saving technique supported by two design models for multimedia purposes.

carr-ctrl		$C_{ISP}, A_{and}, A_{nor}$							
		000	001	011	010	100	101	111	110
B_{and}, B_{nor}	00	0	0	0	0	0	0	0	0
	01	0	0	0	1	0	1	0	0
	11	0	0	0	0	0	0	0	0
	10	0	1	0	0	0	0	0	1

(a)

sign		$C_{lsp}, A_{and}, A_{nor}$							
		000	001	011	010	100	101	111	110
B_{and}, B_{nor}	00	0	0	0	0	0	0	0	0
	01	0	0	0	1	0	1	0	0
	11	0	0	0	0	0	0	0	0
	10	0	1	0	1	0	0	0	1

(b)

Fig. 2 – Representation so two signals as per KARNAUGH maps

As can be seen in fig. 2 (a) and (b), KARNAUGH maps are derived and presented. These tables have values that can lead to Boolean logical equations. A 16-bit adder/subtractor model has been designed as part of the proposed technique. Between eight and ninth bits this is divided into LSPA and MSP. The technique lies in the following fact. When MSP is compulsory, its input data remains same. However, when the MSP values are negligible, its input values are set to zero in order to avoid consumption of power. Based on the requirement the MSP operations are turned off thus reducing power consumption in the proposed technique. There are timing issues in the proposed technique which are described below.

✓ When MSP is turned off by the detection-logic in order to reduce power consumption, the SE unit compensates the outputs of MSP. The delay caused by the detection-logic unit cancels the time saved by getting rid of computations in MSP.

✓ When MSP is turned on by the detection-logic MSP circuts wait for possible notification from detection-logic unit in order to take the data as input. Here delay is caused by the detection-logic unit that will result in delay the circuitry as a whole with respect to 16 bit adder/subtractor.

✓ In case of the detection-logic remains in its decision, irrespective of the previous decision with regard to turning of or off the MSP, there will be negligle delay from as the path of the circuitry is same as usual.

III.   Design Examples Of Proposed Technique

There are two designs implemented in this paper. The first one is ETD with two categories of PEs. However, for computing 1D transform the four PEs are used. There are two PEs in the right hand side of the design too that are meant for computing 2-D transform. ETD exhibits eight pixels per cycle throughput. The second example design created for proposed technique is known as VMFU and it can support six types of mathematicaloperations as described in the beginning of this paper. In this design approach there are three considerations.

✓ Applying proposed technique to modified booth encoder.

✓ Applying it to the compression tree.

✓ Freezing the unused circuits and switching actions.

IV.   Implementation And Testing

The proposed techniuque with two design samples is realized and the two design samles are verified using MATLAB and VEROLOG for simulation. The simulation results are as given in table 1.

	Power Reduction (PR) (%)	Area (A, #tr.)	Magnitude Of PR/A
MUX	28.71	38572	3
OR	28.62	38376	2
CPL	29.69	37964	1

Table 1 –Results of the proposed technique

As seen in table 1, the power reduction, area and magnitude when different circuts are used in the experiments. When CPL circuits are used the magnitude, area and power reduction are higher when compared with that of OR and MUX circuits.

V.   Performance Evaluation

The proposed designs and also the technique which is energy efficient are evaluated here. Both ETD and adder/subtractor designs are evaluated towards the performance of the proposed technique.

Freq. (MHz)	Applications	Power (p, mW)		Reduction of P.(%)
		SPST ON	SPST OFF	
22	HD 720p	5.49	7.57	27.48
50	HD 1080i	12.05	16.59	27.37
100	Digital cinema	24.18	33.25	27.28

Table 2- Results of ETD with proposed technique

As can be seen in table 2, when the proposed technique is used the power consumption is greately minimized with various frequencies and devices.

Designs	Area (gate)	Freq. (MHz)	Throughput (M pixels/ sec)	TPUA (pixels sec/gate)
Kordasiewicz [20]	77280	107	1712	22.15k
Wang [21]	6538	80	320	48.94k
Wang [21] redesigned	6274	100	400	63.76k
Liu [22]	3524	129	129	36.61k
SPST-equipped ETD	7839	100	800	102.05k

Table 3 – Hardware efficiency comparisons

As can be seen in table 3, comparisons are made among various techniques including the proposed technique with respect to area, frequencfy, throughput and TPUA. In all parameters the proposed technique with ETD design is showing performance better.
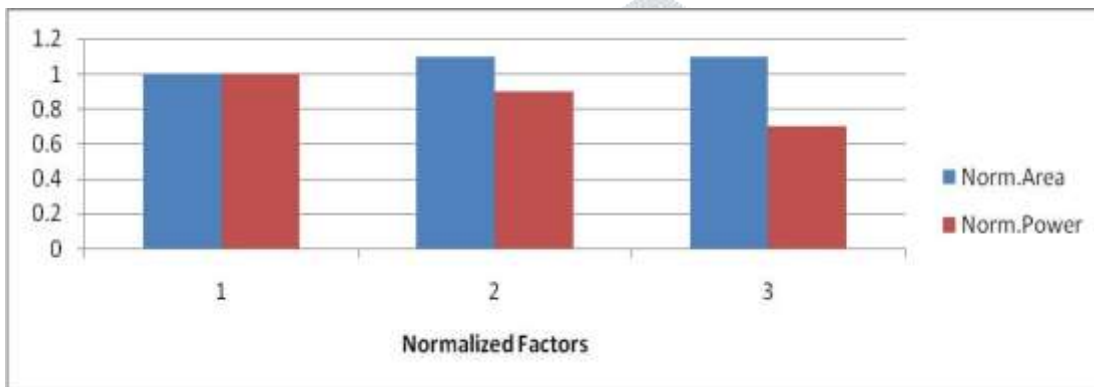

Fig. 3 –Improvements in Power Consumption

As can be seen in fig. 3, it is evident that on applying the proposed technique with VMFU, the technqque is applied to compression tree in the first place and then applied to modified booth decoder. Both applications together reduce power consumption of the proposed technique up to 24%.
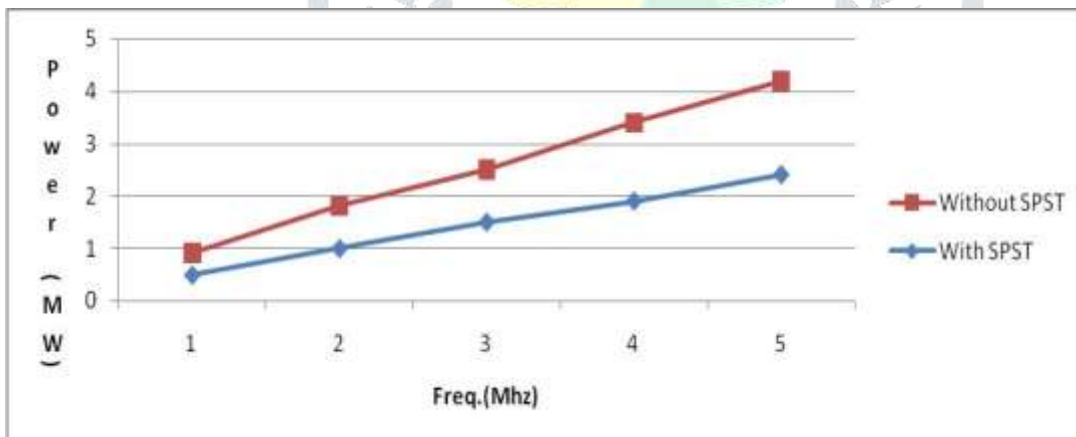

Fig. 4 –Power reduction using VMFU

As seen in fig. 4, it is evident that the power consumption is less with the usage of proposed techniquein the devices while the same is high when the technique is not used.
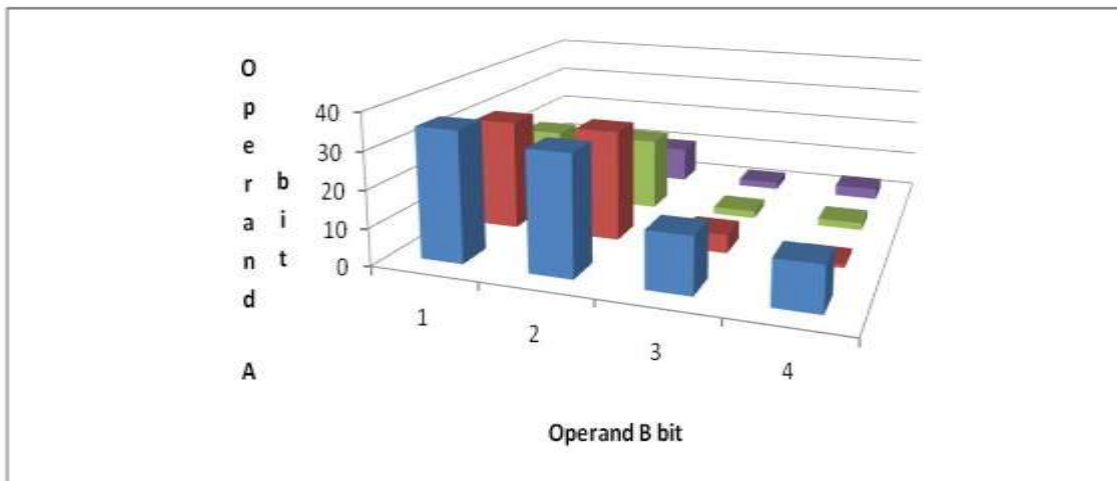
Fig. 5 – Power consumption of proposed technique for multiplication using VMFU

As can be seen in fig. 5, it is evident that for different effective ranges with respect to multiplication example, the power reduction capabilities of the proposed system with 4, 8, 12 and 16-bits.

VI.   Conclusion

This paper proposed an energy efficient technique for portable computing devices that supports multimedia applications. The proposed technique reduces dynamic power dissipation that is major part of the whole dissipation of power. An effective multi-transform coding design is proposed that could save up to 27% power with only 20% area overhead. The both approaches proposed in this paper are verified and implemented practically. The performance of these revealsthat the proposed technique is very good with given designs. Moreover the proposed technique is robust to voltage dropping, signal racing and leakage power problems.

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